Stereo 2.7-W Audio Power Amplifier (with DC_Volume Control)

Features

- Low Operating Current with 14mA
- Improved Depop Circuitry to Eliminate
- Turn-on and Turn-off Transients in Outputs
  High PSRR
- 32 Steps Volume Adjustable by DC Voltage with Hysteresis
- 2W per Channel Output Power into 4Ω Load at 5V, BTL Mode
- Two Output Modes Allowable with BTL and SE Modes Selected by SE/$\overline{\text{BTL}}$ pin
- Low Current Consumption in Shutdown Mode (50μA)
- Short Circuit Protection
- Power Off Depop Circuit Integration
- PDIP-16 & SOP-16 Packages Available
- Lead Free Available (RoHS Compliant)

General Description

APA2065 is a monolithic integrated circuit, which provides precise DC volume control, and a stereo bridged audio power amplifiers capable of producing 2.7W(2.0W) into 3Ω with less than 10%(1.0%) THD+N. The attenuator range of the volume control in APA2065 is from 20dB (DC_Vol=0V) to -80dB (DC_Vol=3.54V) with 32 steps. The advantage of internal gain setting can be less components and PCB area. Both of the depop circuitry and the thermal shutdown protection circuitry are integrated in APA2065, that reduce pops and clicks noise during power up or shutdown mode operation. It also improves the power off pop noise and protects the chip from being destroyed by over temperature and short current failure. To simplify the audio system design, APA2065 combines a stereo bridge-tied loads (BTL) mode for speaker drive and a stereo single-end (SE) mode for headphone drive into a single chip, where both modes are easily switched by the SE/$\overline{\text{BTL}}$ input control pin signal.

Applications

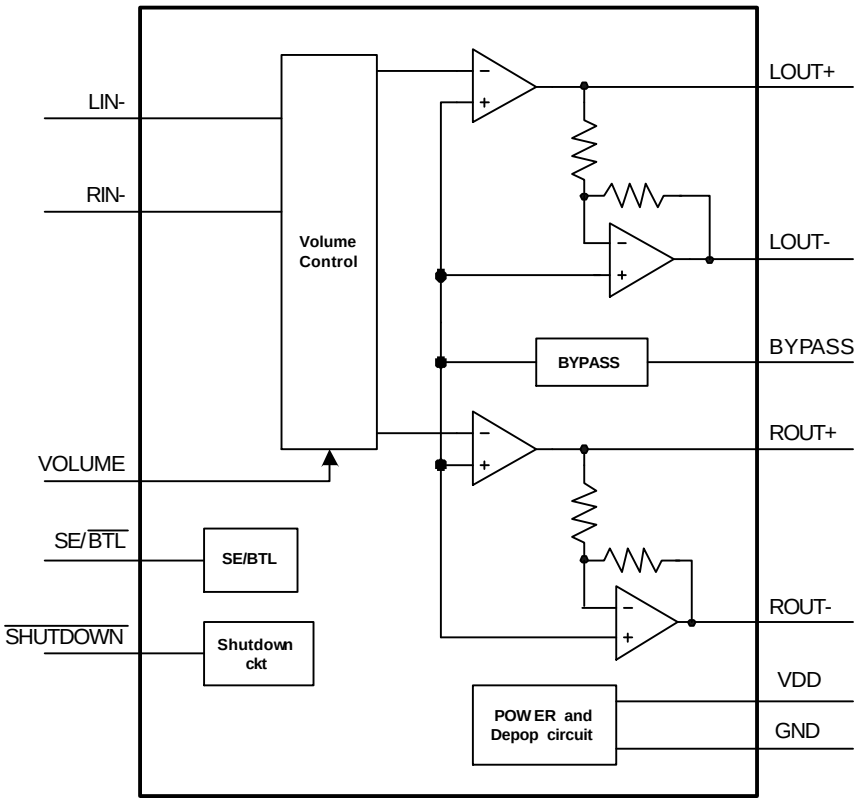
- NoteBook PC
- LCD Monitor or TV

Ordering and Marking Information

APA2065 □□-□□□ Lead Free Code Handling Code Temp. Range Package Code	Package Code J : PDIP-16 K : SOP-16 Temp. Range I : - 40 to 85 °C Handling Code TU : Tube TR : Tape & Reel TY : Tray Lead Free Code L : Lead Free Device Blank : Original Device
APA2065 J : APA2065 XXXXX	XXXXX - Date Code
APA2065 K : APA2065 XXXXX	XXXXX - Date Code

Note: ANPEC lead-free products contain molding compounds/die attach materials and 100% matte tin plate termination finish; which are fully compliant with RoHS and compatible with both SnPb and lead-free soldiering operations. ANPEC lead-free products meet or exceed the lead-free requirements of IPC/JEDEC J STD-020C for MSL classification at lead-free peak reflow temperature.

Block Diagram



Absolute Maximum Ratings

(Over operating free-air temperature range unless otherwise noted.)

Symbol	Parameter	Rating	Unit
V_{DD}	Supply Voltage Range	-0.3 to 6	V
V_{IN}	Input Voltage Range, SE/$\overline{BTL}$, $\overline{SHUTDOWN}$	-0.3 to V_{DD}+0.3	V
T_A	Operating Ambient Temperature Range	-40 to 85	°C
T_J	Maximum Junction Temperature	Intermal Limited*[1]	°C
T_{STG}	Storage Temperature Range	-65 to +150	°C
T_S	Soldering Temperature,10 seconds	260	°C
V_{ESD}	Electrostatic Discharge	-3000 to 3000*[2] -200 to 200*[3]	V
P_D	Power Dissipation	Intermal Limited	

Note:

1.APA2065 integrated internal thermal shutdown protection when junction temperature ramp up to 150°C

2.Human body model: C=100pF, R=1500Ω, 3 positives pulse plus 3 negative pulses

3.Machine model: C=200pF, L=0.5μF, 3 positive pulses plus 3 negative pulses

Recommended Operating Conditions

		Min.	Max.	Unit
Supply Voltage, V_{DD}		4.5	5.5	V
High level threshold voltage, V_{IH}	$\overline{SHUTDOWN}$	2		V
	SE/$\overline{BTL}$	4		
Low level threshold voltage, V_{IL}	$\overline{SHUTDOWN}$		1.0	V
	SE/$\overline{BTL}$		3	
Common mode input voltage, V_{ICM}		V_{DD}-1.0		V

Thermal Characteristics

Symbol	Parameter	Value	Unit
R_{THJA}	Thermal Resistance from Junction to Ambient in Free Air		
	PDIP-16	45	K/W
	SOP-16	60	K/W

Electrical Characteristics

V_{DD}=5V, -20°C<T_A<85°C (unless otherwise noted)

Symbol	Parameter	Test Condition	APA2065			Unit
			Min.	Typ.	Max.	
V_{DD}	Supply Voltage		4.5		5.5	V
I_{DD}	Supply Current	SE/$\overline{BTL}$=0V		14	25	mA
		SE/$\overline{BTL}$=5V		8.0	15	
I_{SD}	Supply Current in Shutdown Mode	SE/$\overline{BTL}$=5V $\overline{SHUTDOWN}$=0V		50		µA
I_{IH}	High input Current			900		nA
I_{IL}	Low Input Current			900		nA
V_{OS}	Output Differential Voltage			5		mV

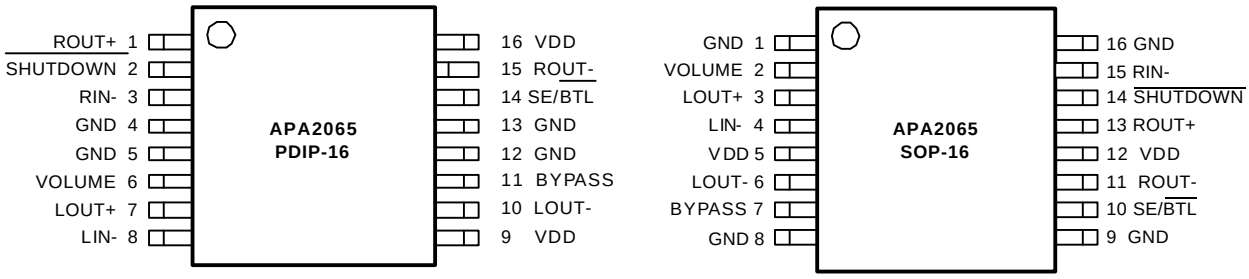
Operating Characteristics, BTL mode V_{DD}=5V,T_A=25°C,R_L=4Ω, Gain=2V/V (unless otherwise noted)

Symbol	Parameter	Test Condition	APA2065			Unit
			Min.	Typ.	Max.	
P_O	Maximum Output Power	THD=10%, R_L=3Ω, Fin=1kHz		2.7		W
		THD=10%, R_L=4Ω, Fin=1kHz		2.3		
		THD=10%, R_L=8Ω, Fin=1kHz		1.5		
		THD=1%, R_L=3Ω, Fin=1kHz		2.0		
		THD=1%, R_L=4Ω, Fin=1kHz		1.9		
		THD=0.5%, R_L=8Ω, Fin=1kHz	1	1.1		
THD+N	Total Harmonic Distortion Plus Noise	P_O=1.5W, R_L=4Ω, Fin=1kHz		0.05		%
		P_O=1W, R_L=8Ω, Fin=1kHz		0.07		
PSRR	Power Ripple Rejection Ratio	V_{IN}=0.1Vrms, R_L=8Ω, C_B=1µF, Fin=120Hz		60		dB
Xtalk	Channel Separation	C_B=1µF, R_L=8Ω, Fin=1kHz		90		dB
S/N	Signal to Noise Ratio	P_O=1.1W, R_L=8Ω, A_wieght		95		dB

Operating Characteristics, SE mode V_{DD}=5V,T_A=25°C,R_L=4Ω, Gain=1V/V (unless otherwise noted)

Symbol	Parameter	Test Condition	APA2065			Unit
			Min.	Typ.	Max.	
P_O	Maximum Output Power	THD=10%, R_L=8Ω, Fin=1kHz		400		mW
		THD=10%, R_L=32Ω, Fin=1kHz		110		
		THD=1%, R_L=8Ω, Fin=1kHz		320		
		THD=1%, R_L=32Ω, Fin=1kHz		90		
THD+N	Total Harmonic Distortion Plus Noise	P_O=250mW, R_L=8Ω, Fin=1kHz		0.08		%
		P_O=75mW, R_L=32Ω, Fin=1kHz		0.08		
PSRR	Power Ripple Rejection Ratio	V_{IN}=0.1Vrms, R_L=8Ω, C_B=1µF, Fin=120Hz		48		dB
Xtalk	Channel Separation	C_B=1µF, R_L=32Ω, Fin=1kHz		100		dB
S/N	Signal to Noise Ratio	P_O=75mW, SE, R_L=32Ω, A_wieght		100		dB

Pin Description



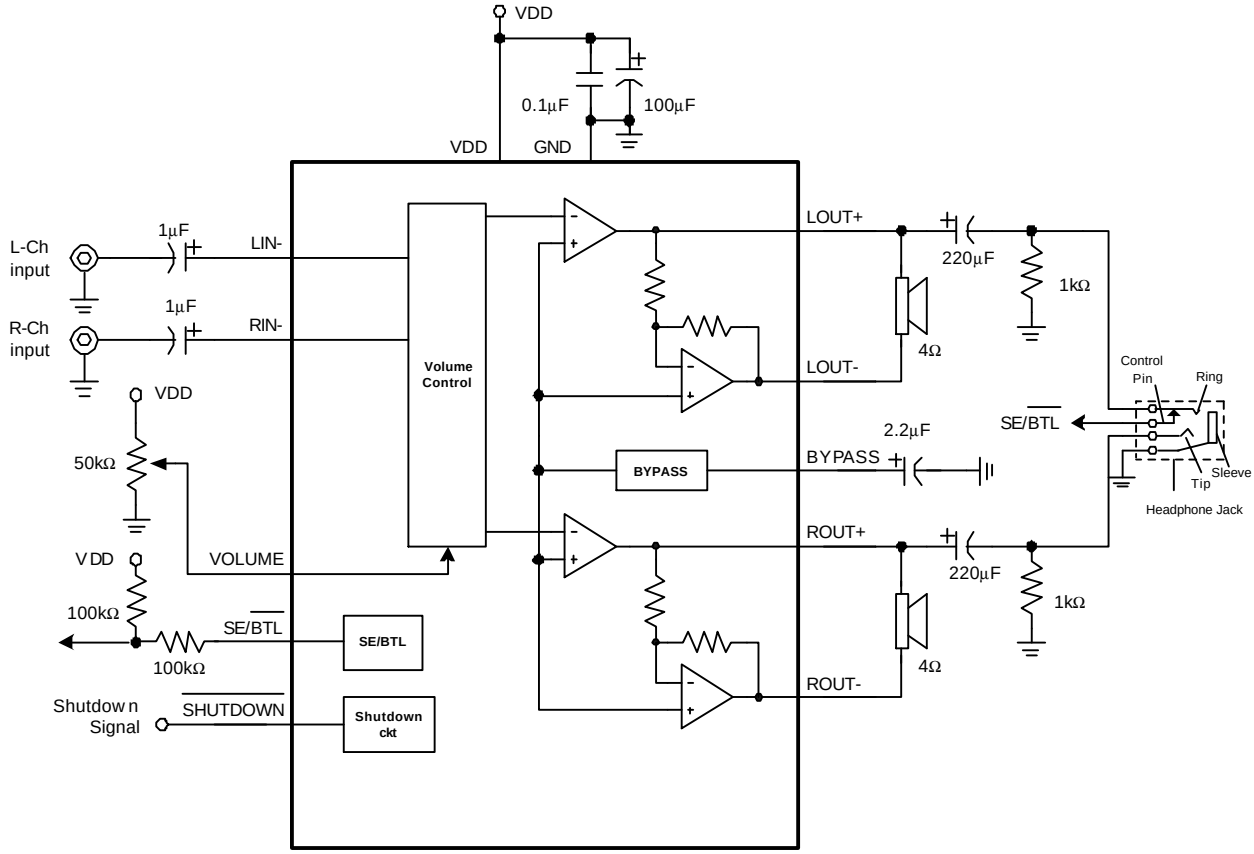
Pin Function Description

Pin Name	Config.	Description
GND		Ground connection, Connected to thermal pad.
VOLUME	I/P	Input signal for internal volume gain setting.
LOUT+	O/P	Left channel positive output in BTL mode and SE mode.
LIN-	I/P	Left channel input terminal
LOUT-	O/P	Left channel negative output in BTL mode and high impedance in SE mode.
BYPASS		Bias voltage generator
SE/$\overline{BTL}$	I/P	Output mode control input, high for SE output mode and low for BTL mode.
ROUT-	O/P	Right channel negative output in BTL mode and high impedance in SE mode.
VDD		Supply voltage for internal circuit excepting power amplifier.
ROUT+	O/P	Right channel positive output in BTL mode and SE mode.
$\overline{SHUTDOWN}$	I/P	It will be into shutdown mode when pull low.
RIN-	I/P	Right channel input terminal

Control Input Table

SE/$\overline{BTL}$	$\overline{SHUTDOWN}$	Operating mode
X	L	Shutdown mode
L	H	BTL out
H	H	SE out

Typical Application Circuit



Volume Control Table_BTL Mode

Supply Voltage Vdd=5V

Gain(dB)	High(V)	Low(V)	Hysteresis(mV)	Recommended Voltage(V)
20	0.12	0.00		0
18	0.23	0.17	52	0.20
16	0.34	0.28	51	0.31
14	0.46	0.39	50	0.43
12	0.57	0.51	49	0.54
10	0.69	0.62	47	0.65
8	0.80	0.73	46	0.77
6	0.91	0.84	45	0.88
4	1.03	0.96	44	0.99
2	1.14	1.07	43	1.10
0	1.25	1.18	41	1.22
-2	1.37	1.29	40	1.33
-4	1.48	1.41	39	1.44
-6	1.59	1.52	38	1.56
-8	1.71	1.63	37	1.67

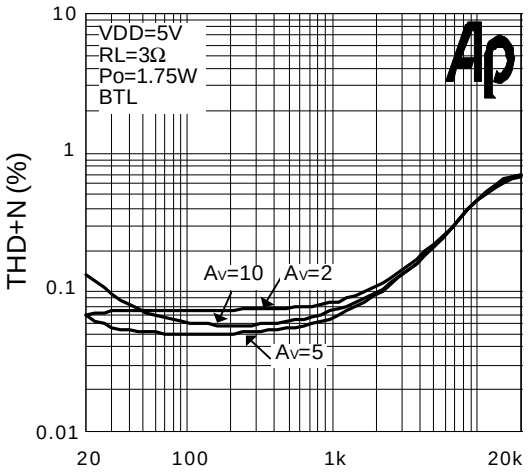
Volume Control Table_BTL Mode (Cont.)

Supply Voltage Vdd=5V

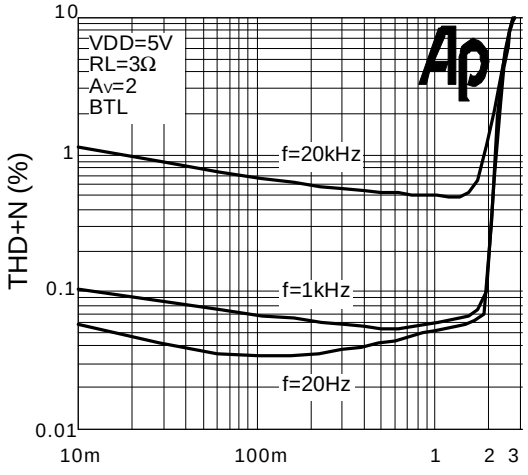
Gain(dB)	High(V)	Low(V)	Hysteresis(mV)	Recommended Voltage(V)
-10	1.82	1.74	35	1.78
-12	1.93	1.85	34	1.89
-14	2.05	1.97	33	2.01
-16	2.16	2.08	32	2.12
-18	2.28	2.19	30	2.23
-20	2.39	2.30	29	2.35
-22	2.50	2.42	28	2.46
-24	2.62	2.53	27	2.57
-26	2.73	2.64	26	2.69
-28	2.84	2.75	24	2.80
-30	2.96	2.87	23	2.91
-32	3.07	2.98	22	3.02
-34	3.18	3.09	21	3.14
-36	3.30	3.20	20	3.25
-38	3.41	3.32	18	3.36
-40	3.52	3.43	17	3.48
-80	5.00	3.54	16	5

Typical Characteristics

THD+N vs. Frequency

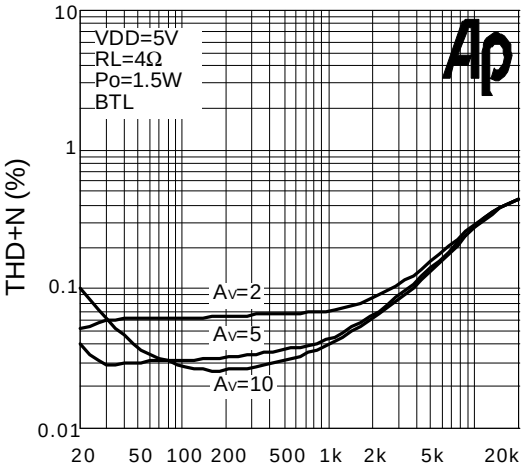


THD+N vs. Output Power

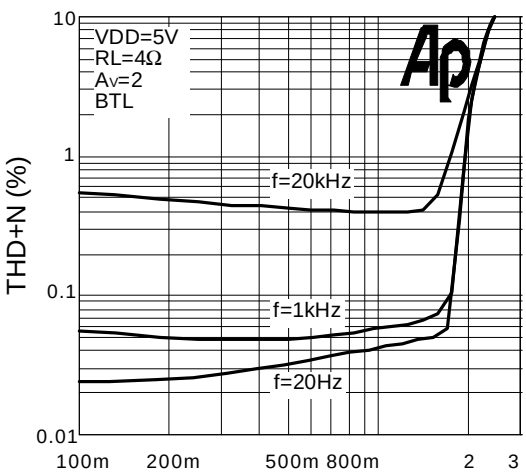


Typical Characteristics

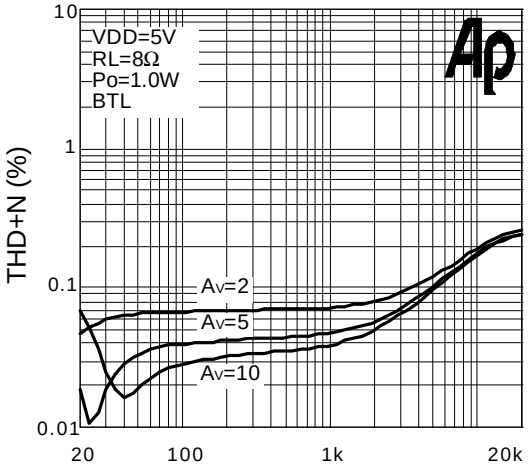
THD+N vs. Frequency



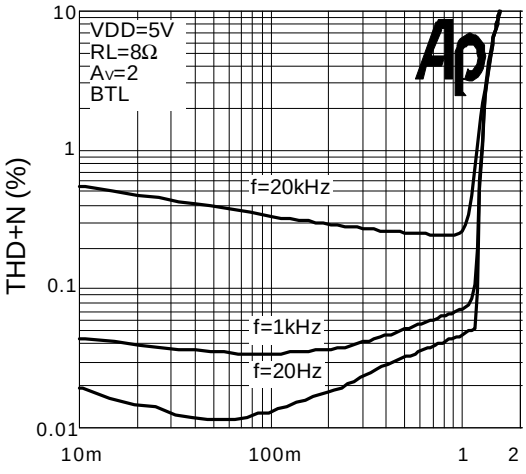
THD+N vs. Output Power



THD+N vs. Frequency

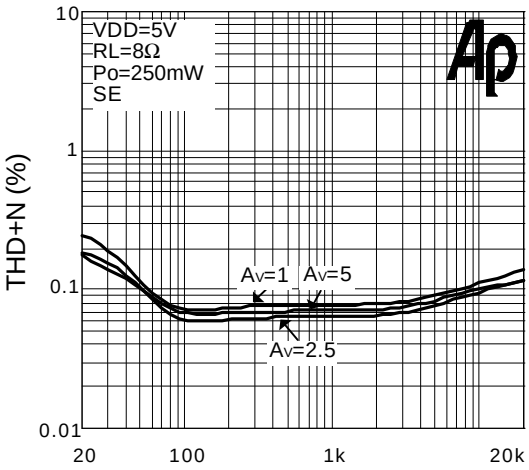


THD+N vs. Output Power

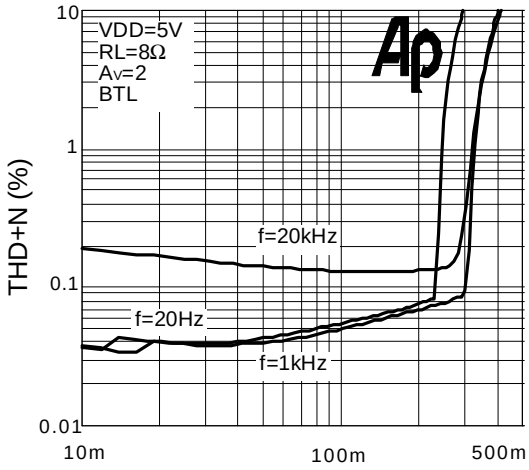


Typical Characteristics (Cont.)

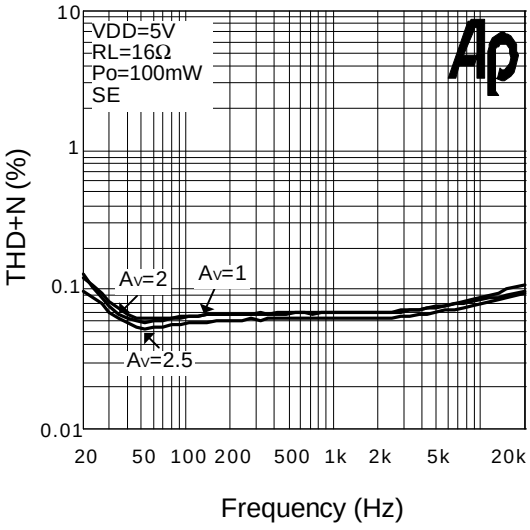
THD+N vs. Frequency



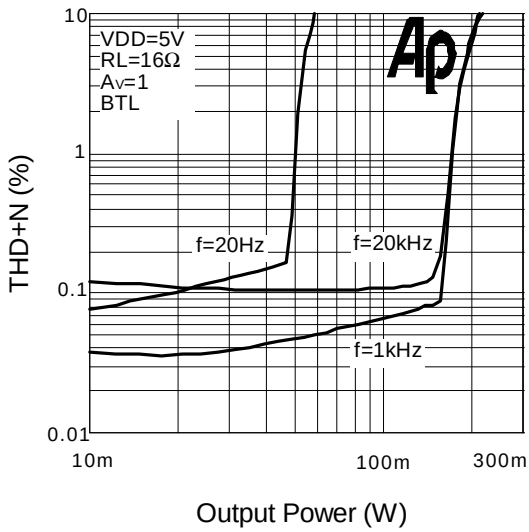
THD+N vs. Output Power



THD+N vs. Frequency

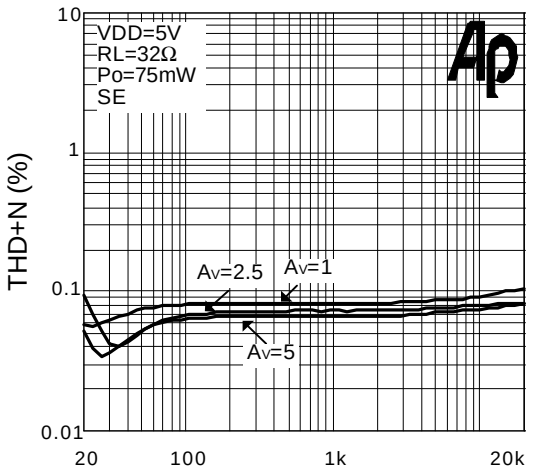


THD+N vs. Output Power

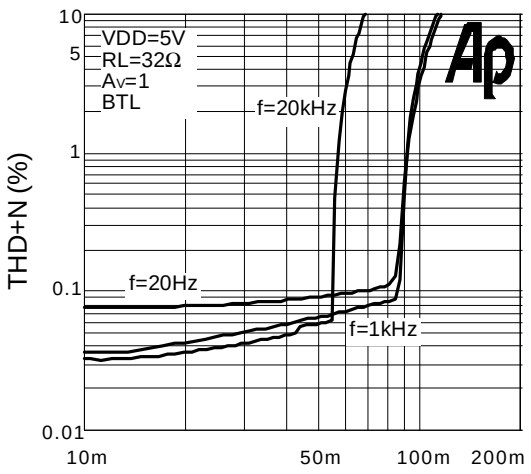


Typical Characteristics (Cont.)

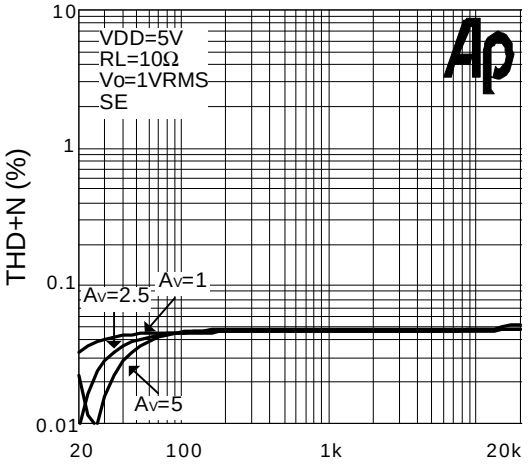
THD+N vs. Frequency



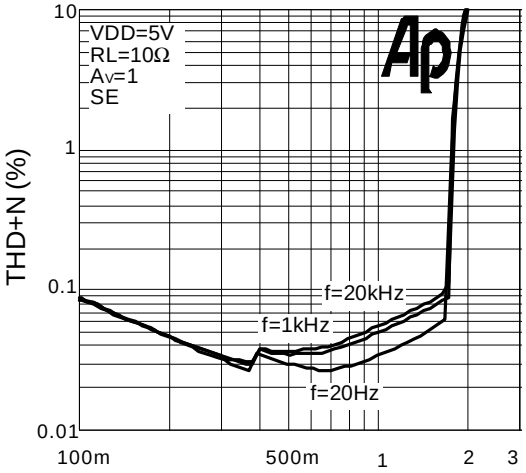
THD+N vs. Output Power



THD+N vs. Frequency



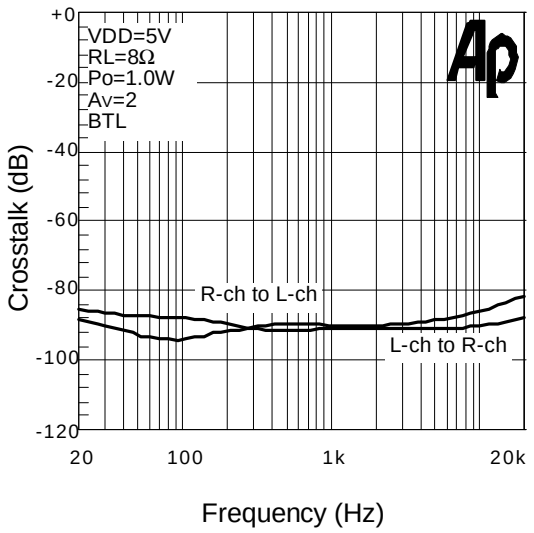
THD+N vs. Output Swing



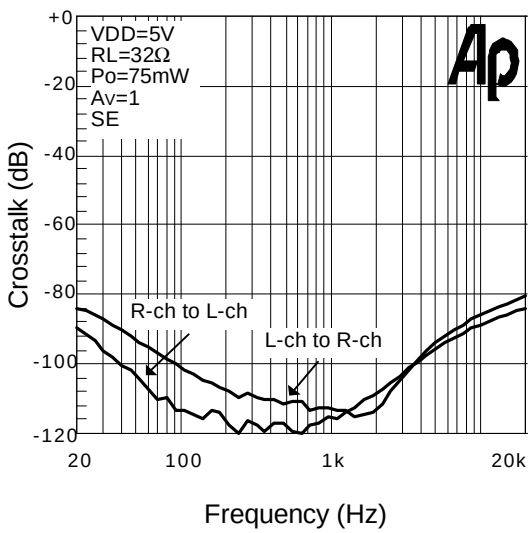
Note:Dropout voltage definition:V_{IN}-V_{OUT} when V_{OUT} is 2% below the value of V_{OUT} for V_{IN}= V_{OUT}+1V

Typical Characteristics (Cont.)

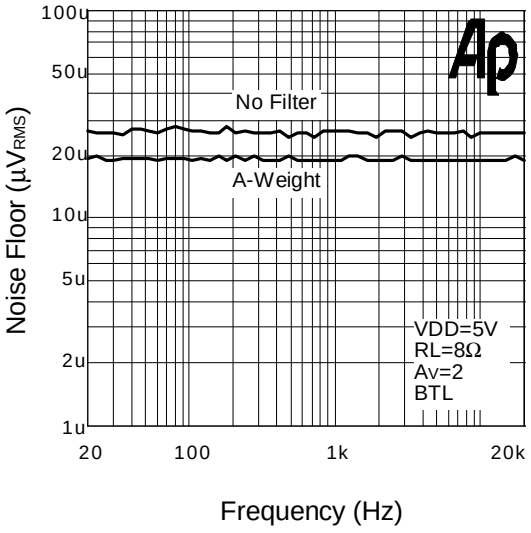
Crosstalk vs. Frequency



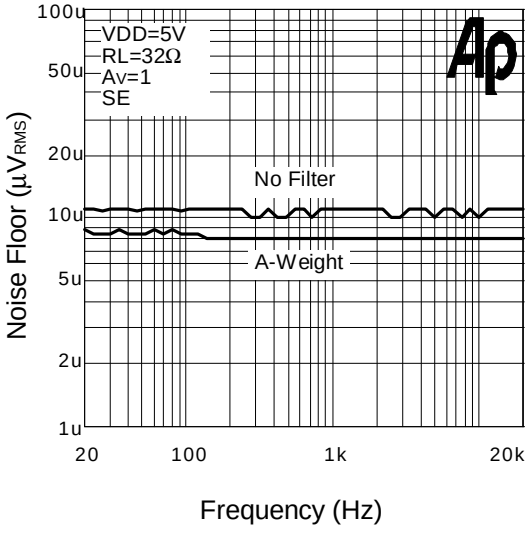
Crosstalk vs. Frequency



Noise Floor vs. Frequency

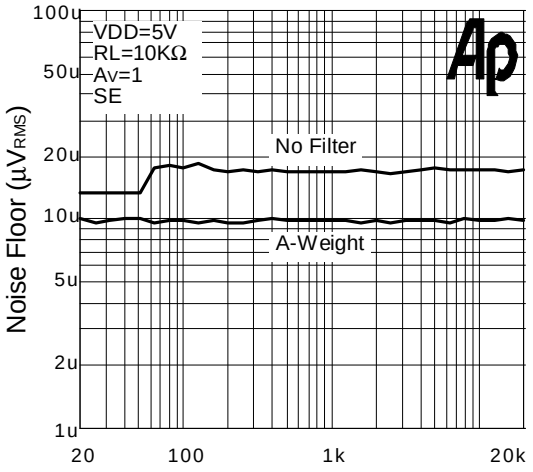


Noise Floor vs. Frequency

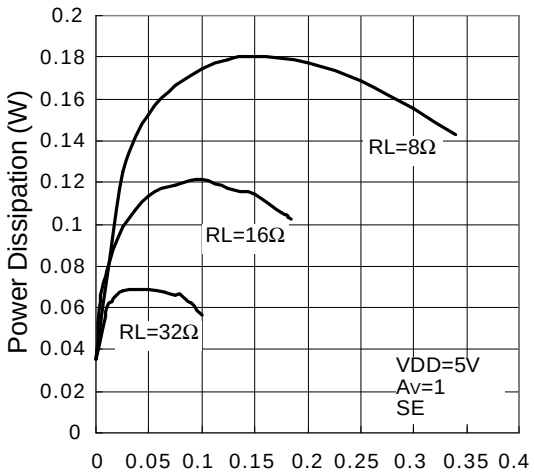


Typical Characteristics (Cont.)

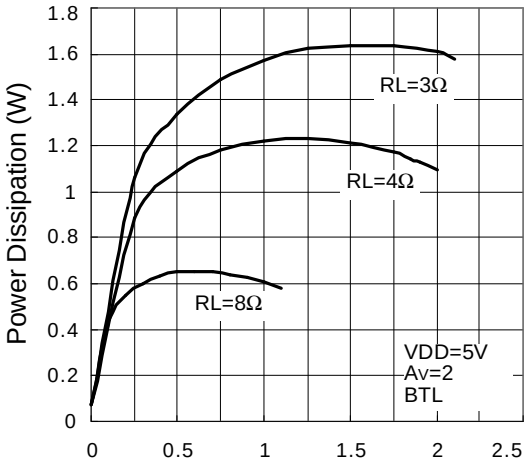
Noise Floor vs. Frequency



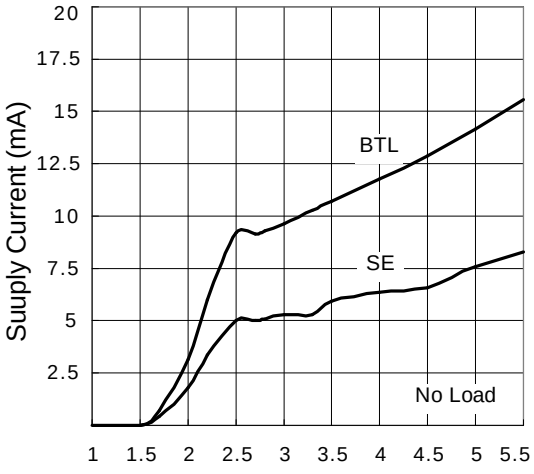
Power Dissipation vs. Output Power



Power Dissipation vs. Output Power

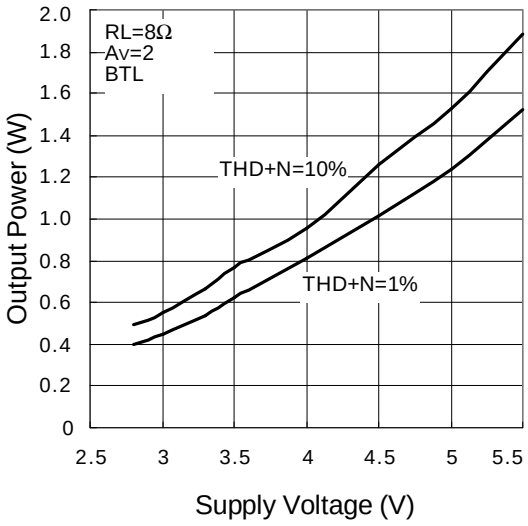


Supply Current vs. Supply Voltage

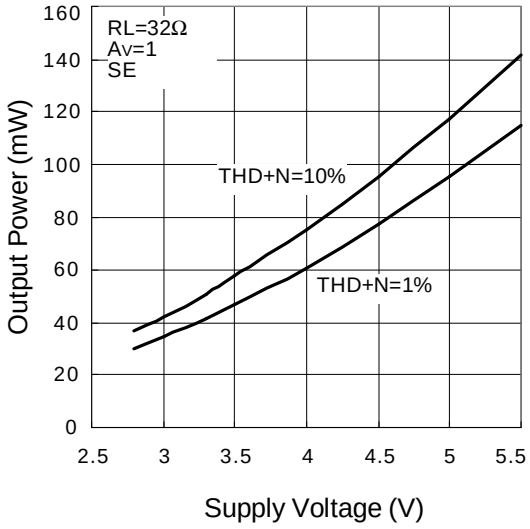


Typical Characteristics (Cont.)

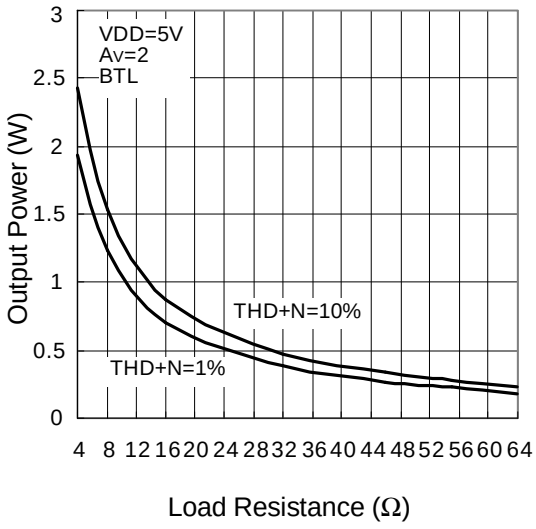
Output Power vs. Supply Voltage



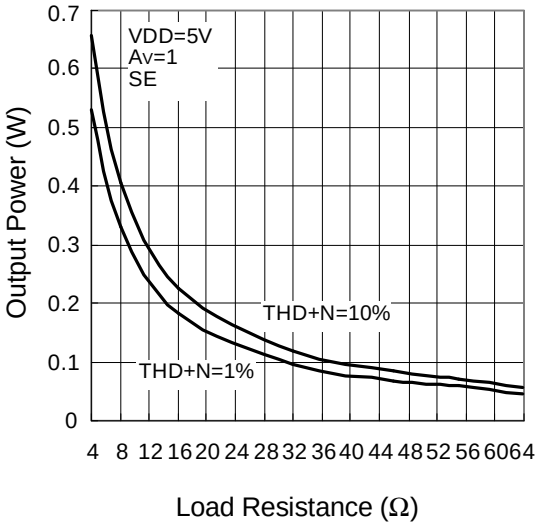
Output Power vs. Supply Voltage



Output Power vs. Load Resistance

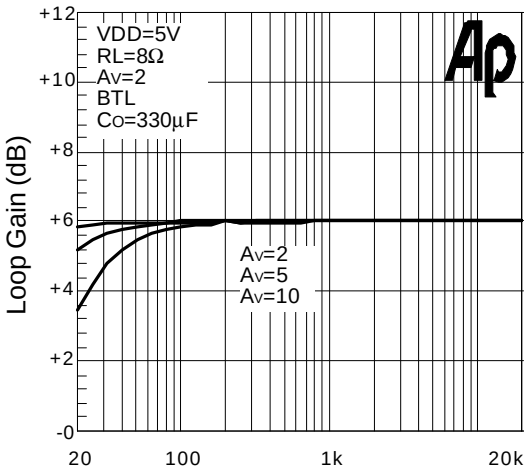


Output Power vs. Load Resistance

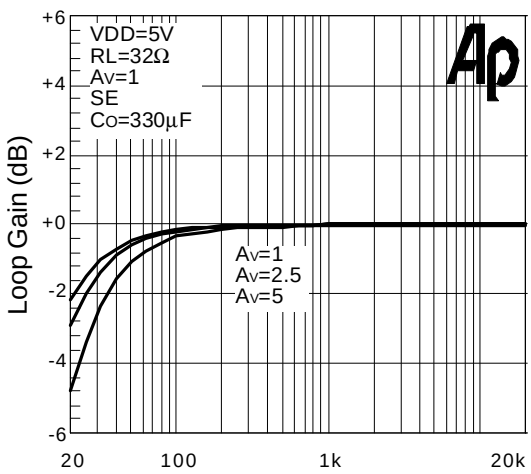


Typical Characteristics (Cont.)

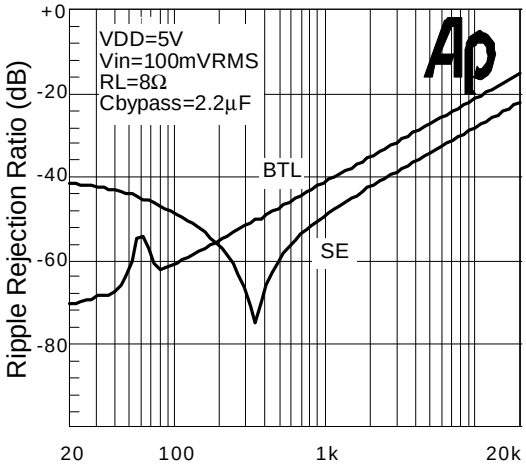
Close Loop Response



Close Loop Response



PSRR vs. Frequency



Application Descriptions

BTL Operation

The APA2065 output stage (power amplifier) has two pairs of operational amplifiers internally, allowed for different amplifier configurations.

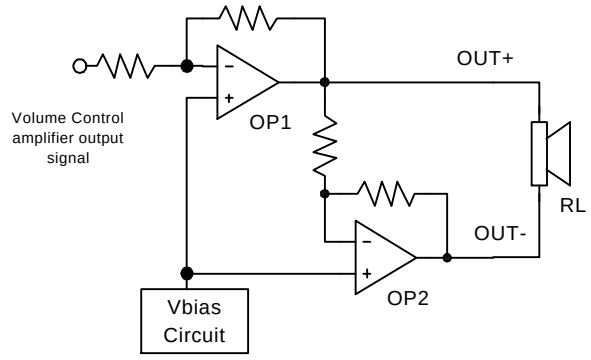


Figure 1: APA2065 internal configuration

(each channel)

The power amplifier's OP1 gain is setting by internal unity-gain and input audio signal is come from internal volume control amplifier, while the second amplifier OP2 is internally fixed in a unity-gain, inverting configuration. Figure 1 shows that the output of OP1 is connected to the input to OP2, which results in the output signals of with both amplifiers with identical in magnitude, but out of phase 180°. Consequently, the differential gain for each channel is 2 x (Gain of SE mode).

By driving the load differentially through outputs OUT+ and OUT-, an amplifier configuration commonly referred to as bridged mode is established. BTL mode operation is different from the classical single-ended SE amplifier configuration where one side of its load is connected to ground.

A BTL amplifier design has a few distinct advantages over the SE configuration, as it provides differential drive to the load, thus doubling the output swing for a specified supply voltage.

Four times the output power same conditions. A BTL configuration, such as the one used in APA2065, also creates a second advantage over SE amplifiers. Since the differential outputs, ROUT+, ROUT-, LOUT+, and LOUT-, are biased at half-supply, no need DC voltage exists across the load. This eliminates the need for an output coupling capacitor which is required in a single supply, SE configuration.

Single-Ended Operation

Consider the single-supply SE configuration shown Application Circuit. A coupling capacitor is required to block the DC offset voltage from reaching the load. These capacitors can be quite large (approximately 33µF to 1000µF) so they tend to be expensive, occupy valuable PCB area, and have the additional drawback of limiting low-frequency performance of the system (refer to the Output Coupling Capacitor). The rules described still hold with the addition of the following relationship:

$$\frac{1}{\text{Cbypass x } 125k\Omega} \leq \frac{1}{RiCi} << \frac{1}{R_L C_C} \qquad (1)$$

Output SE/$\overline{\text{BTL}}$ Operation

The ability of the APA2065 to easily switch between BTL and SE modes is one of its most important costs saving features. This feature eliminates the requirement for an additional headphone amplifier in applications where internal stereo speakers are driven in BTL mode but external headphone or speakers must be accommodated.

Internal to the APA2065, two separate amplifiers drive OUT+ and OUT- (see Figure 1). The SE/BTL input controls the operation of the follower amplifier that drives LOUT- and ROUT-.

• When SE/$\overline{\text{BTL}}$ is held low, the OP2 is turn on and the APA2065 is in the BTL mode.

Application Descriptions (Cont.)

Output SE/$\overline{BTL}$ Operation (Cont.)

- When SE/$\overline{BTL}$ is held high, the OP2 is in a high output impedance state, which configures the APA2065 as SE driver from OUT+. I_{DD} is reduced by approximately one-half in SE mode.

Control of the SE/$\overline{BTL}$ input can be a logic-level TTL source or a resistor divider network or the stereo headphone jack with switch pin as shown in Application Circuit.

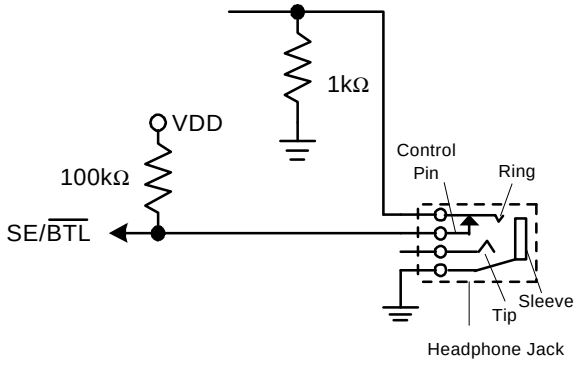


Figure 2: SE/$\overline{BTL}$ input selection by phonejack plug

In Figure 2, input SE/$\overline{BTL}$ operates as follows :

When the phonejack plug is inserted, the 1kΩ resistor is disconnected and the SE/$\overline{BTL}$ input is pulled high and enables the SE mode. When the input goes high, the OUT- amplifier is shutdown causing the speaker to mute. The OUT+ amplifier then drives through the output capacitor (C_C) into the headphone jack. When there is no headphone plugged into the system, the contact pin of the headphone jack is connected from **the signal pin,** the voltage divider set up by resistors 100kΩ and 1kΩ.

Resistor 1kΩ then pulls low the SE/$\overline{BTL}$ pin, enabling the BTL function.

Volume Control Function

APA2065 has an internal stereo volume control whose setting is a function of the DC voltage applied to the VOLUME input pin. The APA2065 volume control consists of 32 steps that are individually selected by a variable DC voltage level on the VOLUME control pin. The range of the steps, controlled by the DC voltage, are from 20dB to -80dB. Each gain step corresponds to a specific input voltage range, as shown in table. To minimize the effect of noise on the volume control pin, which can affect the selected gain level, hysteresis and clock delay are implemented. The amount of hysteresis corresponds to half of the step width, as shown in volume control graph.

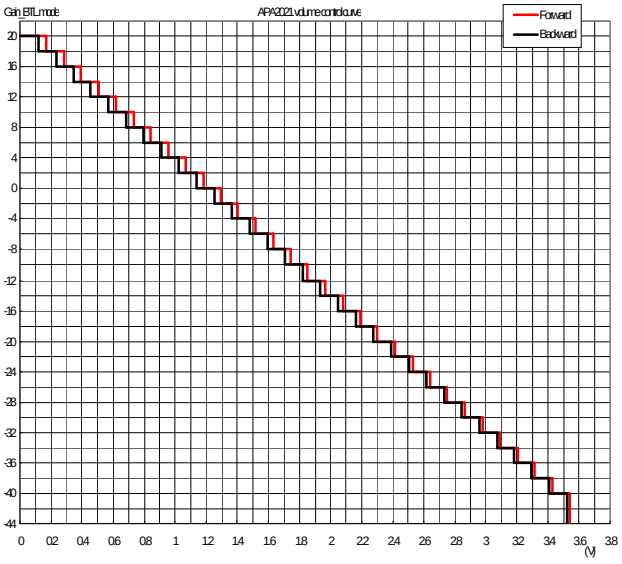


Figure 3: Gain setting vs VOLUME pin voltage

For highest accuracy, the voltage shown in the 'recommended voltage' column of the table is used to select a desired gain. This recommended voltage is exactly halfway between the two nearest transitions. The gain levels are 2dB/step from 20dB to -40dB in BTL mode, and the last step at -80dB as mute mode.

Input Resistance, Ri

The gain for each audio input of the APA2065 is set by the internal resistors (Ri and Rf) of volume control amplifier in inverting configuration.

Application Descriptions (Cont.)

Input Resistance, Ri (Cont.)

$$\text{SE Gain} = A_V = -\frac{R_F}{Ri} \quad (2)$$

$$\text{BTL Gain} = -2 \times \frac{R_F}{Ri} \quad (3)$$

BTL mode operation brings the factor of 2 in the gain equation due to the inverting amplifier mirroring the voltage swing across the load. For the varying gain setting, APA2065 generates each input resistance on figure 4. The input resistance will affect the low frequency performance of audio signal. The minmum input resistance is 10kΩ when gain setting is 20dB and the resistance will ramp up when close loop gain below 20dB. The input resistance has wide variation (+/-10%) caused by process variation.

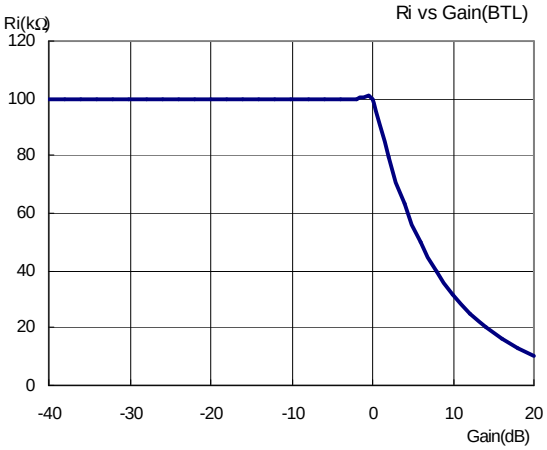


Figure 4: Input resistance vs Gain setting

Input Capacitor, Ci

In the typical application an input capacitor, Ci, is required to allow the amplifier to bias the input signal to the proper DC level for optimum operation. In this case, Ci and the minimum input impedance Ri (10kΩ) form a high-pass filter with the corner frequency determined in the follow equation:

$$F_C(\text{highpass}) = \frac{1}{2\pi \times 10k\Omega \times Ci} \quad (4)$$

The value of Ci is important to consider as it directly affects the low frequency performance of the circuit. Consider the example where Ri is 10kΩ and the specification calls for a flat bass response down to 100Hz. Equation is reconfigured as follow :

$$Ci = \frac{1}{2\pi \times 10k\Omega \times f_C} \quad (5)$$

Consider to input resistance variation, the Ci is 0.16μF so one would likely choose a value in the range of 0.22μF to 1.0μF.

A further consideration for this capacitor is the leakage path from the input source through the input network (Ri+Rf, Ci) to the load. This leakage current creates a DC offset voltage at the input to the amplifier that reduces useful headroom, especially in high gain applications. For this reason a low-leakage tantalum or ceramic capacitor is the best choice. When polarized capacitors are used, the positive side of the capacitor should face the amplifier input in most applications as the DC level there is held at $V_{DD}/2$, which is likely higher that the source DC level. Please note that it is important to confirm the capacitor polarity in the application.

Effective Bypass Capacitor, Cbypass

As other power amplifiers, proper supply bypassing is critical for low noise performance and high power supply rejection.

The capacitors located on both the bypass and power supply pins should be as close to the device as possible. The effect of a larger bypass capacitor will improve PSRR due to increased supply stability. Typical applications employ a 5V regulator with 1.0μF and a 0.1μF bypass capacitor as supply filtering. This does not eliminate the need for bypassing the supply nodes of the APA2065. The selection of bypass capacitors, especially Cbypass, is thus dependent upon desired PSRR requirements, click and pop performance.

Application Descriptions (Cont.)

Effective Bypass Capacitor, Cbypass (Cont.)

To avoid start-up pop noise occurred, the bypass voltage should rise slower than the input bias voltage and the relationship shown in equation (6) should be maintained.

$$\frac{1}{Cbypass \times 125k\Omega} << \frac{1}{100k\Omega \times Ci} \qquad (6)$$

The bypass capacitor is fed thru from a 125kΩ resistor inside the amplifier and the 100kΩ is maximum input resistance of (Ri+ Rf). Bypass capacitor, Cb, values of 3.3µF to 10µF ceramic or tantalum low-ESR capacitors are recommended for the best THD and noise performance.

The bypass capacitance also effects to the start up time. It is determined in the following equation:

$$Tstart\ up = 5 \times (Cbypass \times 125K\Omega) \qquad (7)$$

Output Coupling Capacitor, Cc

In the typical single-supply SE configuration, an output coupling capacitor (Cc) is required to block the DC bias at the output of the amplifier thus preventing DC currents in the load. As with the input coupling capacitor, the output coupling capacitor and impedance of the load form a high-pass filter governed by equation.

$$F_C(highpass) = \frac{1}{2\pi R_L C_C} \qquad (8)$$

For example, a 330µF capacitor with an 8Ω speaker would attenuate low frequencies below 60.6Hz. The main disadvantage, from a performance standpoint, is the load impedance is typically small, which drives the low-frequency corner higher degrading the bass response. Large values of C_C are required to pass low frequencies into the load.

Power Supply Decoupling, Cs

The APA2065 provides two independent power inputs for right channel and left channel used. PV_{DD} is used for power amplifier only and V_{DD} is used for volume control amplifier and internal circuit excepting power amplifier. The APA2065 is a high-performance CMOS audio amplifier that requires adequate power supply decoupling to ensure the output total harmonic distortion (THD) is as low as possible. Power supply decoupling also prevents the oscillations causing by long lead length between the amplifier and the speaker. The optimum decoupling is achieved by using two different type capacitors that target on different type of noise on the power supply leads.

For higher frequency transients, spikes, or digital hash on the line, a good low equivalent-series-resistance (ESR) ceramic capacitor, typically 0.1µF placed as close as possible to the device V_{DD} lead works best. For filtering lower-frequency noise signals, a large aluminum electrolytic capacitor of 10µF or greater placed near the audio power amplifier is recommended.

Optimizing Depop Circuitry

Circuitry has been included in the APA2065 to minimize the amount of popping noise at power-up and when coming out of shutdown mode. Popping occurs whenever a voltage step is applied to the speaker. In order to eliminate clicks and pops, all capacitors must be fully discharged before turn-on. Rapid on/off switching of the device or the shutdown function will cause the click and pop circuitry.

The value of Ci will also affect turn-on pops (Refer to Effective Bypass Capacitance). The bypass voltage ramp up should be slower than input bias voltage. Although the bypass pin current source cannot be modified, the size of Cbypass can be changed to alter the device turn-on time and the amount of clicks and pops. By increasing the value of Cbypass, turn-on pop can be reduced. However, the tradeoff for using a larger bypass capacitor is to increase the turn-on time for this device. There is a linear relationship between the

Application Descriptions (Cont.)

Optimizing Depop Circuitry (Cont.)

size of Cbypass and the turn-on time. In a SE configuration, the output coupling capacitor, C_C, is of particular concern.

This capacitor discharges through the internal 10kΩ resistors. Depending on the size of C_C, the time constant can be relatively large. To reduce transients in SE mode, an external 1kΩ resistor can be placed in parallel with the internal 10kΩ resistor. The tradeoff for using this resistor is an increase in quiescent current. In the most cases, choosing a small value of Ci in the range of 0.33μF to 1μF, Cb being equal to 4.7μF and an external 1kΩ resistor should be placed in parallel with the internal 10kΩ resistor should produce a virtually clickless and popless turn-on.

A high gain amplifier intensifies the problem as the small delta in voltage is multiplied by the gain. So it is advantageous to use low-gain configurations.

Shutdown Function

In order to reduce power consumption while not in use, the APA2065 contains a shutdown pin to externally turn off the amplifier bias circuitry. This shutdown feature turns the amplifier off when a logic low is placed on the $\overline{\text{SHUTDOWN}}$ pin. The trigger point between a logic high and logic low level is typically 2.0V. It is best to switch between ground and the supply V_{DD} to provide maximum device performance.

By switching the $\overline{\text{SHUTDOWN}}$ pin to low, the amplifier enters a low-current state, I_{DD}<50μA. On normal operating, $\overline{\text{SHUTDOWN}}$ pin pull to high level to keeping the IC out of the shutdown mode. The $\overline{\text{SHUTDOWN}}$ pin should be tied to a definite voltage to avoid unwanted state changes.

Clock Generator

APA2065 integrates a clock block 130kHz to avoid volume control function abnormal when VOLUME control signal with spike or noise. APA2065 changes each step of volume gain after four clock cycles to make sure control signal ready.

BTL Amplifier Efficiency

An easy-to-use equation to calculate efficiency starts out as being equal to the ratio of power from the power supply to the power delivered to the load.

The following equations are the basis for calculating amplifier efficiency.

$$\text{Efficiency} = \frac{P_O}{P_{SUP}} \quad (9)$$

Where :

$$P_O = \frac{V_{ORMS} \times V_{ORMS}}{RL} = \frac{V_P \times V_P}{2RL}$$

$$V_{ORMS} = \frac{V_P}{\sqrt{2}} \quad (10)$$

$$P_{SUP} = V_{DD} \times I_{DDAVG} = V_{DD} \times \frac{2V_P}{\pi R_L} \quad (11)$$

Efficiency of a BTL configuration :

$$\frac{P_O}{P_{SUP}} = \left(\frac{V_P \times V_P}{2R_L}\right) / \left(V_{DD} \times \frac{2V_P}{\pi R_L}\right) = \frac{\pi V_P}{4V_{DD}} \quad (12)$$

Note that the efficiency of the amplifier is quite low for lower power levels and rises sharply as power to the load is increased resulting in a nearly flat internal power dissipation over the normal operating range. Note that the internal dissipation at full output power is less than in the half power range. Calculating the efficiency for a specific system is the key to proper power supply design. For a stereo 1W audio system with 8Ω loads and a 5V supply, the maximum draw on the power supply is almost 3W.

A final point to remember about linear amplifiers (either SE or BTL) is how to manipulate the terms in the efficiency equation to utmost advantage when possible. Note that in equation, V_{DD} is in the

Application Descriptions (Cont.)

BTL Amplifier Efficiency (Cont.)

denominator. This indicates that as V_{DD} goes down, efficiency goes up. In other words, use the efficiency analysis to choose the correct supply voltage and speaker impedance for the application.

Po (W)	Efficiency (%)	I_{DD}(A)	V_{PP}(V)	P_D (W)
0.25	31.25	0.16	2.00	0.55
0.50	47.62	0.21	2.83	0.55
1.00	66.67	0.30	4.00	0.5
1.25	78.13	0.32	4.47	0.35

**High peak voltages cause the THD to increase.

Table 1. Efficiency Vs Output Power in 5-V/8Ω BTL Systems

Power Dissipation

Whether the power amplifier is operated in BTL or SE modes, power dissipation is a major concern. In equation13 states the maximum power dissipation point for a SE mode operating at a given supply voltage and driving a specified load.

$$\text{SE mode : } P_{D,MAX}=\frac{V_{DD}^2}{2\pi^2 R_L} \quad (13)$$

In BTL mode operation, the output voltage swing is doubled as in SE mode. Thus the maximum power dissipation point for a BTL mode operating at the same given conditions is 4 times as in SE mode.

$$\text{BTL mode : } P_{D,MAX}=\frac{4V_{DD}^2}{2\pi^2 R_L} \quad (14)$$

Since the APA2065 is a dual channel power amplifier, the maximum internal power dissipation is 2 times that both of equations depending on the mode of operation. Even with this substantial increase in power dissipation, the APA2065 does not require extra heatsink. The power dissipation from equation14, assuming a 5V-power supply and an 8Ω load, must not be greater than the power dissipation that results from the equation15:

$$P_{D,MAX}=\frac{T_{J,MAX}-T_A}{\theta_{JA}} \quad (15)$$

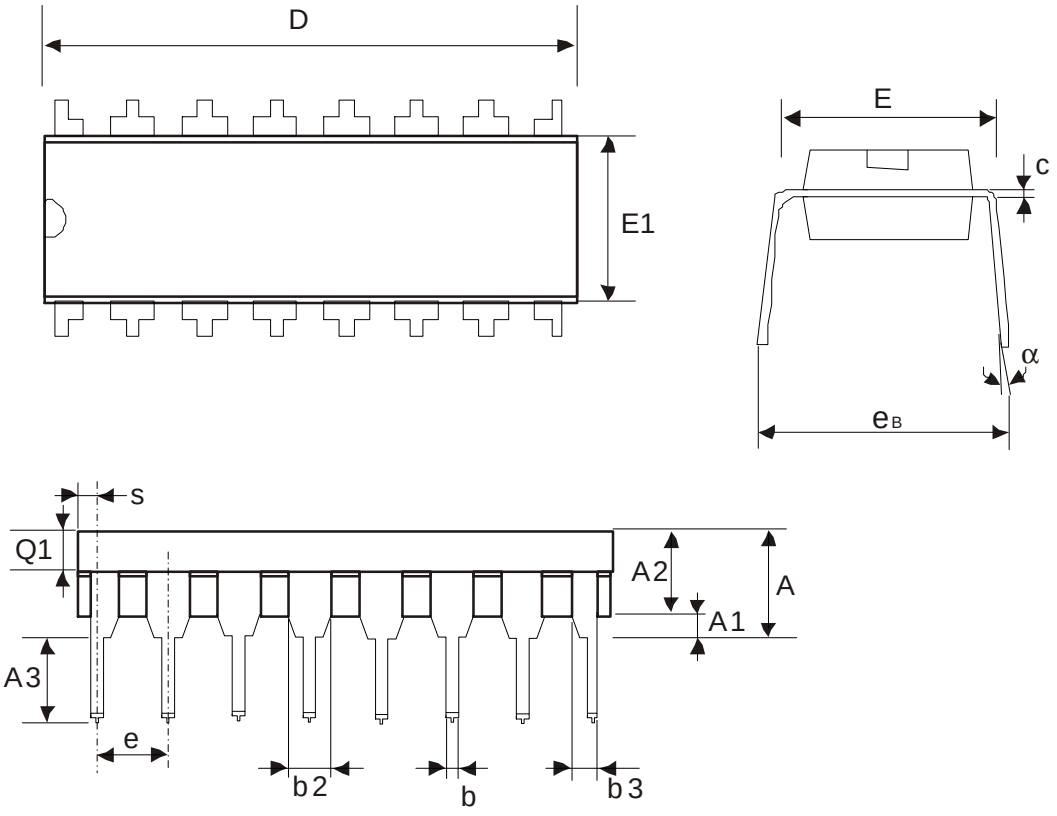
For DIP-16 package with thermal pad, the thermal resistance (θ_{JA}) is equal to 45°C/W.

Since the maximum junction temperature ($T_{J,MAX}$) of APA2065 is 150°C and the ambient temperature (T_A) is defined by the power system design, the maximum power dissipation which the IC package is able to handle can be obtained from equation15.

Once the power dissipation is greater than the maximum limit ($P_{D,MAX}$), either the supply voltage (V_{DD}) must be decreased, the load impedance (R_L) must be increased or the ambient temperature should be reduced.

Packaging Information

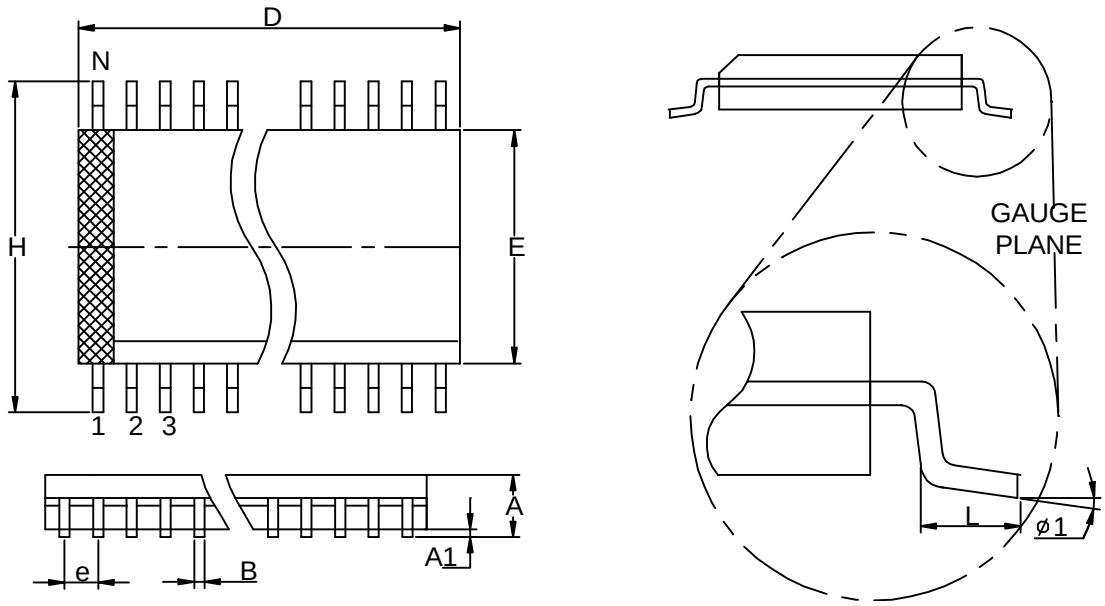
PDIP-16 pin (Reference JEDEC Registration MS-001)



Dim	Millimeters		Inches	
	Min.	Max.	Min.	Max.
A	-	5.32	-	0.210
A1	0.38	-	0.015	-
A2	3.17	3.42	0.125	0.135
A3	2.92	3.80	0.115	0.150
b	0.36	0.56	0.014	0.022
b2	1.14	1.78	0.045	0.070
b3	0.76	1.14	0.030	0.045
c	0.20	0.36	0.008	0.014
D	18.632	19.646	0.735	0.775
E	7.605BSC		0.300BSC	
E1	6.223	6.477	0.245	0.255
e	2.54BSC		0.100BSC	
e_B	8.492	9.506	0.335	0.375
Q1	1.397	1.651	0.055	0.065
s	0.58	0.84	0.023	0.033
α	3°	8°	3°	8°

Package Information

SO – 300mil (Reference JEDEC Registration MS-013)

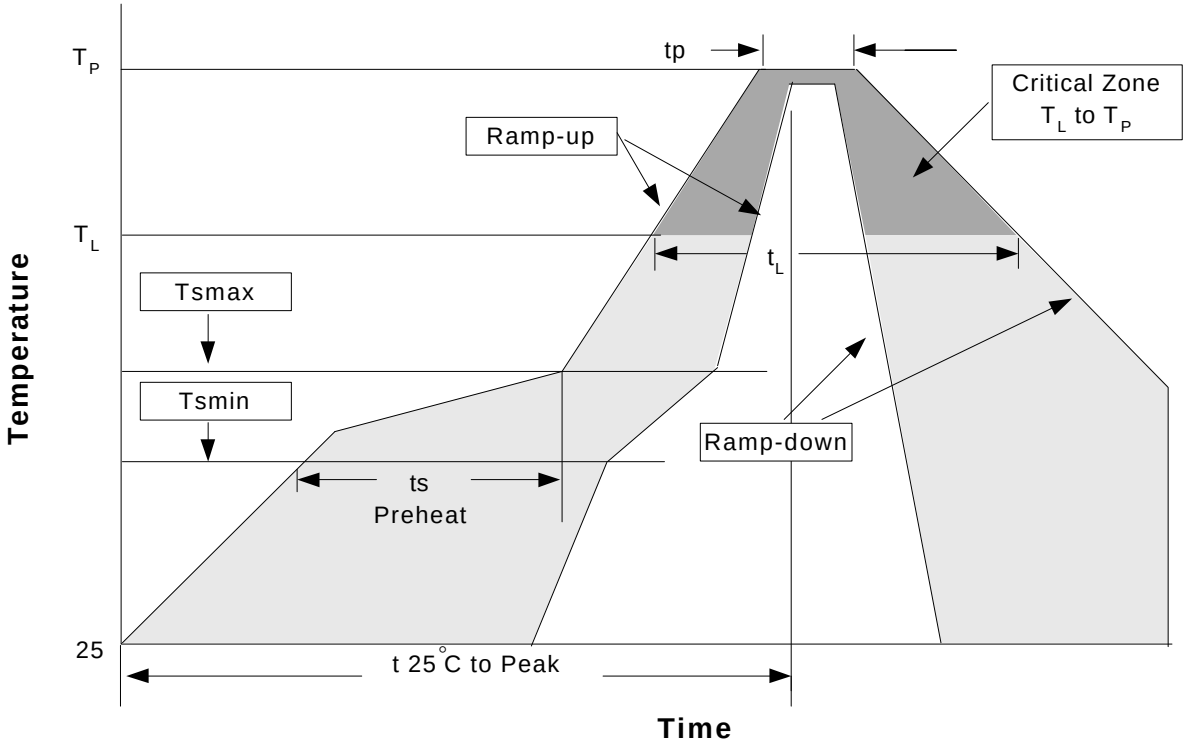


Dim	Millimeters		Variations- D			Dim	Inches		Variations- D		
	Min.	Max.	Variations	Min.	Max.		Min.	Max.	Variations	Min.	Max.
A	2.35	2.65	SO-16	10.10	10.50	A	0.093	0.1043	SO-16	0.398	0.413
A1	0.10	0.30	SO-18	11.35	11.76	A1	0.004	0.0120	SO-18	0.447	0.463
B	0.33	0.51	SO-20	12.60	13	B	0.013	0.020	SO-20	0.496	0.512
D	See variations		SO-24	15.20	15.60	D	See variations		SO-24	0.599	0.614
E	7.40	7.60	SO-28	17.70	18.11	E	0.2914	0.2992	SO-28	0.697	0.713
e	1.27BSC		SO-14	8.80	9.20	e	0.050BSC		SO-14	0.347	0.362
H	10	10.65				H	0.394	0.419			
L	0.40	1.27				L	0.016	0.050			
N	See variations					N	See variations				
ϕ 1	0°	8°				ϕ 1	0°	8°			

Physical Specifications

Terminal Material	Solder-Plated Copper (Solder Material : 90/10 or 63/37 SnPb), 100%Sn
Lead Solderability	Meets EIA Specification RSI86-91, ANSI/J-STD-002 Category 3.

Reflow Condition (IR/Convection or VPR Reflow)



Classificatin Reflow Profiles

Profile Feature	Sn-Pb Eutectic Assembly	Pb-Free Assembly
Average ramp-up rate (T_L to T_P)	3°C/second max.	3°C/second max.
Preheat - Temperature Min (Tsmin) - Temperature Max (Tsmax) - Time (min to max) (ts)	100°C 150°C 60-120 seconds	150°C 200°C 60-180 seconds
Time maintained above: - Temperature (T_L) - Time (t_L)	183°C 60-150 seconds	217°C 60-150 seconds
Peak/Classificatioon Temperature (Tp)	See table 1	See table 2
Time within 5°C of actual Peak Temperature (tp)	10-30 seconds	20-40 seconds
Ramp-down Rate	6°C/second max.	6°C/second max.
Time 25°C to Peak Temperature	6 minutes max.	8 minutes max.

Notes: All temperatures refer to topside of the package .Measured on the body surface.

Classificatin Reflow Profiles(Cont.)

Table 1. SnPb Entectic Process – Package Peak Reflow Temperatures

Package Thickness	Volume mm^3 <350	Volume mm^3 ³350
<2.5 mm	240 +0/-5°C	225 +0/-5°C
≥2.5 mm	225 +0/-5°C	225 +0/-5°C

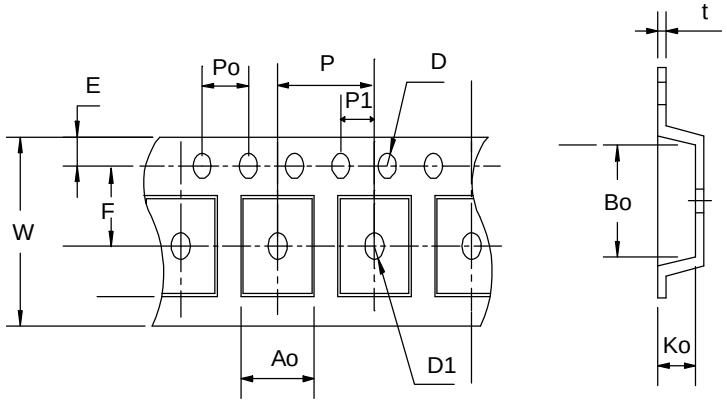
Table 2. Pb-free Process – Package Classification Reflow Temperatures

Package Thickness	Volume mm^3 <350	Volume mm^3 350-2000	Volume mm^3 >2000
<1.6 mm	260 +0°C*	260 +0°C*	260 +0°C*
1.6 mm – 2.5 mm	260 +0°C*	250 +0°C*	245 +0°C*
≥2.5 mm	250 +0°C*	245 +0°C*	245 +0°C*
*Tolerance: The device manufacturer/supplier **shall** assure process compatibility up to and including the stated classification temperature (this means Peak reflow temperature +0°C. For example 260°C+0°C) at the rated MSL level.			

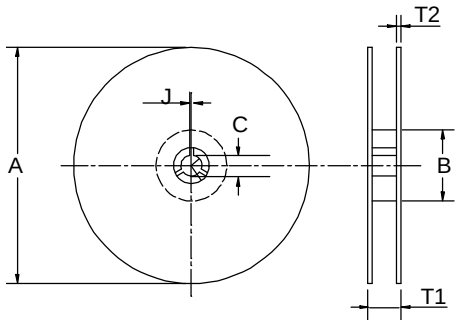
Reliability Test Program

Test item	Method	Description
SOLDERABILITY	MIL-STD-883D-2003	245°C, 5 SEC
HOLT	MIL-STD-883D-1005.7	1000 Hrs Bias @125°C
PCT	JESD-22-B,A102	168 Hrs, 100%RH, 121°C
TST	MIL-STD-883D-1011.9	-65°C~150°C, 200 Cycles
ESD	MIL-STD-883D-3015.7	VHBM > 2KV, VMM > 200V
Latch-Up	JESD 78	10ms, 1_{tr} > 100mA

Carrier Tape & Reel Dimensions



Carrier Tape & Reel Dimensions(Cont.)



Application	A	B	C	J	T1	T2	W	P	E
SOP- 16	330 ± 1	100 +2	13+ 0.5	2 ± 0.5	16.4 +0.3 -0.2	2.5 ± 0.5	16± 0.2	12± 0.1	1.75±0.1
	F	D	D1	Po	P1	Ao	Bo	Ko	t
	7.5± 0.1	1.5 +0.1	1.5+ 0.25	4.0 ± 0.1	2.0 ± 0.1	10.9 ± 0.1	10.8± 0. 1	3.0± 0.1	0.3±0.013

(mm)

Cover Tape Dimensions

Application	Carrier Width	Cover Tape Width	Devices Per Reel
SOP- 16	24	21.3	1000

Customer Service

Anpec Electronics Corp.

Head Office :

5F, No. 2 Li-Hsin Road, SBIP,

Hsin-Chu, Taiwan, R.O.C.

Tel : 886-3-5642000

Fax : 886-3-5642050

Taipei Branch :

7F, No. 137, Lane 235, Pac Chiao Rd.,

Hsin Tien City, Taipei Hsien, Taiwan, R. O. C.

Tel : 886-2-89191368

Fax : 886-2-89191369