

## 16-Mbit (1M x 16 / 2M x 8) Static RAM

### Features

- Configurable as 1M x 16 or as 2M x 8 SRAM
- Very high speed: 45 ns
- Wide voltage range: 4.5V–5.5V
- Ultra low standby power
  - Typical standby current: 1.5  $\mu$ A
  - Maximum standby current: 12  $\mu$ A
- Ultra low active power
  - Typical active current: 2.2 mA @ f = 1 MHz
- Easy memory expansion with  $\overline{CE}_1$ ,  $CE_2$ , and  $\overline{OE}$  features
- Automatic power down when deselected
- CMOS for optimum speed and power
- Offered in 48-pin TSOP I package

### Functional Description<sup>[1]</sup>

The CY62167E is a high performance CMOS static RAM organized as 1M words by 16 bits/2M words by 8 bits. This device features advanced circuit design to provide an ultra low active current. This is ideal for providing More Battery Life™ (MoBL®) in portable applications such as cellular telephones. The device also has an automatic power down feature that reduces power consumption by 99% when addresses are not toggling. Place the device into standby mode when deselected

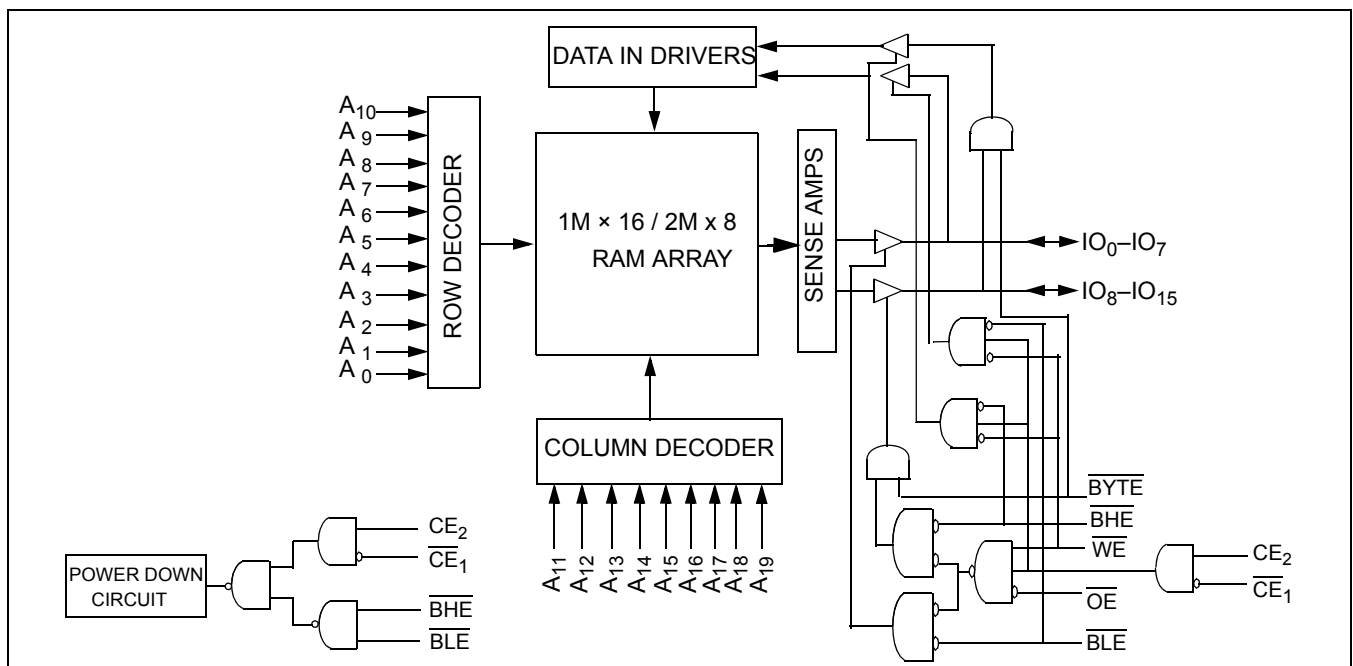
( $\overline{CE}_1$  HIGH, or  $CE_2$  LOW, or both  $\overline{BHE}$  and  $\overline{BLE}$  are HIGH). The input and output pins (IO<sub>0</sub> through IO<sub>15</sub>) are placed in a high impedance state when:

- The device is deselected ( $\overline{CE}_1$  HIGH or  $CE_2$  LOW)
- Outputs are disabled ( $\overline{OE}$  HIGH)
- Both Byte High Enable and Byte Low Enable are disabled ( $\overline{BHE}$ ,  $\overline{BLE}$  HIGH) or
- A write operation is in progress ( $\overline{CE}_1$  LOW,  $CE_2$  HIGH, and  $\overline{WE}$  LOW)

To write to the device, take Chip Enables ( $\overline{CE}_1$  LOW and  $CE_2$  HIGH) and Write Enable ( $\overline{WE}$ ) input LOW. If Byte Low Enable ( $\overline{BLE}$ ) is LOW, then data from IO pins (IO<sub>0</sub> through IO<sub>7</sub>), is written into the location specified on the address pins (A<sub>0</sub> through A<sub>19</sub>). If Byte High Enable ( $\overline{BHE}$ ) is LOW, then data from the IO pins (IO<sub>8</sub> through IO<sub>15</sub>) is written into the location specified on the address pins (A<sub>0</sub> through A<sub>19</sub>).

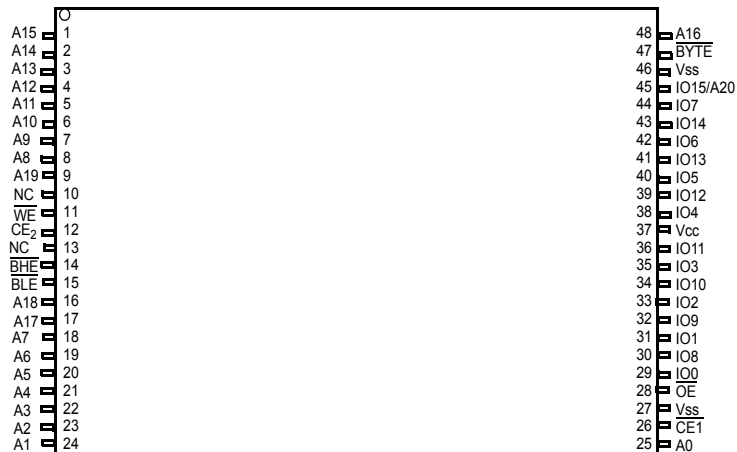
To read from the device, take Chip Enables ( $\overline{CE}_1$  LOW and  $CE_2$  HIGH) and Output Enable ( $\overline{OE}$ ) LOW while forcing the Write Enable ( $\overline{WE}$ ) HIGH. If Byte Low Enable ( $\overline{BLE}$ ) is LOW, then data from the memory location specified by the address pins appears on IO<sub>0</sub> to IO<sub>7</sub>. If Byte High Enable ( $\overline{BHE}$ ) is LOW, then data from memory appears on IO<sub>8</sub> to IO<sub>15</sub>. See the “Truth Table” on page 10 for a complete description of read and write modes.

### Logic Block Diagram



#### Note

1. For best practice recommendations, refer to the Cypress application note AN1064, SRAM System Guidelines.

**Pin Configuration<sup>[2, 3]</sup>**
**48-Pin TSOP I Top View**

**Product Portfolio**

Product	V <sub>CC</sub> Range (V)			Speed (ns)	Power Dissipation					
					Operating I <sub>CC</sub> (mA)				Standby I <sub>SB2</sub> (μA)	
					f = 1 MHz		f = f <sub>max</sub>			
Min	Typ <sup>[4]</sup>	Max	Typ <sup>[4]</sup>	Max	Typ <sup>[4]</sup>	Max	Typ <sup>[4]</sup>	Max		
CY62167ELL	4.5	5.0	5.5	45	2.2	4.0	25	30	1.5	12

**Notes**

- NC pins are not connected on the die.
- The BYTE pin in the 48-TSOP I package must be tied to V<sub>CC</sub> to use the device as a 1M X 16 SRAM. The 48-TSOP I package can also be used as a 2M X 8 SRAM by tying the BYTE signal to V<sub>SS</sub>. In the 2M x 8 configuration, pin 45 is A20, while BHE, BLE and IO<sub>8</sub> to IO<sub>14</sub> pins are not used.
- Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at V<sub>CC</sub> = V<sub>CC</sub>(typ), T<sub>A</sub> = 25°C.

**Maximum Ratings**

Exceeding the maximum ratings may shorten the battery life of the device. User guidelines are not tested.

Storage Temperature ..... -65°C to + 150°C

Ambient Temperature with Power Applied ..... -55°C to + 125°C

Supply Voltage to Ground Potential ..... -0.5V to 6.0V

DC Voltage Applied to Outputs in High-Z State<sup>[5, 6]</sup> ..... -0.5V to 6.0V

DC Input Voltage<sup>[5, 6]</sup> ..... -0.5V to 6.0V

Output Current into Outputs (LOW) ..... 20 mA

Static Discharge Voltage ..... >2001V (MIL-STD-883, Method 3015)

Latch Up Current ..... >200 mA

**Operating Range**

Device	Range	Ambient Temperature	V <sub>CC</sub> <sup>[7]</sup>
CY62167ELL	Industrial	-40°C to +85°C	4.5V to 5.5V

**Electrical Characteristics**

Over the Operating Range

Parameter	Description	Test Conditions	45 ns			Unit
			Min	Typ <sup>[4]</sup>	Max	
V <sub>OH</sub>	Output HIGH Voltage	I <sub>OH</sub> = -1.0 mA	2.4			V
V <sub>OL</sub>	Output LOW Voltage	I <sub>OL</sub> = 2.1mA			0.4	V
V <sub>IH</sub>	Input HIGH Voltage	V <sub>CC</sub> = 4.5V to 5.5V	2.2		V <sub>CC</sub> + 0.5V	V
V <sub>IL</sub>	Input LOW Voltage	V <sub>CC</sub> = 4.5V to 5.5V	-0.5		0.7 <sup>[8]</sup>	V
I <sub>Ix</sub>	Input Leakage Current	GND ≤ V <sub>I</sub> ≤ V <sub>CC</sub>	-1		+1	μA
I <sub>OZ</sub>	Output Leakage Current	GND ≤ V <sub>O</sub> ≤ V <sub>CC</sub> , Output Disabled	-1		+1	μA
I <sub>CC</sub>	V <sub>CC</sub> Operating Supply Current	f = f <sub>MAX</sub> = 1/t <sub>RC</sub>		25	30	mA
		f = 1 MHz		2.2	4.0	
I <sub>SB2</sub> <sup>[9]</sup>	Automatic CE Power Down Current—CMOS Inputs	$\overline{CE}_1 \geq V_{CC} - 0.2V$ or $CE_2 \leq 0.2V$ , $V_{IN} \geq V_{CC} - 0.2V$ or $V_{IN} \leq 0.2V$ , f = 0, V <sub>CC</sub> = V <sub>CC(max)</sub>		1.5	12	μA

**Capacitance<sup>[10]</sup>**

Parameter	Description	Test Conditions	Max	Unit
C <sub>IN</sub>	Input Capacitance	T <sub>A</sub> = 25°C, f = 1 MHz, V <sub>CC</sub> = V <sub>CC(typ)</sub>	10	pF
C <sub>OUT</sub>	Output Capacitance		10	pF

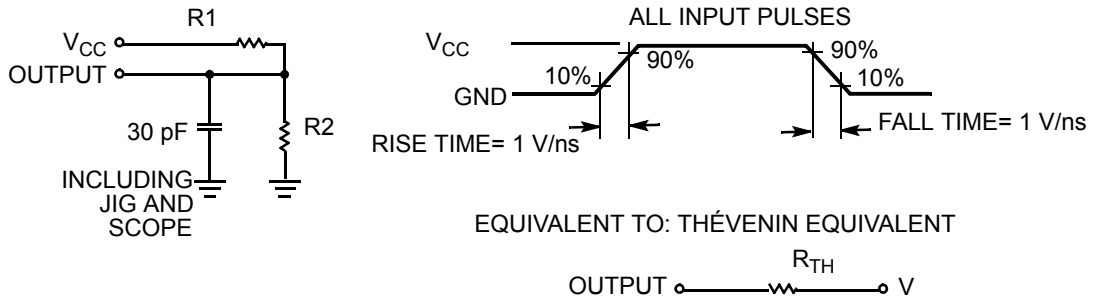
**Thermal Resistance<sup>[10]</sup>**

Parameter	Description	Test Conditions	TSOP I	Unit
Θ <sub>JA</sub>	Thermal Resistance (junction to ambient)	Still air, soldered on a 3 × 4.5 inch, two-layer printed circuit board	60	°C/W
Θ <sub>JC</sub>	Thermal Resistance (junction to case)		4.3	°C/W

**Notes**

- V<sub>IL</sub>(min) = -2.0V for pulse durations less than 20 ns.
- V<sub>IH</sub>(max) = V<sub>CC</sub> + 0.75V for pulse durations less than 20 ns.
- Full Device AC operation is based on a 100 μs ramp time from 0 to V<sub>CC</sub> (min) and 200 μs wait time after V<sub>CC</sub> stabilization.
- Under DC conditions the device meets a V<sub>IL</sub> of 0.8V. However, in dynamic conditions Input LOW Voltage applied to the device must not be higher than 0.7V.
- Only chip enables ( $\overline{CE}_1$  and CE<sub>2</sub>), byte enables ( $\overline{BHE}$  and BLE) and  $\overline{BYTE}$  need to be tied to CMOS levels to meet the I<sub>SB2</sub> / I<sub>CCDR</sub> spec. Other inputs can be left floating.
- Tested initially and after any design or process changes that may affect these parameters.

**AC Test Loads and Waveforms**



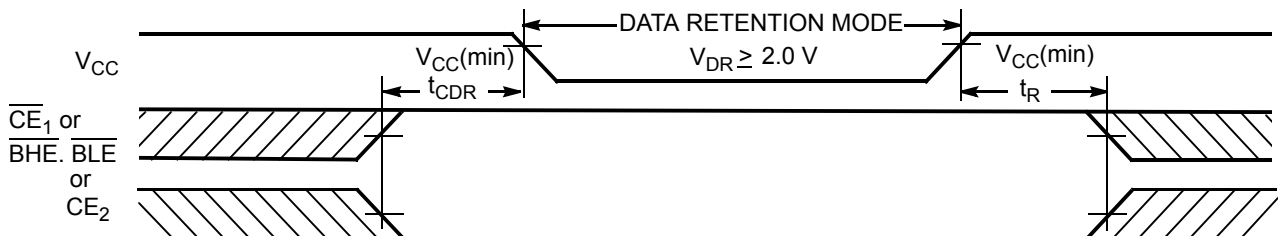
Parameters	Values	Unit
R1	1800	Ω
R2	990	Ω
R <sub>TH</sub>	639	Ω
V <sub>TH</sub>	1.77	V

**Data Retention Characteristics**

Over the Operating Range

Parameter	Description	Conditions	Min	Typ <sup>[4]</sup>	Max	Unit
V <sub>DR</sub>	V <sub>CC</sub> for Data Retention		2.0			V
I <sub>CCDR</sub> <sup>[9]</sup>	Data Retention Current	V <sub>CC</sub> = V <sub>DR</sub> CE <sub>1</sub> ≥ V <sub>CC</sub> - 0.2V, CE <sub>2</sub> ≤ 0.2V, V <sub>IN</sub> ≥ V <sub>CC</sub> - 0.2V or V <sub>IN</sub> ≤ 0.2V			12	μA
t <sub>CDR</sub> <sup>[10]</sup>	Chip Deselect to Data Retention Time		0			ns
t <sub>R</sub> <sup>[11]</sup>	Operation Recovery Time		t <sub>RC</sub>			ns

**Data Retention Waveform<sup>[12]</sup>**



**Notes**

11. Full device operation requires linear V<sub>CC</sub> ramp from V<sub>DR</sub> to V<sub>CC</sub>(min) ≥ 100 μs or stable at V<sub>CC</sub>(min) ≥ 100 μs.

12. BHE, BLE is the AND of BHE and BLE. Deselect the chip by either disabling the chip enable signals or by disabling BHE and BLE.

## Switching Characteristics

 Over the Operating Range<sup>[13, 14]</sup>

Parameter	Description	45 ns		Unit
		Min	Max	
<b>READ CYCLE</b>				
$t_{RC}$	Read Cycle Time	45		ns
$t_{AA}$	Address to Data Valid		45	ns
$t_{OHA}$	Data Hold from Address Change	10		ns
$t_{ACE}$	$\overline{CE}_1$ LOW and $CE_2$ HIGH to Data Valid		45	ns
$t_{DOE}$	$\overline{OE}$ LOW to Data Valid		22	ns
$t_{LZOE}$	$\overline{OE}$ LOW to Low-Z <sup>[15]</sup>	5		ns
$t_{HZOE}$	$\overline{OE}$ HIGH to High-Z <sup>[15, 16]</sup>		18	ns
$t_{LZCE}$	$\overline{CE}_1$ LOW and $CE_2$ HIGH to Low-Z <sup>[15]</sup>	10		ns
$t_{HZCE}$	$\overline{CE}_1$ HIGH and $CE_2$ LOW to High-Z <sup>[15, 16]</sup>		18	ns
$t_{PU}$	$\overline{CE}_1$ LOW and $CE_2$ HIGH to Power Up	0		ns
$t_{PD}$	$\overline{CE}_1$ HIGH and $CE_2$ LOW to Power Down		45	ns
$t_{DBE}$	BLE/BHE LOW to Data Valid		45	ns
$t_{LZBE}$	$\overline{BLE}/\overline{BHE}$ LOW to Low-Z <sup>[15]</sup>	10		ns
$t_{HZBE}$	$\overline{BLE}/\overline{BHE}$ HIGH to High-Z <sup>[15, 16]</sup>		18	ns
<b>WRITE CYCLE<sup>[17]</sup></b>				
$t_{WC}$	Write Cycle Time	45		ns
$t_{SCE}$	$\overline{CE}_1$ LOW and $CE_2$ HIGH to Write End	35		ns
$t_{AW}$	Address Setup to Write End	35		ns
$t_{HA}$	Address Hold from Write End	0		ns
$t_{SA}$	Address Setup to Write Start	0		ns
$t_{PWE}$	$\overline{WE}$ Pulse Width	35		ns
$t_{BW}$	$\overline{BLE}/\overline{BHE}$ LOW to Write End	35		ns
$t_{SD}$	Data Setup to Write End	25		ns
$t_{HD}$	Data Hold from Write End	0		ns
$t_{HZWE}$	$\overline{WE}$ LOW to High-Z <sup>[15, 16]</sup>		18	ns
$t_{LZWE}$	$\overline{WE}$ HIGH to Low-Z <sup>[15]</sup>	10		ns

### Notes

13. Test conditions for all parameters other than tri-state parameters assume signal transition time of 1 V/ns, timing reference levels of  $V_{CC}(typ)/2$ , input pulse levels of 0 to  $V_{CC}(typ)$ , and output loading of the specified  $I_{OL}/I_{OH}$  as shown in "AC Test Loads and Waveforms" on page 4.
14. AC timing parameters are subject to byte enable signals (BHE or BLE) not switching when chip is disabled. See application note AN13842 for further clarification.
15. At any temperature and voltage condition,  $t_{HZCE}$  is less than  $t_{LZCE}$ ,  $t_{HZBE}$  is less than  $t_{LZBE}$ ,  $t_{HZOE}$  is less than  $t_{LZOE}$ , and  $t_{HZWE}$  is less than  $t_{LZWE}$  for any device.
16.  $t_{HZOE}$ ,  $t_{HZCE}$ ,  $t_{HZBE}$ , and  $t_{HZWE}$  transitions are measured when the outputs enter a high impedance state.
17. The internal write time of the memory is defined by the overlap of  $\overline{WE}$ ,  $\overline{CE}_1 = V_{IL}$ , BHE or BLE or both =  $V_{IL}$ , and  $CE_2 = V_{IH}$ . All signals must be active to initiate a write and any of these signals can terminate a write by going inactive. The data input setup and hold timing should be referenced to the edge of the signal that terminates the write.

### Switching Waveforms

Figure 1 shows address transition controlled read cycle waveforms.<sup>[18, 19]</sup>

Figure 1. Read Cycle No. 1

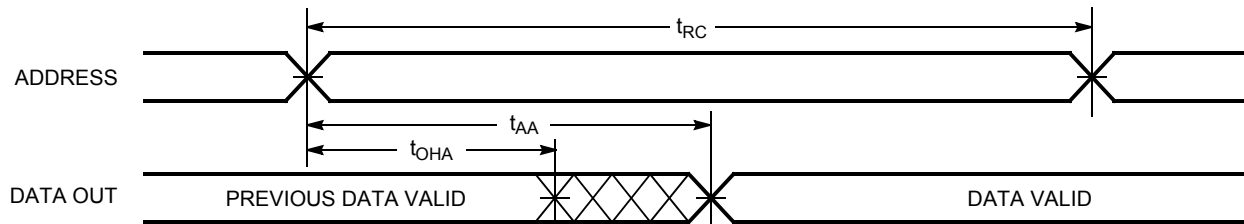
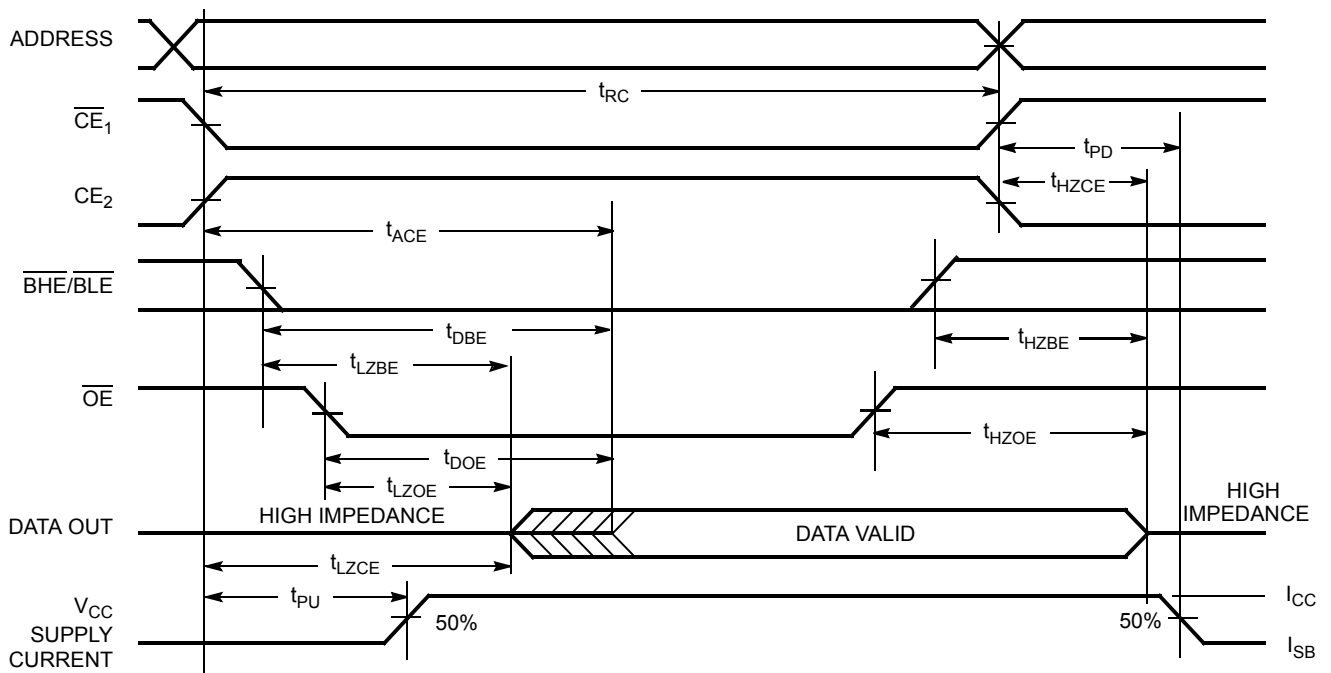


Figure 2 shows  $\overline{OE}$  controlled read cycle waveforms.<sup>[19, 20]</sup>

Figure 2. Read Cycle No. 2



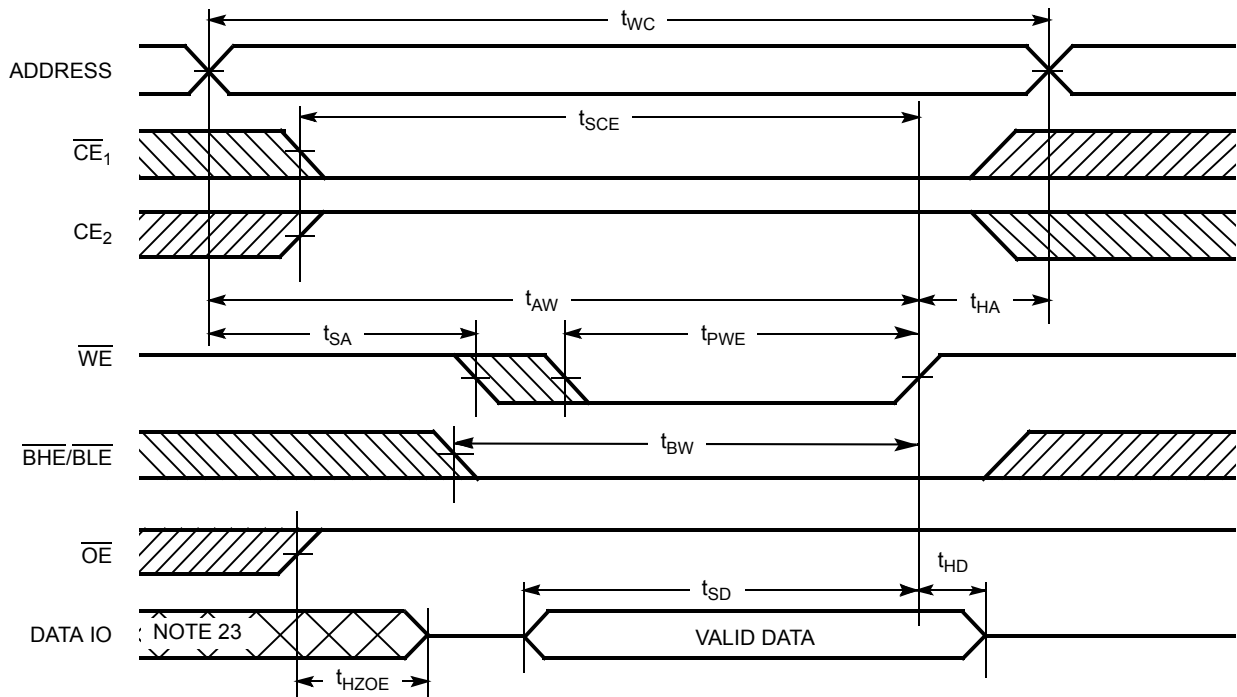
**Notes**

- 18. The device is continuously selected.  $\overline{OE}$ ,  $\overline{CE}_1 = V_{IL}$ ,  $\overline{BHE}$ ,  $\overline{BLE}$  or both =  $V_{IL}$ , and  $CE_2 = V_{IH}$ .
- 19.  $\overline{WE}$  is HIGH for read cycle.
- 20. Address valid before or similar to  $\overline{CE}_1$ ,  $\overline{BHE}$ ,  $\overline{BLE}$  transition LOW and  $CE_2$  transition HIGH.

Switching Waveforms (continued)

Figure 3 shows  $\overline{WE}$  controlled write cycle waveforms. [17, 21, 22]

Figure 3. Write Cycle No. 1



Notes

- 21. Data IO is high impedance if  $\overline{OE} = V_{IH}$ .
- 22. If  $\overline{CE}_1$  goes HIGH and  $CE_2$  goes LOW simultaneously with  $\overline{WE} = V_{IH}$ , the output remains in a high impedance state.
- 23. During this period the IOs are in output state and input signals must not be applied.

Switching Waveforms (continued)

Figure 4 shows  $\overline{CE}_1$  or  $CE_2$  controlled write cycle waveforms.<sup>[17, 21, 22]</sup>

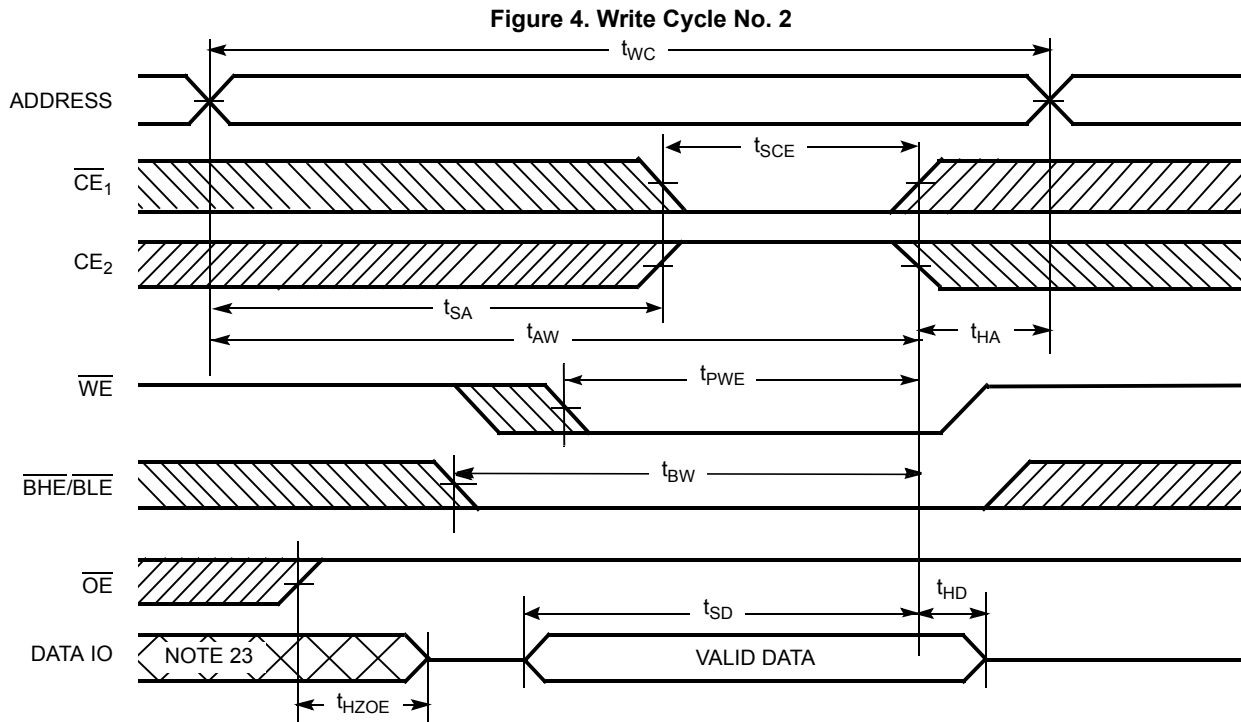
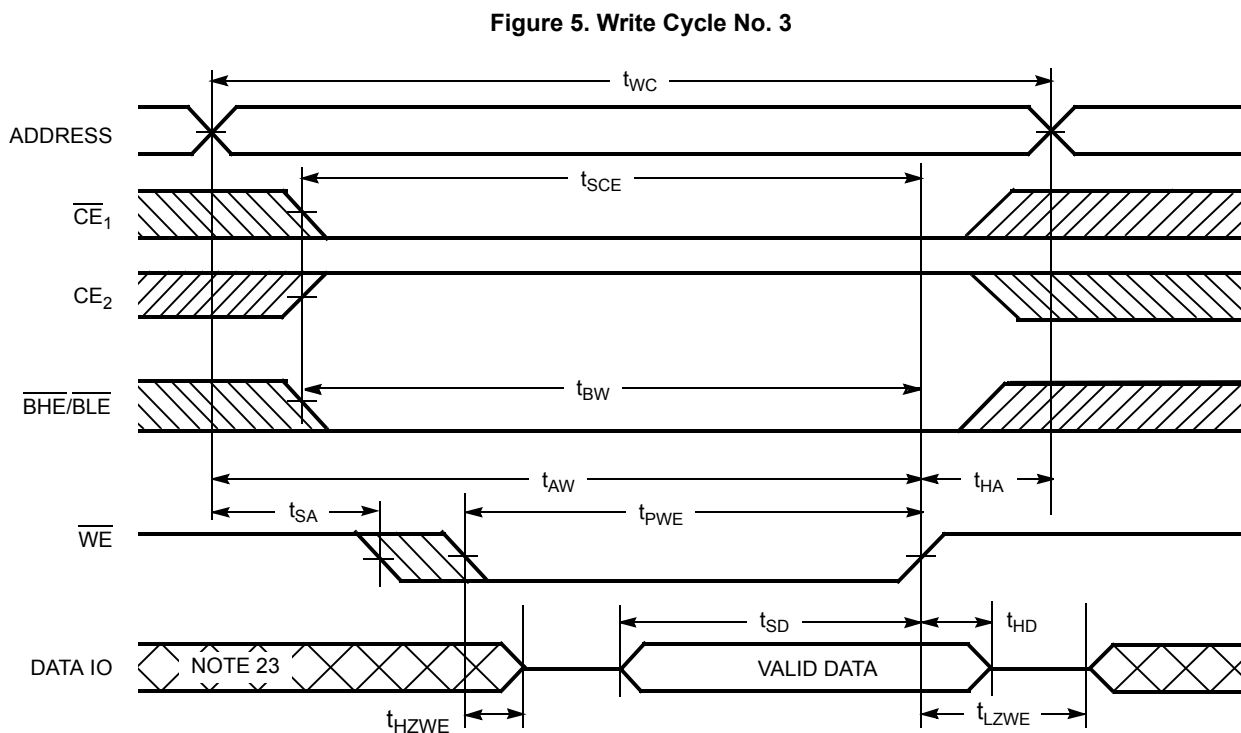


Figure 5 shows  $\overline{WE}$  controlled,  $\overline{OE}$  LOW write cycle waveforms.<sup>[22]</sup>

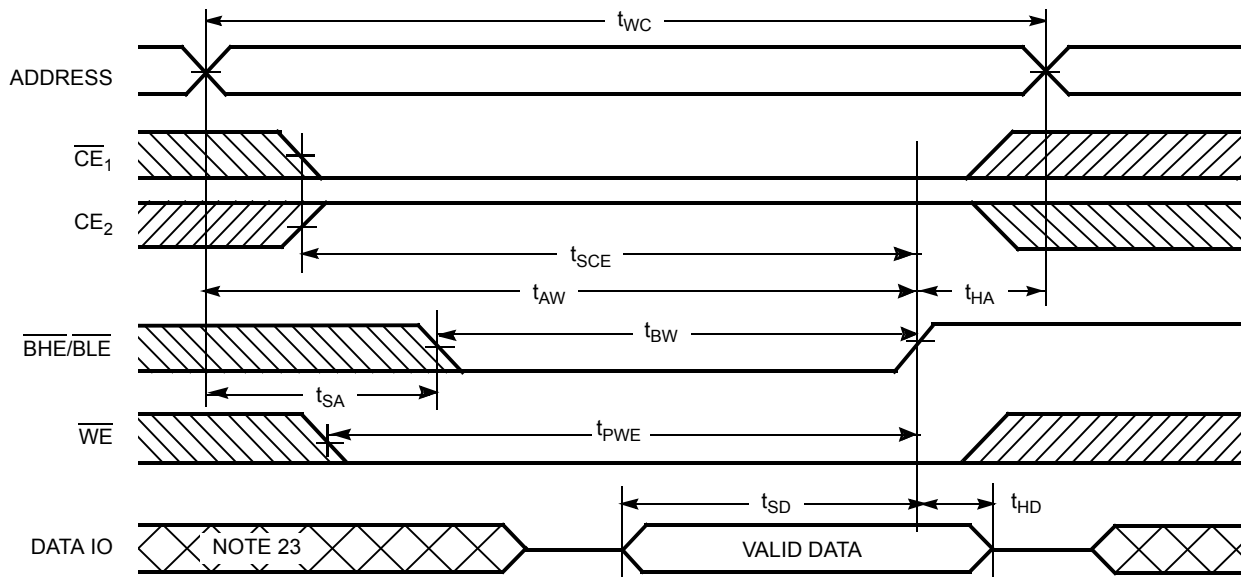




Switching Waveforms (continued)

Figure 6 shows  $\overline{\text{BHE}}/\overline{\text{BLE}}$  controlled,  $\overline{\text{OE}}$  LOW write cycle waveforms.<sup>[22]</sup>

Figure 6. Write Cycle No. 4



**Truth Table**

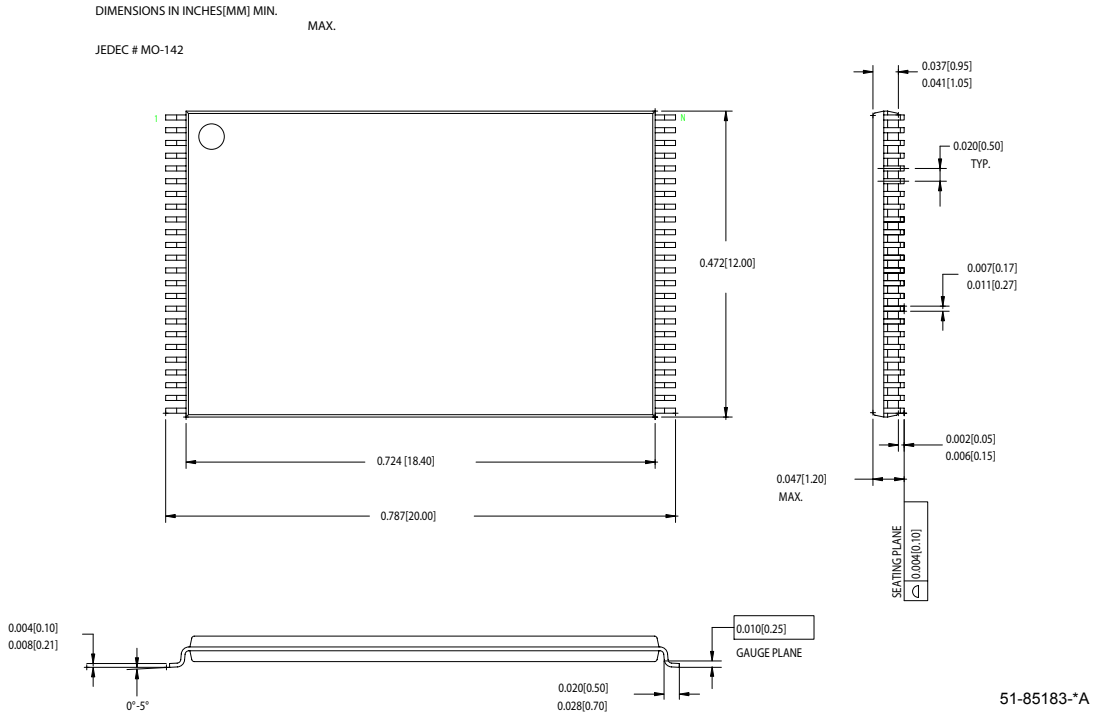
$\overline{CE}_1$	$\overline{CE}_2$	$\overline{WE}$	$\overline{OE}$	$\overline{BHE}$	$\overline{BLE}$	Inputs Outputs	Mode	Power
H	X	X	X	X	X	High-Z	Deselect/Power Down	Standby ( $I_{SB}$ )
X	L	X	X	X	X	High-Z	Deselect/Power Down	Standby ( $I_{SB}$ )
X	X	X	X	H	H	High-Z	Deselect/Power Down	Standby ( $I_{SB}$ )
L	H	H	L	L	L	Data Out ( $IO_0$ – $IO_{15}$ )	Read	Active ( $I_{CC}$ )
L	H	H	L	H	L	Data Out ( $IO_0$ – $IO_7$ ); High-Z ( $IO_8$ – $IO_{15}$ )	Read	Active ( $I_{CC}$ )
L	H	H	L	L	H	High-Z ( $IO_0$ – $IO_7$ ); Data Out ( $IO_8$ – $IO_{15}$ )	Read	Active ( $I_{CC}$ )
L	H	H	H	L	H	High-Z	Output Disabled	Active ( $I_{CC}$ )
L	H	H	H	H	L	High-Z	Output Disabled	Active ( $I_{CC}$ )
L	H	H	H	L	L	High-Z	Output Disabled	Active ( $I_{CC}$ )
L	H	L	X	L	L	Data In ( $IO_0$ – $IO_{15}$ )	Write	Active ( $I_{CC}$ )
L	H	L	X	H	L	Data In ( $IO_0$ – $IO_7$ ); High-Z ( $IO_8$ – $IO_{15}$ )	Write	Active ( $I_{CC}$ )
L	H	L	X	L	H	High-Z ( $IO_0$ – $IO_7$ ); Data In ( $IO_8$ – $IO_{15}$ )	Write	Active ( $I_{CC}$ )

**Ordering Information**

Speed (ns)	Ordering Code	Package Diagram	Package Type	Operating Range
45	CY62167ELL-45ZXI	51-85183	48-pin TSOP I (Pb-free)	Industrial

**Package Diagram**

**Figure 7. 48-Pin TSOP I (12 mm x 18.4 mm x 1.0 mm), 51-85183**



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**Document History Page**

Document Title: CY62167E MoBL <sup>®</sup> 16-Mbit (1M x 16 / 2M x 8) Static RAM Document Number: 001-15607				
REV.	ECN NO.	Issue Date	Orig. of Change	Description of Change
**	1103145	See ECN	VKN	New Data Sheet
*A	1138903	See ECN	VKN	Converted from preliminary to final Changed I <sub>CC(max)</sub> spec from 2.8 mA to 4.0 mA for f=1MHz Changed I <sub>CC(typ)</sub> spec from 22 mA to 25 mA for f=f <sub>max</sub> Changed I <sub>CC(max)</sub> spec from 25 mA to 30 mA for f=f <sub>max</sub> Added footnote# 8 related to V <sub>IL</sub> Changed I <sub>CCDR</sub> spec from 10 μA to 12 μA Added footnote# 14 related to AC timing parameters