

HM514270A/AL Series

HM51S4270A/AL Series

262,144-word × 16-bit Dynamic Random Access Memory

The Hitachi HM514270A/AL are CMOS dynamic RAM organized as 262,144-word × 16-bit. HM514270A/AL have realized higher density, higher performance and various functions by employing 0.8 μm CMOS process technology and some new CMOS circuit design technologies. The HM514270A/AL offer fast page mode as a high speed access mode.

Multiplexed address input permits the HM514270A/AL to be packaged in standard 400-mil 40-pin plastic SOJ, standard 475-mil 40-pin plastic ZIP and standard 400-mil 40-pin plastic TSOPII.

Internal refresh timer enables HM51S4270A/AL self refresh operation.

Features

- Single 5 V (±10%)
- High speed
 - Access time: 70 ns/80 ns (max)
- Low power dissipation
 - Active mode: 825 mW/770 mW (max)
 - Standby mode: 11 mW (max)
1.1 mW (max) (L-version)
- Fast page mode capability
- 512 refresh cycles: 8 ms
128 ms (L-version)
- 2 $\overline{\text{WE}}$ byte control
- 2 variations of refresh
 - $\overline{\text{RAS}}$ -only refresh
 - $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ refresh
- Battery back up operation (L-version)
- Self-refresh operation (HM51S4270A/AL)

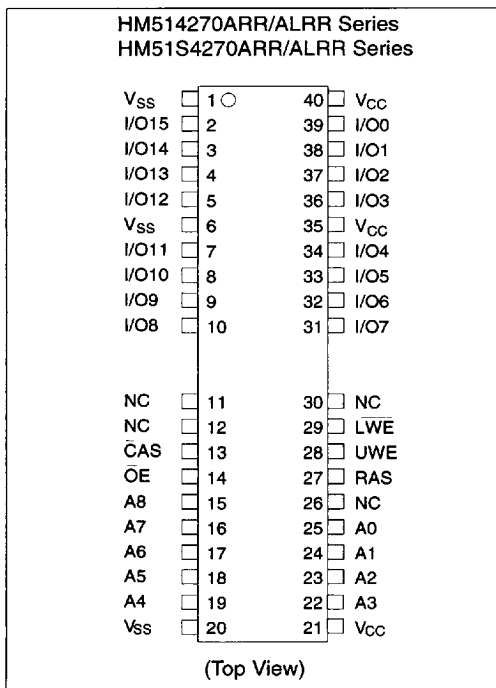
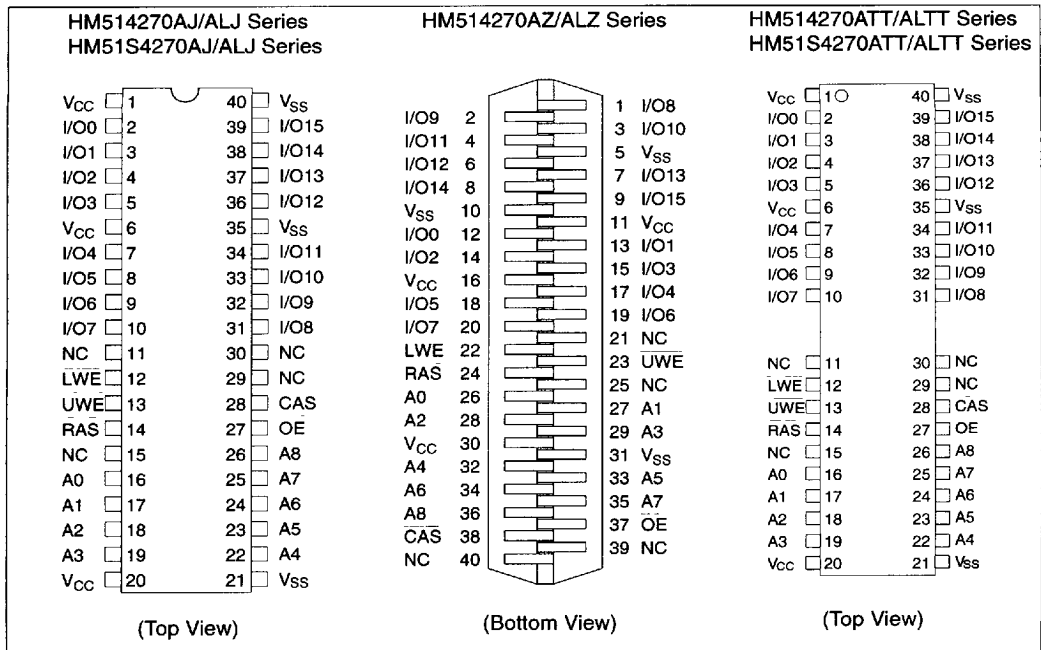
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Ordering Information

Type No.	Access time	Package	Type No.	Access time	Package
HM514270AJ-7	70 ns	400-mil 40-pin	HM514270ALRR-7	70 ns	400 mil 40-pin
HM514270AJ-8	80 ns	plastic SOJ (CP-40DA)	HM514270ALRR-8	80 ns	plastic TSOPII (TTP-40DB)
HM514270AZ-7	70 ns	475-mil 40-pin	HM51S4270AJ-7	70 ns	400-mil 40-pin
HM514270AZ-8	80 ns	plastic ZIP (ZP-40)	HM51S4270AJ-8	80 ns	plastic SOJ (CP-40DA)
HM514270ATT-7	70 ns	400-mil 40-pin	HM51S4270ATT-7	70 ns	400-mil 40-pin
HM514270ATT-8	80 ns	plastic TSOPII (TTP-40DB)	HM51S4270ATT-8	80 ns	plastic TSOPII (TTP-40DB)
HM514270ARR-7	70 ns	400 mil 40-pin	HM51S4270ARR-7	70 ns	400 mil 40-pin
HM514270ARR-8	80 ns	plastic TSOPII (TTP-40DB)	HM51S4270ARR-8	80 ns	plastic TSOPII (TTP-40DB)
HM514270ALJ-7	70 ns	400 mil 40-pin	HM51S4270ALJ-7	70 ns	400 mil 40-pin
HM514270ALJ-8	80 ns	plastic SOJ (CP-40DA)	HM51S4270ALJ-8	80 ns	plastic SOJ (CP-40DA)
HM514270ALZ-7	70 ns	475-mil 40-pin	HM51S4270ALTT-7	70 ns	400 mil 40-pin
HM514270ALZ-8	80 ns	plastic ZIP (ZP-40)	HM51S4270ALTT-8	80 ns	plastic TSOPII (TTP-40DB)
HM514270ALTT-7	70 ns	400 mil 40-pin	HM51S4270ALRR-7	70 ns	400 mil 40-pin
HM514270ALTT-8	80 ns	plastic TSOPII (TTP-40DB)	HM51S4270ALRR-8	80 ns	plastic TSOPII (TTP-40DB)

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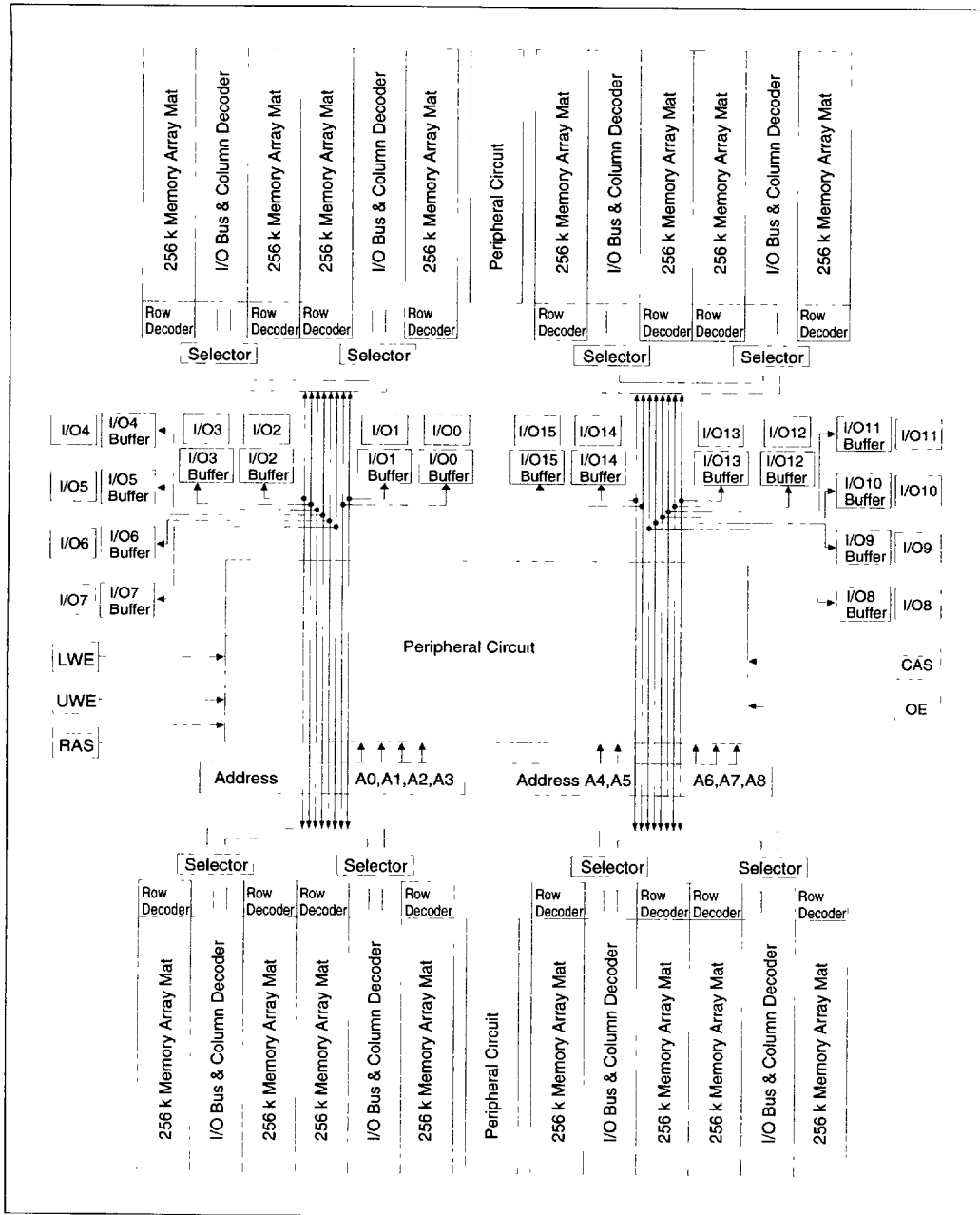
Pin Arrangement



Pin Description

Pin name	Function
A0 – A8	Address input – Row address A0 – A8 – Column address A0 – A8 – Refresh address A0 – A8
I/O0 – I/O15	Data-in/data-out
$\overline{\text{RAS}}$	Row address strobe
$\overline{\text{CAS}}$	Column address strobe
$\overline{\text{UWE}} / \overline{\text{LWE}}$	Read/write enable
$\overline{\text{OE}}$	Output enable
V _{CC}	Power (+5 V)
V _{SS}	Ground

Block Diagram



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Truth Table

Inputs					I/O		Operation
RAS	LWE	UWE	CAS	OE	I/O0 – I/O7	I/O8 – I/O15	
H	H	H	H	H	High-Z	High-Z	Standby
L	H	H	H	H	High-Z	High-Z	Refresh
L	H	H	L	L	Dout	Dout	Word read
L	L	H	L	H	Din	Don't care	Lower byte write
L	H	L	L	H	Don't care	Din	Upper byte write
L	L	L	L	H	Din	Din	Word write
L	H	H	L	H	High-Z	High-Z	
H to L	–	–	L	–	High-Z	High-Z	CBR refresh or Self refresh

Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Voltage on any pin relative to V_{SS}	V_T	–1.0 to +7.0	V
Supply voltage relative to V_{SS}	V_{CC}	–1.0 to +7.0	V
Short circuit output current	I_{out}	50	mA
Power dissipation	P_T	1.0	W
Operating temperature	T_{opr}	0 to +70	°C
Storage temperature	T_{stg}	–55 to +125	°C

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Recommended DC Operating Conditions (Ta = 0 to +70°C) *2

Parameter	Symbol	Min	Typ	Max	Unit	Note
Supply voltage	V _{SS}	0	0	0	V	
	V _{CC}	4.5	5.0	5.5	V	1
Input high voltage	V _{IH}	2.4	—	6.5	V	1
Input low voltage (I/O pin)	V _{IL}	-1.0	—	0.8	V	1
	(Others) V _{IL}	-2.0	—	0.8	V	1

- Notes: 1. All voltage referenced to V_{SS}
 2. The supply voltage with all V_{CC} pins must be on the same level.
 The supply voltage with all V_{SS} pins must be on the same level.

DC Characteristics (Ta = 0 to +70°C, V_{CC} = 5 V ± 10%, V_{SS} = 0 V)

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Parameter	Symbol	-7		-8		Unit	Testconditions	Notes
		Min	Max	Min	Max			
Operating current	I _{CC1}	—	150	—	140	mA	RAS cycling CAS cycling t _{RC} = min	1, 2
Standby current	I _{CC2}	—	2	—	2	mA	TTL interface RAS, CAS = V _{IH} Dout = High-Z	
		—	1	—	1	mA	CMOS interface RAS, CAS, UWE, LWE OE ≥ V _{CC} - 0.2 V Dout = High	
Standby current (L-version)		—	200	—	200	μA	CMOS interface RAS, CAS, OE, UWE, LWE ≥ V _{CC} - 0.2 V Dout = High-Z	
RAS-only refresh current	I _{CC3}	—	140	—	130	mA	t _{RC} = min	2
Standby current	I _{CC5}	—	5	—	5	mA	RAS = V _{IH} CAS = V _{IL} Dout = enable	1
CAS-before-RAS refresh current	I _{CC6}	—	140	—	130	mA	t _{RC} = min	2

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DC Characteristics (Ta = 0 to +70°C, V_{CC} = 5 V ± 10%, V_{SS} = 0 V) (cont)

		HM514270A/AL, HM51S4270A/AL						
		-7		-8				
Parameter	Symbol	Min	Max	Min	Max	Unit	Testconditions	Notes
Fast page mode current	I _{CC7}	—	130	—	120	mA	t _{PC} = min	1, 3
Battery back up current (Standby with CBR refresh) (L-version)	I _{CC10}	—	300	—	300	μA	Standby: CMOS interface Dout = High-Z CBR refresh: t _{RC} = 250 μs t _{RAS} ≤ 1 μs, $\overline{CAS} = V_{IL}$ UWE, LWE, $\overline{OE} = V_{IH}$	4
Self-refresh mode current (HM51S4270A)	I _{CC11}	—	1	—	1	mA	CMOS interface $\overline{RAS}, \overline{CAS} \leq 0.2 V$, Dout = High-Z	
Self-refresh mode current (HM51S4270AL)		—	200	—	200	μA	CMOS interface $\overline{RAS}, \overline{CAS} \leq 0.2 V$, Dout = High-Z	
Input leakage current	I _{LI}	−10	10	−10	10	μA	0 V ≤ Vin ≤ 6.5 V	
Output leakage current	I _{LO}	−10	10	−10	10	μA	0 V ≤ Vout ≤ 6.5 V Dout = disable	
Output high voltage	V _{OH}	2.4	V _{CC}	2.4	V _{CC}	V	High Iout = −5.0 mA	
Output low voltage	V _{OL}	0	0.4	0	0.4	V	Low Iout = 4.2 mA	

- Notes: 1. I_{CC} depends on output load condition when the device is selected. I_{CC} max is specified at the output open condition.
2. Address can be changed once or less while $\overline{RAS} = V_{IL}$.
3. Address can be changed once or less while $\overline{CAS} = V_{IH}$.
4. $V_{IH} \geq V_{CC} - 0.2 V$, $0 \leq V_{IL} \leq 0.2 V$, Address can be changed once or less while $\overline{RAS} = V_{IL}$.
5. All the V_{CC} pins shall be supplied with the same voltage. And all the V_{SS} pins shall be supplied with the same voltage.

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Capacitance ($T_a = 25^\circ\text{C}$, $V_{CC} = 5\text{ V} \pm 10\%$)

Parameter	Symbol	Typ	Max	Unit	Notes
Input capacitance (Address)	C_{I1}	—	5	pF	1
Input capacitance (Clocks)	C_{I2}	—	7	pF	1
Output capacitance (Data-in, Data-out)	$C_{I/O}$	—	10	pF	1, 2

Notes: 1. Capacitance measured with Boonton Meter or effective capacitance measuring method.
2. $\overline{\text{CAS}} = V_{IH}$ to disable Dout.

AC Characteristics ($T_a = 0$ to $+70^\circ\text{C}$, $V_{CC} = 5\text{ V} \pm 10\%$, $V_{SS} = 0\text{ V}$)*1, *14, *15, *17, *18

Test Conditions

- Input rise and fall times: 5 ns
- Input timing reference levels: 0.8 V, 2.4 V
- Output load: 2 TTL gate + C_L (100 pF)
(Including scope and jig)

Read, Write, Read-Modify-Write and Refresh Cycles (Common Parameters)

		HM514270A/AL, HM51S4270A/AL					
		-7		-8			
Parameter	Symbol	Min	Max	Min	Max	Unit	Notes
Random read or write cycle time	t_{RC}	130	—	150	—	ns	
$\overline{\text{RAS}}$ precharge time	t_{RP}	50	—	60	—	ns	
$\overline{\text{RAS}}$ pulse width	t_{RAS}	70	10000	80	10000	ns	
$\overline{\text{CAS}}$ pulse width	t_{CAS}	20	10000	20	10000	ns	22
Row address setup time	t_{ASR}	0	—	0	—	ns	
Row address hold time	t_{RAH}	10	—	10	—	ns	
Column address setup time	t_{ASC}	0	—	0	—	ns	
Column address hold time	t_{CAH}	15	—	15	—	ns	
$\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ delay time	t_{RCD}	20	50	20	60	ns	8
$\overline{\text{RAS}}$ to column address delay time	t_{RAD}	15	35	15	40	ns	9
$\overline{\text{RAS}}$ hold time	t_{RSH}	20	—	20	—	ns	
$\overline{\text{CAS}}$ hold time	t_{CSH}	70	—	80	—	ns	
$\overline{\text{CAS}}$ to $\overline{\text{RAS}}$ precharge time	t_{CRP}	15	—	15	—	ns	23

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Read, Write, Read-Modify-Write and Refresh Cycles (Common Parameters) (cont)

		HM514270A/AL, HM51S4270A/AL					
		-7		-8			
Parameter	Symbol	Min	Max	Min	Max	Unit	Notes
OE to Din delay time	t _{ODD}	20	—	20	—	ns	
OE delay time from Din	t _{DZO}	0	—	0	—	ns	
CAS setup time from Din	t _{DZC}	0	—	0	—	ns	
Transition time (rise and fall)	t _T	3	50	3	50	ns	7
Refresh period	t _{REF}	—	8	—	8	ms	
Refresh period (L-version)	t _{REF}	—	128	—	128	ms	

Read Cycle

		HM514270A/AL, HM51S4270A/AL					
		-7		-8			
Parameter	Symbol	Min	Max	Min	Max	Unit	Notes
Access time from $\overline{RAS}$	t _{RAC}	—	70	—	80	ns	2, 3
Access time from $\overline{CAS}$	t _{CAC}	—	20	—	20	ns	3, 4, 13
Access time from address	t _{AA}	—	35	—	40	ns	3, 5, 13
Access time from $\overline{OE}$	t _{OAC}	—	20	—	20	ns	3, 22
Read command setup time	t _{RCS}	0	—	0	—	ns	20
Read command hold time to $\overline{CAS}$	t _{RCH}	0	—	0	—	ns	16, 19
Read command hold time to $\overline{RAS}$	t _{RRH}	0	—	0	—	ns	16, 19
Column address to $\overline{RAS}$ lead time	t _{RAL}	35	—	40	—	ns	
Output buffer turn-off time	t _{OFF1}	0	15	0	15	ns	6
Output buffer turn-off to $\overline{OE}$	t _{OFF2}	0	15	0	15	ns	6
$\overline{CAS}$ to Din delay time	t _{CDD}	15	—	15	—	ns	

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Write Cycle

		HM514270A/AL, HM51S4270A/AL					
		-7		-8			
Parameter	Symbol	Min	Max	Min	Max	Unit	Notes
Write command setup time	t _{WCS}	0	—	0	—	ns	10, 19
Write command hold time	t _{WCH}	15	—	15	—	ns	20
Write command pulse width	t _{WP}	10	—	10	—	ns	21
Write command to $\overline{\text{RAS}}$ lead time	t _{RWL}	20	—	20	—	ns	21
Write command to $\overline{\text{CAS}}$ lead time	t _{CWL}	20	—	20	—	ns	21
Data-in setup time	t _{DS}	0	—	0	—	ns	11, 21
Data-in hold time	t _{DH}	15	—	15	—	ns	11, 21
$\overline{\text{CAS}}$ to $\overline{\text{OE}}$ delay time	t _{COD}	—	0	—	0	ns	22

Read-Modify-Write Cycle

		HM514270A/AL, HM51S4270A/AL					
		-7		-8			
Parameter	Symbol	Min	Max	Min	Max	Unit	Notes
Read-modify-write cycle time	t _{RWC}	180	—	200	—	ns	
$\overline{\text{RAS}}$ to $\overline{\text{WE}}$ delay time	t _{RWD}	95	—	105	—	ns	10,19
$\overline{\text{CAS}}$ to $\overline{\text{WE}}$ delay time	t _{CWD}	45	—	45	—	ns	10,19
Column address to $\overline{\text{WE}}$ delay time	t _{AWD}	60	—	65	—	ns	10, 19
$\overline{\text{OE}}$ hold time from $\overline{\text{WE}}$	t _{OEH}	20	—	20	—	ns	21

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Refresh Cycle

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		-7		-8			
Parameter	Symbol	Min	Max	Min	Max	Unit	Notes
CAS setup time (CAS-before-RAS refresh cycle)	t _{CSR}	10	—	10	—	ns	
CAS hold time (CAS-before-RAS refresh cycle)	t _{CHR}	10	—	10	—	ns	
RAS precharge to CAS hold time	t _{RPC}	10	—	10	—	ns	
CAS precharge time in normal mode	t _{CPN}	10	—	10	—	ns	

Fast Page Mode Cycle

		HM514270A/AL, HM51S4270A/AL					
		-7		-8			
Parameter	Symbol	Min	Max	Min	Max	Unit	Notes
Fast page mode cycle time	t _{PC}	45	—	50	—	ns	
Fast page mode $\overline{\text{CAS}}$ precharge time	t _{CP}	10	—	10	—	ns	
Fast page mode $\overline{\text{RAS}}$ pulse width	t _{RASC}	—	100000	—	100000	ns	12
Access time from $\overline{\text{CAS}}$ precharge	t _{ACP}	—	40	—	45	ns	3, 13
$\overline{\text{RAS}}$ hold time from $\overline{\text{CAS}}$ precharge	t _{RHCP}	40	—	45	—	ns	
Fast page mode read-modify-write cycle $\overline{\text{CAS}}$ precharge to $\overline{\text{UWE}}$, $\overline{\text{LWE}}$ delay time	t _{CPW}	65	—	70	—	ns	21
Fast page mode read-modify-write cycle time	t _{PCM}	95	—	100	—	ns	

Self-refresh Mode

		HM51S4270A/AL					
		-7		-8			
Parameter	Symbol	Min	Max	Min	Max	Unit	Notes
RAS pulse width (self-refresh)	t _{RASS}	100	—	100	—	μs	
RAS precharge time (self-refresh)	t _{RPS}	130	—	150	—	ns	
CAS hold time (self-refresh)	t _{CHS}	−50	—	−50	—	ns	

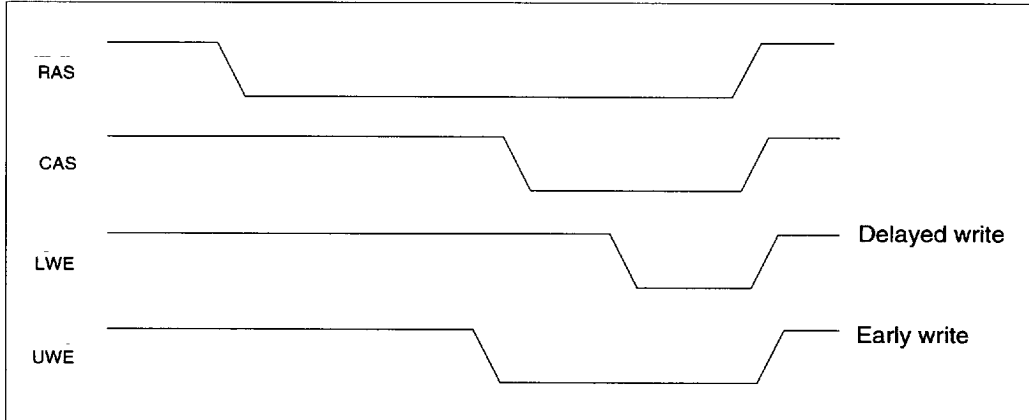
- Notes:
1. AC measurements assume $t_T = 5$ ns.
 2. Assumes that $t_{RCD} \leq t_{RCD}(\text{max})$ and $t_{RAD} \leq t_{RAD}(\text{max})$. If t_{RCD} or t_{RAD} is greater than the maximum recommended value shown in this table, t_{RAC} exceeds the value shown.
 3. Measured with a load circuit equivalent to 2 TTL loads and 100 pF.
 4. Assumes that $t_{RCD} \geq t_{RCD}(\text{max})$ and $t_{RAD} \leq t_{RAD}(\text{max})$.
 5. Assumes that $t_{RCD} \leq t_{RCD}(\text{max})$ and $t_{RAD} \geq t_{RAD}(\text{max})$.
 6. $t_{OFF}(\text{max})$ defines the time at which the output achieves the open circuit condition and is not referred to output voltage levels.
 7. $V_{IH}(\text{min})$ and $V_{IL}(\text{max})$ are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL} .
 8. Operation with the $t_{RCD}(\text{max})$ limit insures that $t_{RAC}(\text{max})$ can be met, $t_{RCD}(\text{max})$ is specified as a reference point only, if t_{RCD} is greater than the specified $t_{RCD}(\text{max})$ limit, then access time is controlled exclusively by t_{CAC} .
 9. Operation with the $t_{RAD}(\text{max})$ limit insures that $t_{RAC}(\text{max})$ can be met, $t_{RAD}(\text{max})$ is specified as a reference point only, if t_{RAD} is greater than the specified $t_{RAD}(\text{max})$ limit, then access time is controlled exclusively by t_{AA} .
 10. t_{WCS} , t_{RWD} , t_{CWD} and t_{AWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only: if $t_{WCS} \geq t_{WCS}(\text{min})$, the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle; if $t_{RWD} \geq t_{RWD}(\text{min})$, $t_{CWD} \geq t_{CWD}(\text{min})$, $t_{AWD} \geq t_{AWD}(\text{min})$ and $t_{CPW} \geq t_{CPW}(\text{min})$, the cycle is a read-modify-write and the data output will contain data read from the selected cell; if neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.
 11. These parameters are referred to $\overline{\text{CAS}}$ leading edge in an early write cycle and to $\overline{\text{WE}}$ leading edge in a delayed write or a read-modify-write cycle.
 12. t_{RASC} defines $\overline{\text{RAS}}$ pulse width in fast page mode cycles.
 13. Access time is determined by the longer of t_{AA} or t_{CAC} or t_{ACP} .
 14. After power up pause for 100 μs, then DRAM initialization requires a minimum of eight $\overline{\text{RAS}}$ -only refresh or eight $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ refresh cycles. If the user will implement $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ timing in their system, then the eight initialization cycles MUST be $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ cycles.
 15. In delayed write or read-modify-write cycles, $\overline{\text{OE}}$ must disable output buffer prior to applying data to the device.
 16. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
 17. The supply voltage with all V_{CC} pins must be on the same level.
The supply voltage with all V_{SS} pins must be on the same level.

18. A word of data can be written only when $\overline{\text{LWE}}$ and $\overline{\text{UWE}}$ go low at the same time. This implies that early write cycles cannot be combined with delayed write cycles in the same cycles because all data is latched at the fall of the first $\overline{\text{WE}}$. In other words, staggering the $\overline{\text{WE}}$ signals in one cycle is not permitted.
19. t_{RCH} , t_{RRH} , t_{WCS} , t_{RWD} , t_{CWD} and t_{AWD} are determined by the earlier falling edge of $\overline{\text{UWE}}$ and $\overline{\text{LWE}}$.
20. t_{WCH} and t_{RCS} are determined by the later rising edge of $\overline{\text{UWE}}$ or $\overline{\text{LWE}}$.
21. t_{WP} , t_{RWL} , t_{CWL} , t_{OEHL} , t_{DS} , t_{DH} and t_{CPW} should be satisfied by both $\overline{\text{UWE}}$ and $\overline{\text{LWE}}$.
22. When output buffers are enabled once, sustain the low impedance state until valid data is obtained. When output buffer is turned on and off within a very short time, generally it causes large $V_{\text{CC}}/V_{\text{SS}}$ line noise, which causes to degrade V_{IH} (min)/ V_{IL} (max) level.
23. t_{CRP} is planned to be improved to match the standard DRAM specifications.
24. If you use distributed CBR refresh mode with 15.6 μs interval in normal read/write cycle, CBR refresh should be executed within 15.6 μs immediately after exiting from and before entering into self refresh mode.
25. If you use $\overline{\text{RAS}}$ only refresh or CBR burst refresh mode in normal read/write cycle, 512 cycles of distributed CBR refresh with 15.6 μs interval should be executed within 8 ms immediately after exiting from and before entering into the self refresh mode.
26. Repetitive self refresh mode without refreshing all memory is not allowed. Once you exit from self refresh mode, all memory cells need to be refreshed before re-entering the self refresh mode again.

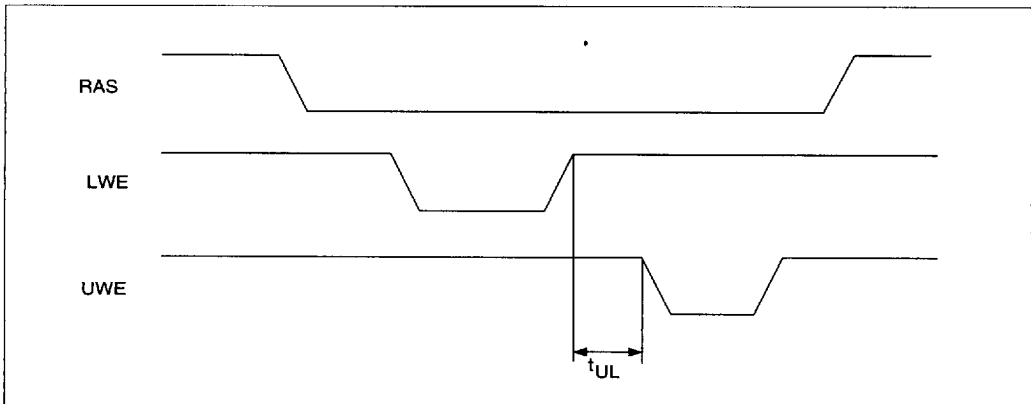
Notes concerning $2\overline{WE}$ control

Please do not separate the $\overline{UWE}/\overline{LWE}$ operation timing intentionally. However skew between $\overline{UWE}/\overline{LWE}$ are allowed under the following conditions.

- (1) Each of the $\overline{UWE}/\overline{LWE}$ should satisfy the timing specifications individually.
- (2) Different operation mode for upper/lower byte is not allowed; such as following.

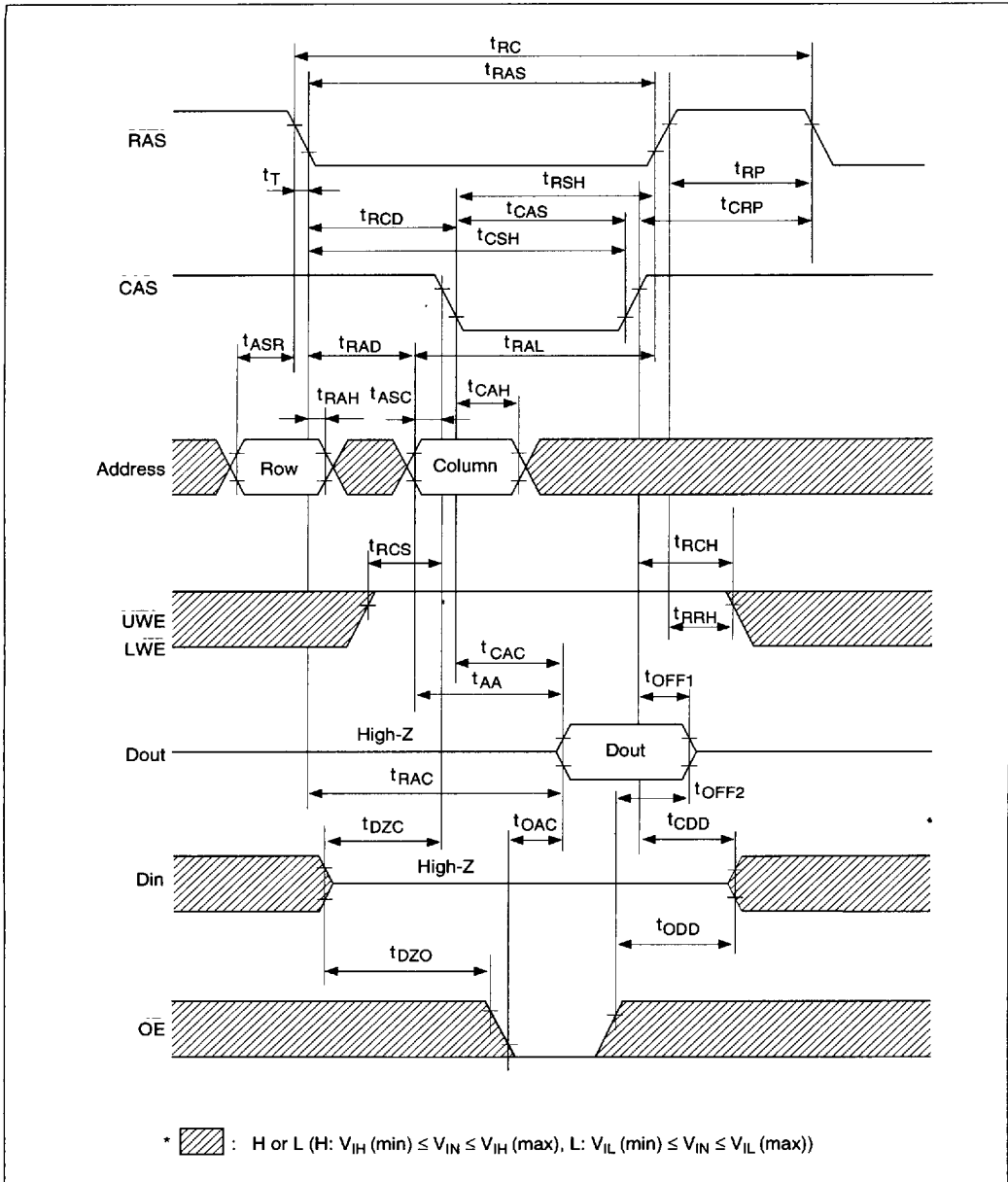


- (3) Closely separated upper/lower byte control is not allowed, unless the condition ($t_{CP} \leq t_{UL}$) is satisfied.

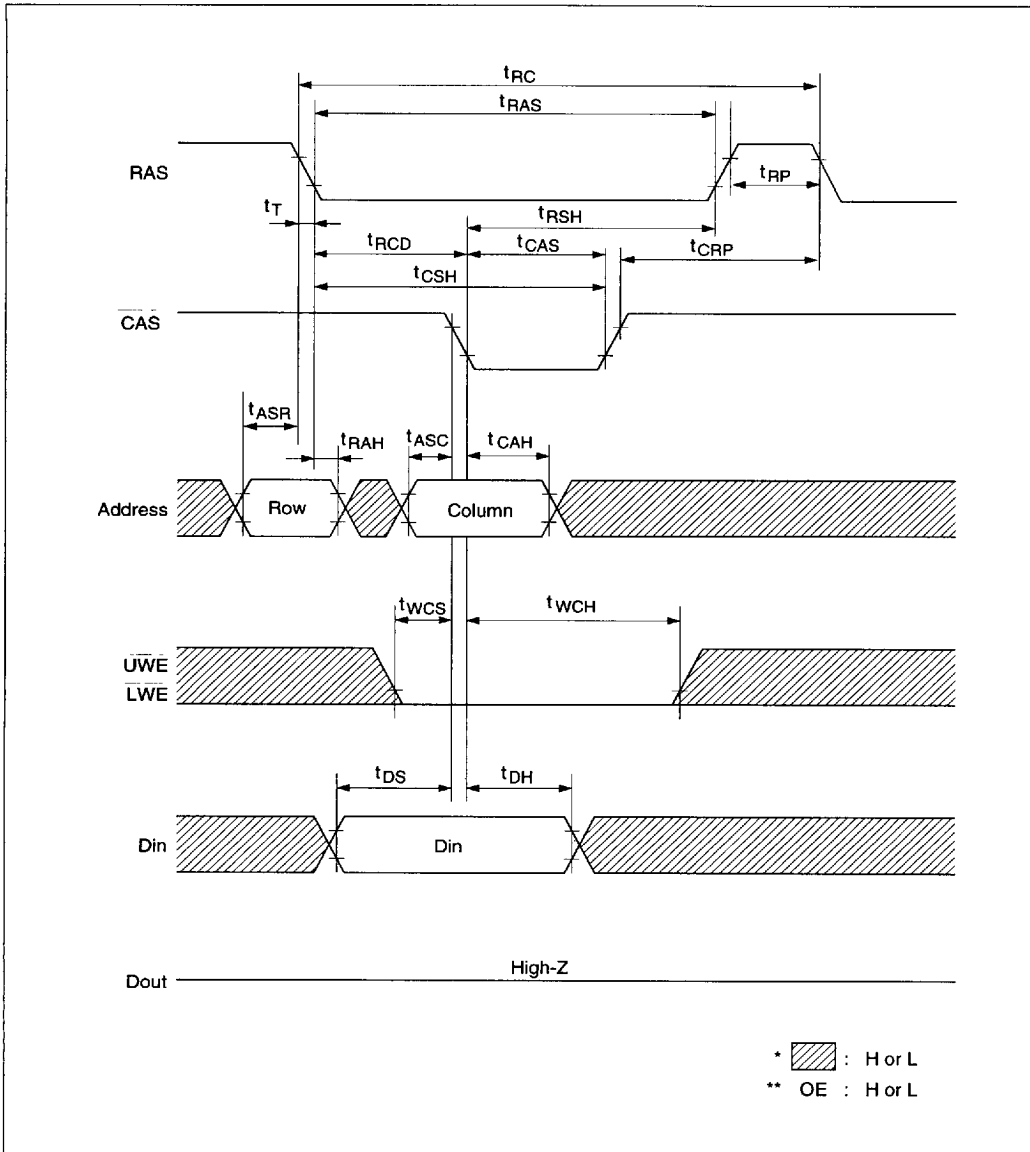


Timing Waveforms

Read Cycle

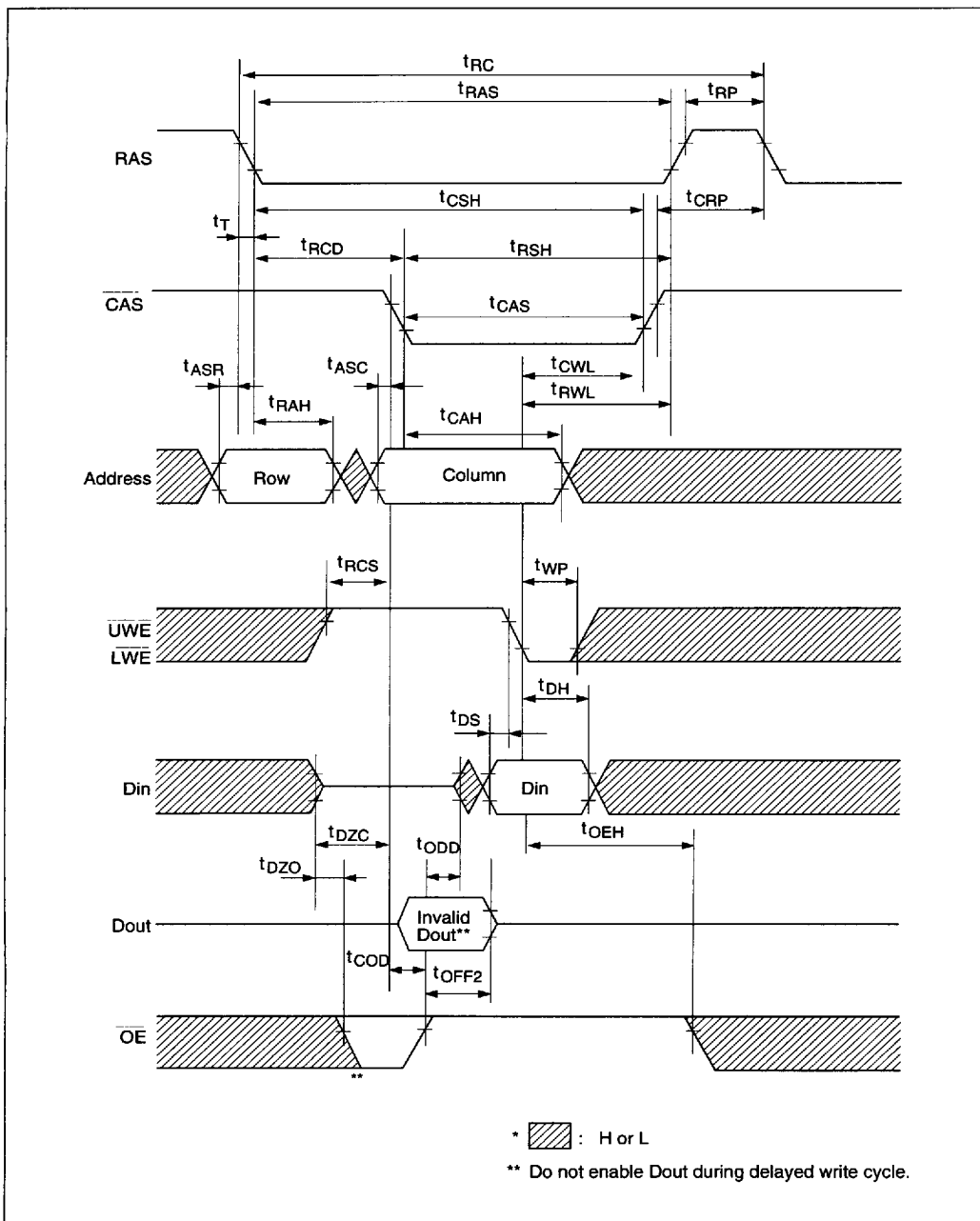


Early Write Cycle

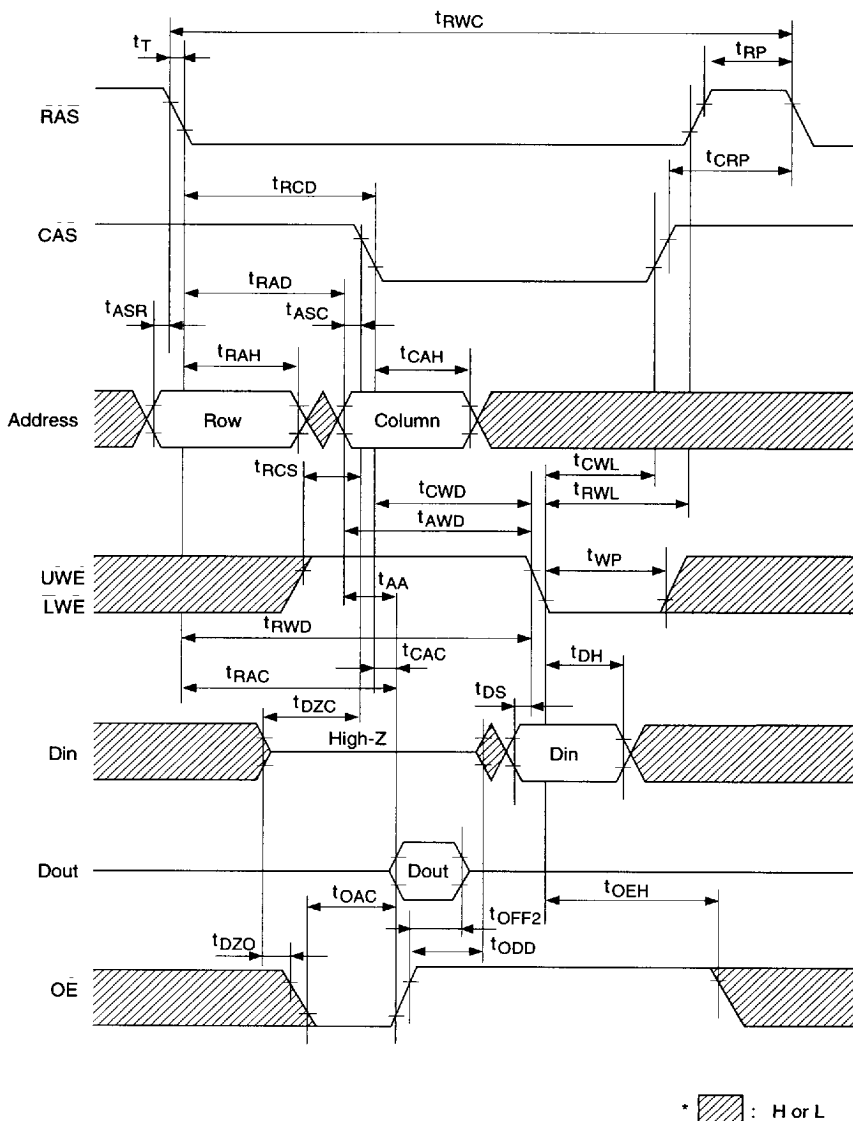


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Delayed Write Cycle

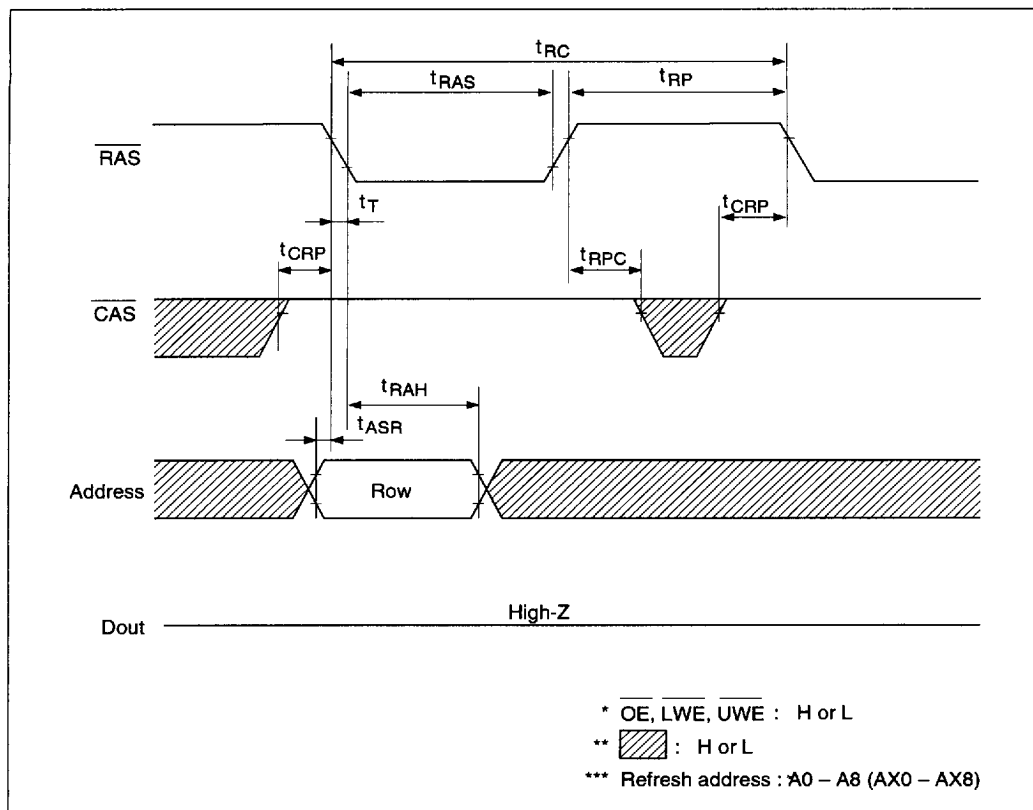


Read-Modify-Write Cycle

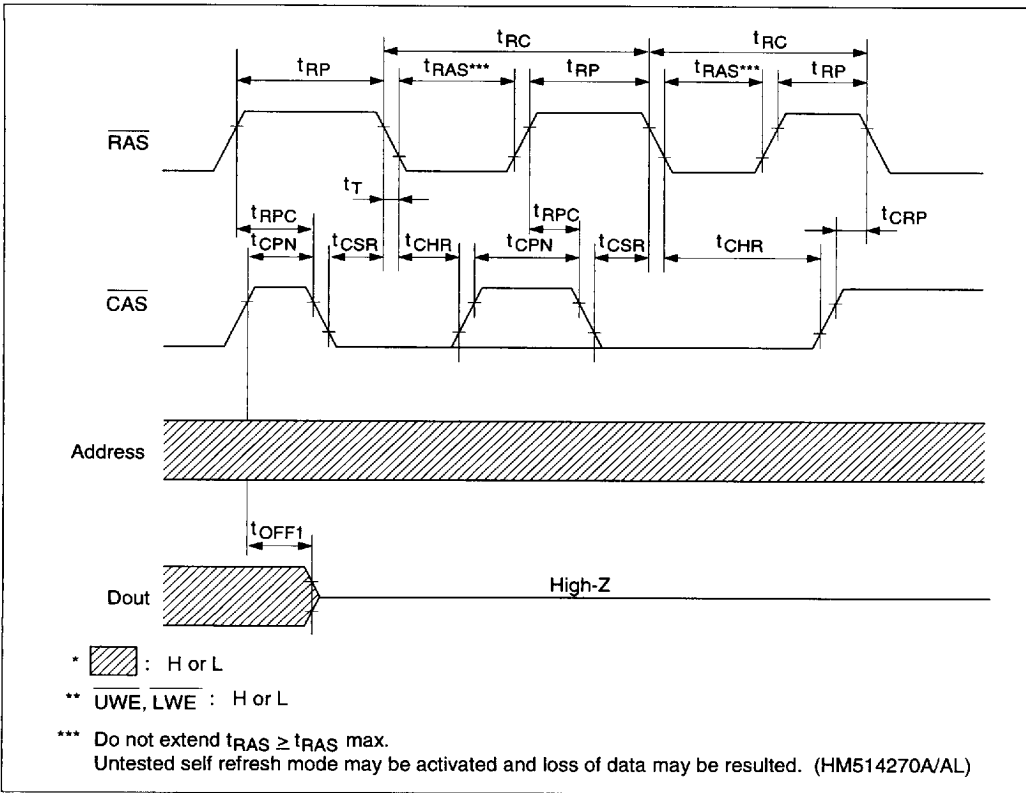


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RAS-Only Refresh Cycle

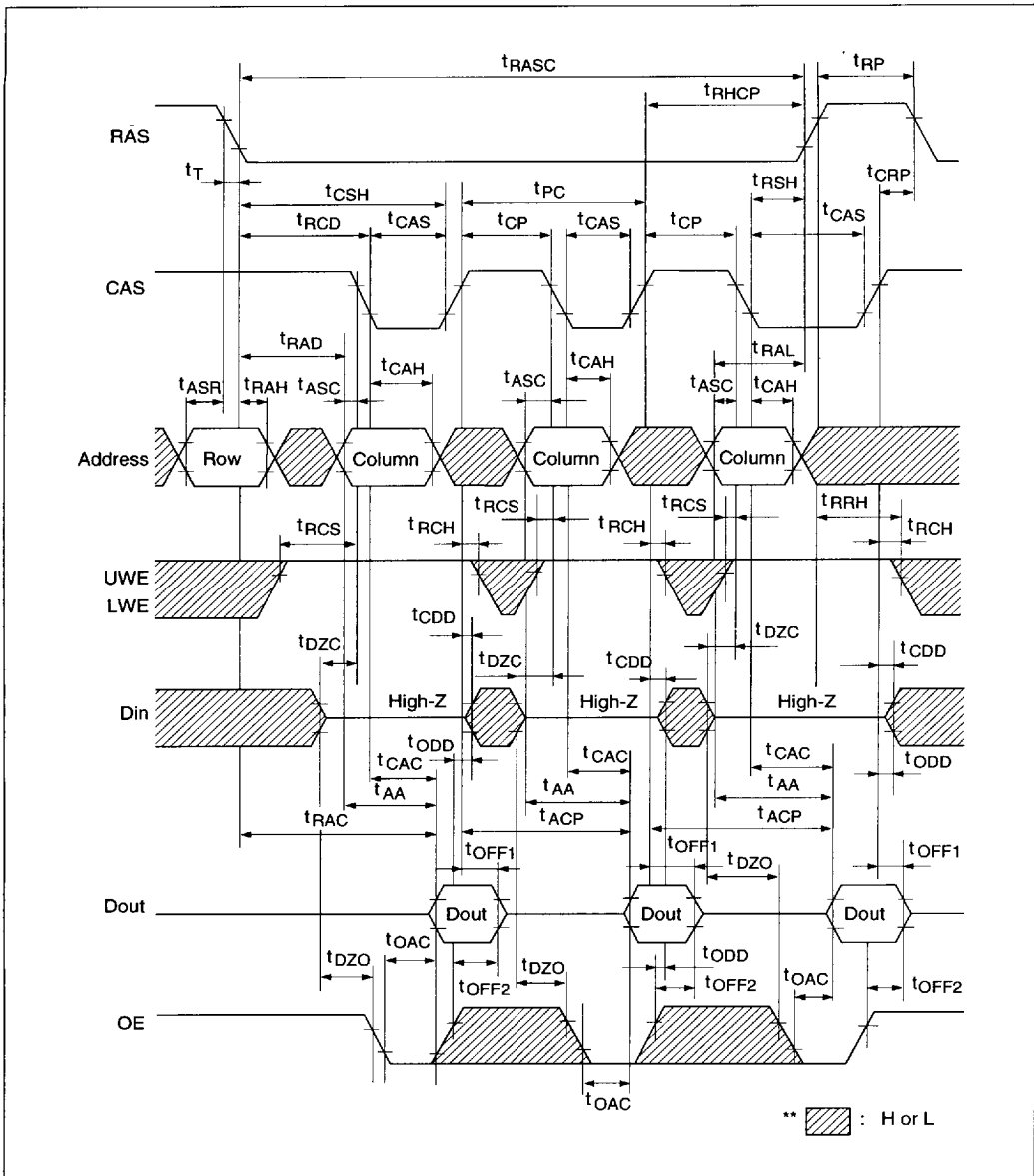


CAS-Before-RAS Refresh Cycle

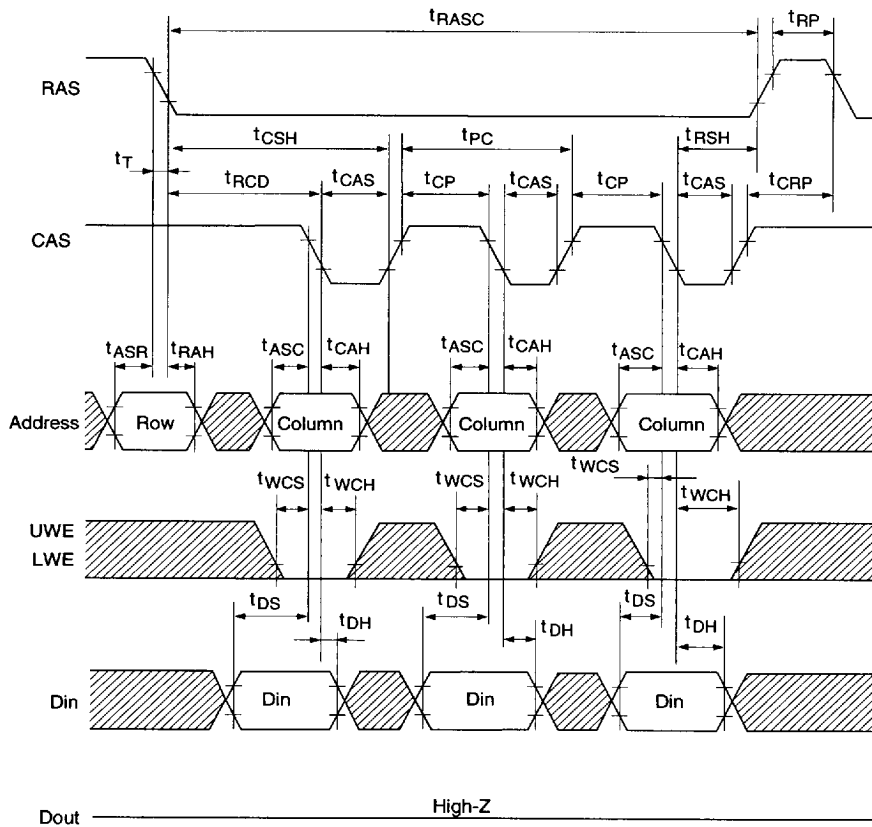


HM514270A/AL, HM51S4270A/AL Series

Fast Page Mode Read Cycle



Fast Page Mode Early Write Cycle

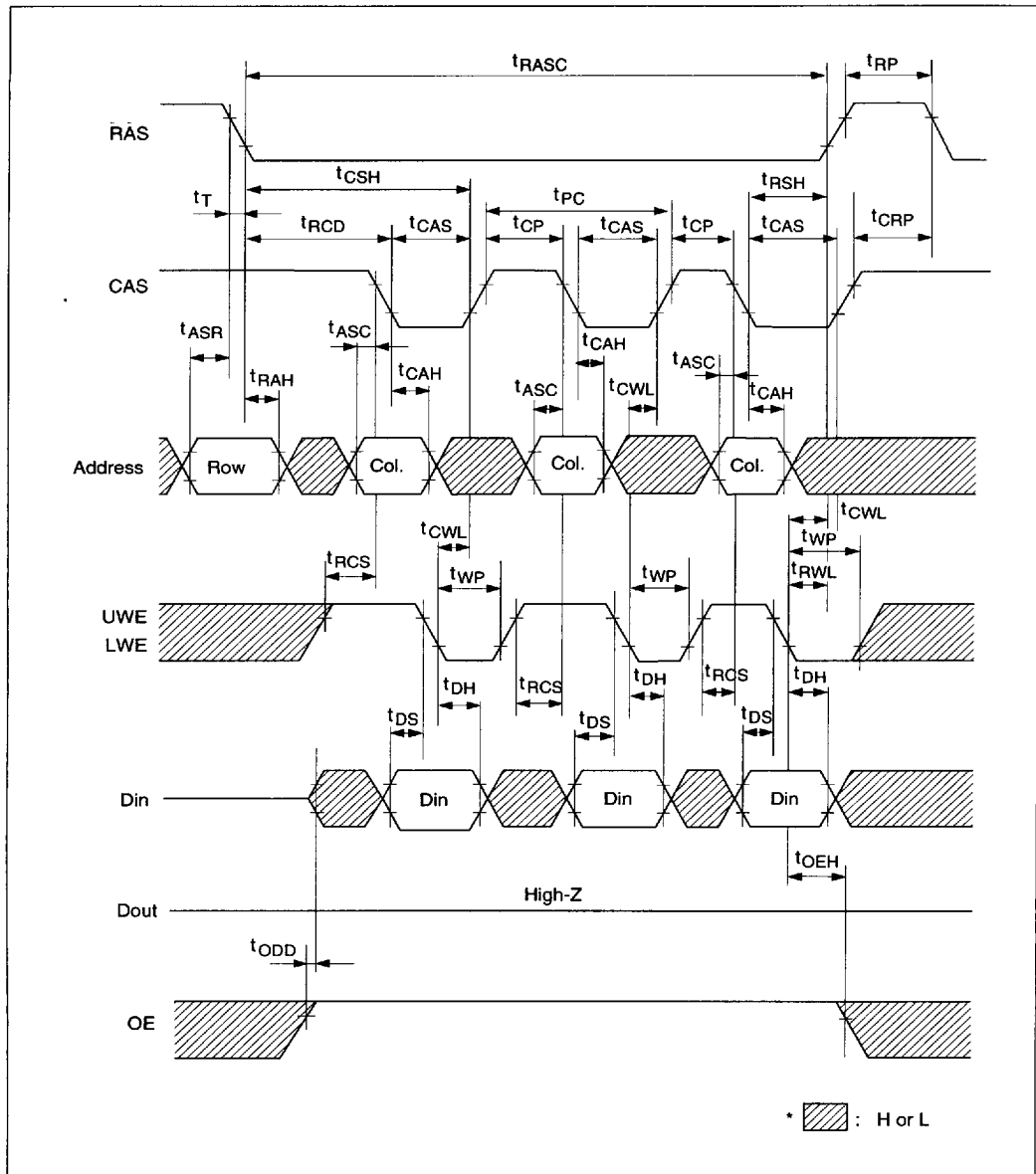


* OE : H or L

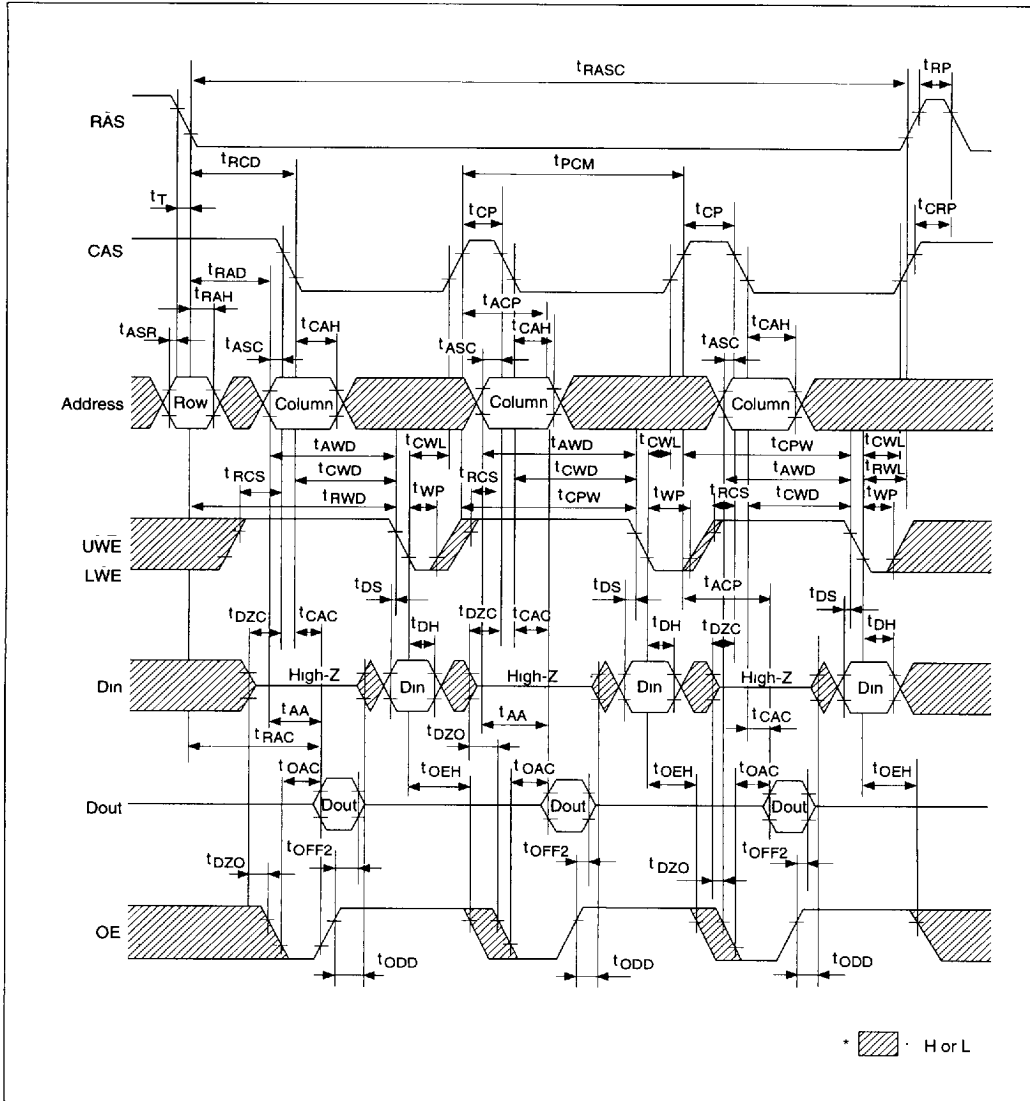
**  : H or L

HM514270A/AL, HM51S4270A/AL Series

Fast Page Mode Delayed Write Cycle



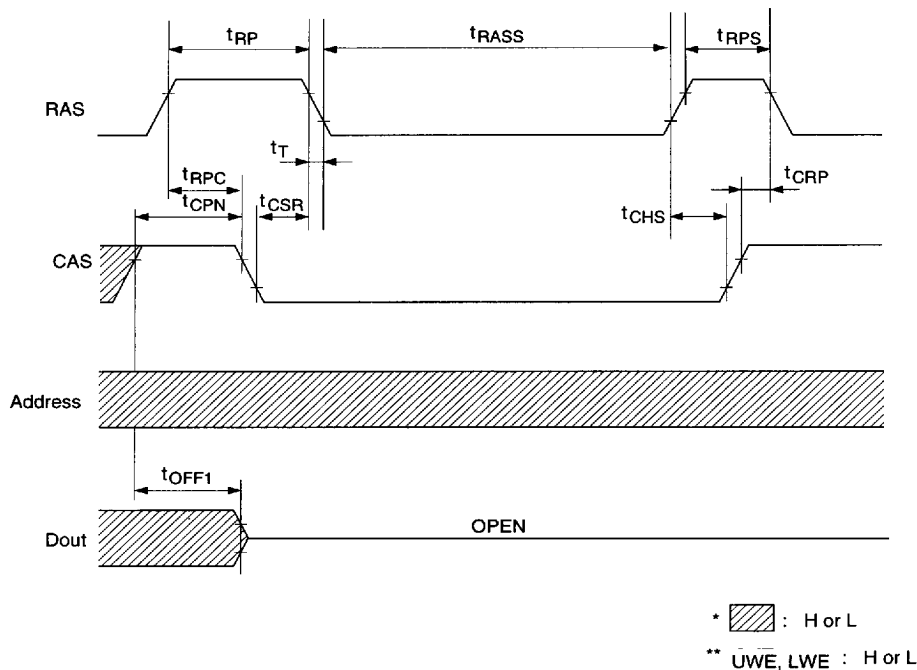
Fast Page Mode Read-Modify-Write Cycle



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Hitachi 355

Self Refresh Cycle



The low self refresh current is achieved by introducing extremely long internal refresh cycle. Therefore some care needs to be taken on the refresh.

1. Please do not use t_{RASS} timing, $10 \mu s \leq t_{RASS} \leq 100 \mu s$. During this period, the device is in transition state from normal operation mode to self refresh mode. If $t_{RASS} \geq 100 \mu s$, then $\overline{RAS}$ precharge time should use t_{RPS} instead of t_{RP} .
2. If you use $\overline{RAS}$ only refresh or CBR burst refresh mode in normal read/write cycle, 512 cycles of distributed CBR refresh with $15.6 \mu s$ interval should be executed within 8 ms immediately after exiting from and before entering into the self refresh mode.
3. If you use distributed CBR refresh mode with $15.6 \mu s$ interval in normal read/write cycle, CBR refresh should be executed within $15.6 \mu s$ immediately after exiting from and before entering into self refresh mode.
4. Repetitive self refresh mode without refreshing all memory is not allowed. Once you exit from self refresh mode, all memory cells need to be refreshed before re-entering the self refresh mode again.