

HYUNDAI
SEMICONDUCTOR

HY62256A
32K×8-Bit CMOS SRAM

M241201B-MAY92

T-46-23-13

DESCRIPTION

The HY62256A is a high speed low power, 32,768 words by 8-bit CMOS static RAM fabricated using HYUNDAI's high performance twin tub CMOS process. This high reliability process coupled with innovative circuit design techniques, yields maximum access time of 70ns.

The HY62256A has a data retention mode that guarantees data will remain valid at a minimum power supply voltage of 2.0 volt.

Using CMOS technology, supply voltages from 2.0 to 5.5 volt have little effect on supply current in data retention mode. Reducing the supply voltage to minimize current drain is unnecessary with the HY62256A family.

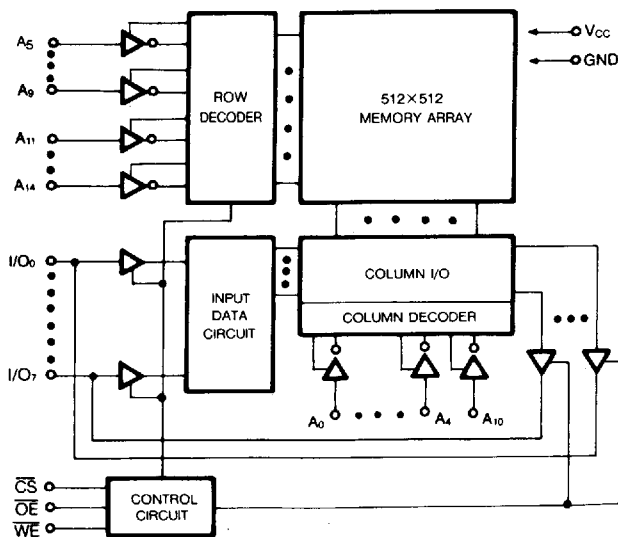
FEATURES

- High speed—70/85/100/120ns (max.)
- Low power consumption
 - 200mW typical operating (HY62256A-70)
 - 10µW typical standby (L/LL-version)
- Battery back up (L/LL-version)
 - 2 volt data retention
- Fully static operation
 - No clock or refresh required
- All inputs and outputs directly TTL compatible
- Tri-state output
- High reliability 28 pin 600 mil P-DIP and 330 mil SOP

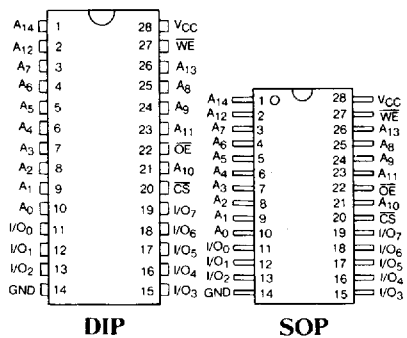
| | HY62256A-70 | HY62256A-85 | HY62256A-100 | HY62256A-120 |
|--|-------------|-------------|--------------|--------------|
| Maximum Access Time (ns) | 70 | 85 | 100 | 120 |
| Maximum Average Operating Current (mA) | 70 | 70 | 70 | 70 |
| Maximum Standby Current (mA) | | 1.0 | 1.0 | 1.0 |
| | L | 0.1 | 0.1 | 0.1 |
| | LL | 0.05 | 0.05 | 0.05 |

5

BLOCK DIAGRAM



PIN CONNECTIONS



PIN NAMES

| | |
|------------------------------------|-------------------|
| A ₀ -A ₁₄ | ADDRESS INPUT |
| I/O ₀ -I/O ₇ | DATA INPUT/OUTPUT |
| CS | CHIP SELECT |
| WE | WRITE ENABLE |
| OE | OUTPUT ENABLE |
| V _{CC} | POWER |
| GND | GROUND |

HY62256A 32,768×8-Bit CMOS SRAM

T-46-23-13

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

| SYMBOL | PARAMETER | RATING | UNIT |
|--|---|----------------------------|------|
| V _{DD} , V _{IN} , V _{I/O} | Power Supply, Input, Input/Output Voltage | -0.5 ⁽²⁾ to 7.0 | V |
| T _{BIAS} | Temperature Under Bias | -10 to 125 | °C |
| T _{STG} | Storage Temperature | -65 to 150 | °C |
| P _D | Power Dissipation | 1.0 | W |
| I _{OUT} | Data Output Current | 50 | mA |

NOTES :

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Exposure to absolute maximum rating condition for extended may affect reliability.

2. -3.5V for 20ns pulse.

RECOMMENDED DC OPERATING CONDITIONS

(T_A=0°C to 70°C)

| SYMBOL | PARAMETER | MIN. | TYP. | MAX. | UNIT |
|-----------------|--------------------|---------------------|------|------|------|
| V _{CC} | Supply Voltage | 4.5 | 5.0 | 5.5 | V |
| V _{IH} | Input High Voltage | 2.2 | 3.5 | 6.0 | V |
| V _{IL} | Input Low Voltage | -0.5 ⁽¹⁾ | - | 0.8 | V |

NOTE :

1. -3.5V for 20 ns pulse

TRUTH TABLE

| MODE | $\overline{\text{CS}}$ | $\overline{\text{OE}}$ | $\overline{\text{WE}}$ | I/O OPERATION |
|-----------------|------------------------|------------------------|------------------------|------------------|
| Standby | H | X | X | High-Z |
| Read | L | L | H | D _{OUT} |
| Write | L | X | L | D _{IN} |
| Output Disabled | L | H | H | High-Z |

NOTE :

1. X : H or L

T-46-23-13

DC CHARACTERISTICS

(V_{CC} = 5V ± 10%, T_A = 0°C to 70°C)

| SYMBOL | PARAMETER | TEST CONDITIONS | HY62256A | | | UNIT | |
|------------------|--------------------------------|--|----------|---------------------|------|------|----|
| | | | MIN. | TYP. ⁽¹⁾ | MAX. | | |
| I _{IL} | Input Leakage Current | V _{IN} =GND to V _{CC} | - | - | 1 | μA | |
| I _{LO} | Output Leakage Current | $\overline{CS}=V_{IH}$ or $\overline{OE}=V_{IH}$ or $\overline{WE}=V_{IL}$ V _{I/O} =GND to V _{CC} | - | - | 1 | μA | |
| I _{CC} | Operating Power Supply Current | $\overline{CS}=V_{IL}$, V _{IN} =V _{IH} or V _{IL} , I _{I/O} =0mA | - | 7 | 15 | mA | |
| I _{CC1} | Average Operating Current | $\overline{CS}=V_{IL}$ Min Duty Cycle=100% I _{I/O} =0mA | -70 | - | 40 | 70 | mA |
| | | | -85 | - | 35 | 70 | mA |
| | | | -10 | - | 30 | 70 | mA |
| | | | -12 | - | 25 | 70 | mA |
| I _{SB} | Standby Power Supply Current | $\overline{CS}=V_{IH}$ | - | - | 2 | mA | |
| I _{SB1} | | $\overline{CS} \geq V_{CC}-0.2V$, | L | - | 2 | 100 | μA |
| | | | LL | - | 2 | 50 | μA |
| V _{OL} | Output Low Voltage | I _{OL} =2.1mA | - | - | 0.4 | V | |
| V _{OH} | Output High Voltage | I _{OH} =-1.0mA | 2.4 | - | - | V | |

NOTE:

1. Typical values are at V_{CC}=5.0V, T_A=25°C and specified loading.

AC CHARACTERISTICS

(V_{CC} = 5V ± 10%, T_A = 0°C to 70°C)

READ CYCLE

| SYMBOL | PARAMETER | HY62256A-70 | | HY62256A-85 | | HY62256A-10 | | HY62256A-12 | | UNIT |
|------------------|--------------------------------------|-------------|------|-------------|------|-------------|------|-------------|------|------|
| | | MIN. | MAX. | MIN. | MAX. | MIN. | MAX. | MIN. | MAX. | |
| t _{RC} | Read Cycle Time | 70 | - | 85 | - | 100 | - | 120 | - | ns |
| t _{AA} | Address Access Time | - | 70 | - | 85 | - | 100 | - | 120 | ns |
| t _{ACS} | Chip Select Access Time | - | 70 | - | 85 | - | 100 | - | 120 | ns |
| t _{CLZ} | Chip Selection to Output in Low-Z | 5 | - | 5 | - | 5 | - | 5 | - | ns |
| t _{OE} | Output Enable to Output Valid | - | 35 | - | 45 | - | 50 | - | 60 | ns |
| t _{OLZ} | Output Enable to Output in Low-Z | 5 | - | 5 | - | 5 | - | 5 | - | ns |
| t _{CHZ} | Chip Deselection to Output in High-Z | 0 | 30 | 0 | 30 | 0 | 35 | 0 | 40 | ns |
| t _{OHZ} | Output Disable to Output in High-Z | 0 | 30 | 0 | 30 | 0 | 35 | 0 | 40 | ns |
| t _{OH} | Output Hold from Address Change | 5 | - | 5 | - | 10 | - | 10 | - | ns |

HY62256A 32,768×8-Bit CMOS SRAM

T-46-23-13

WRITE CYCLE

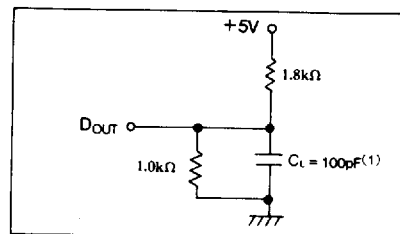
| SYMBOL | PARAMETER | HY62256A-70 | | HY62256A-85 | | HY62256A-10 | | HY62256A-12 | | UNIT |
|------------------|------------------------------------|-------------|------|-------------|------|-------------|------|-------------|------|------|
| | | MIN. | MAX. | MIN. | MAX. | MIN. | MAX. | MIN. | MAX. | |
| t _{WC} | Write Cycle Time | 70 | — | 85 | — | 100 | — | 120 | — | ns |
| t _{CW} | Chip Selection to End of Write | 65 | — | 75 | — | 80 | — | 85 | — | ns |
| t _{AW} | Address Valid to End of Write | 65 | — | 75 | — | 80 | — | 85 | — | ns |
| t _{AS} | Address Set-up Time | 0 | — | 0 | — | 0 | — | 0 | — | ns |
| t _{WP} | Write Pulse Width | 55 | — | 60 | — | 70 | — | 70 | — | ns |
| t _{WR} | Write Recovery Time | 0 | — | 0 | — | 0 | — | 0 | — | ns |
| t _{OZH} | Output Disable to Output in High-Z | 0 | 30 | 0 | 30 | 0 | 35 | 0 | 40 | ns |
| t _{WHZ} | Write to Output in High-Z | 0 | 30 | 0 | 30 | 0 | 35 | 0 | 40 | ns |
| t _{DW} | Data to Write Time Overlap | 35 | — | 40 | — | 40 | — | 50 | — | ns |
| t _{DH} | Data Hold from Write Time | 0 | — | 0 | — | 0 | — | 0 | — | ns |
| t _{OW} | Output Active from End of Write | 5 | — | 5 | — | 10 | — | 10 | — | ns |

AC TEST CONDITIONS

(T_A=0°C to 70°C)

| | |
|---|--------------|
| Input Pulse Level | 0.8V to 2.4V |
| Input Rise and Fall Time | 5ns |
| Input and Output Timing Reference Level | 1.5V |

OUTPUT LOAD



NOTE:

1. Including scope and the Jig.

CAPACITANCE⁽¹⁾(T_A=25°C, f=1.0 MHz)

| SYMBOL | PARAMETER | CONDITIONS | MAX. | UNIT |
|------------------|--------------------------|----------------------|------|------|
| C _{IN} | Input Capacitance | V _{IN} =0V | 6 | pF |
| C _{I/O} | Input/Output Capacitance | V _{I/O} =0V | 8 | pF |

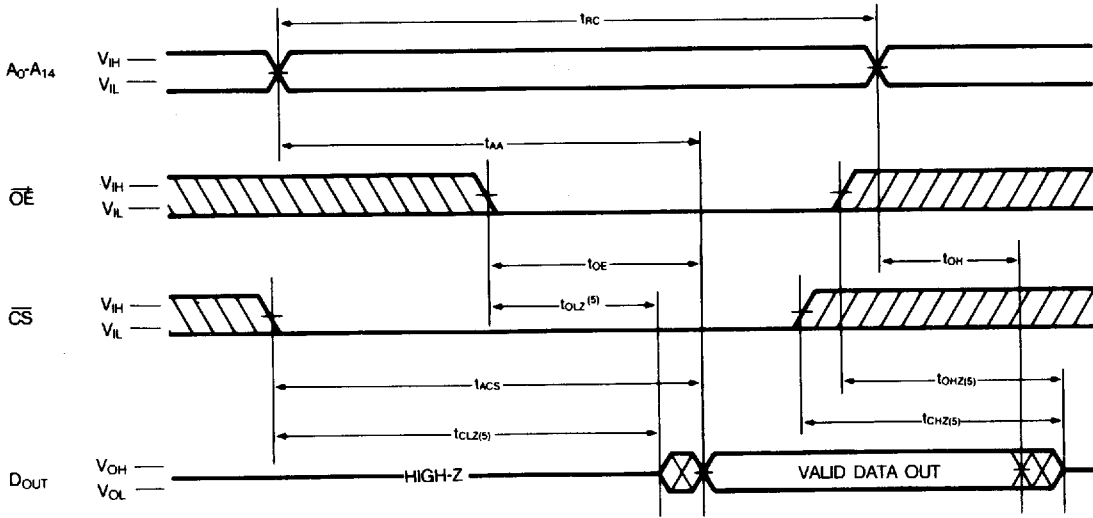
NOTE:

1. This parameter is sampled and not 100% tested.

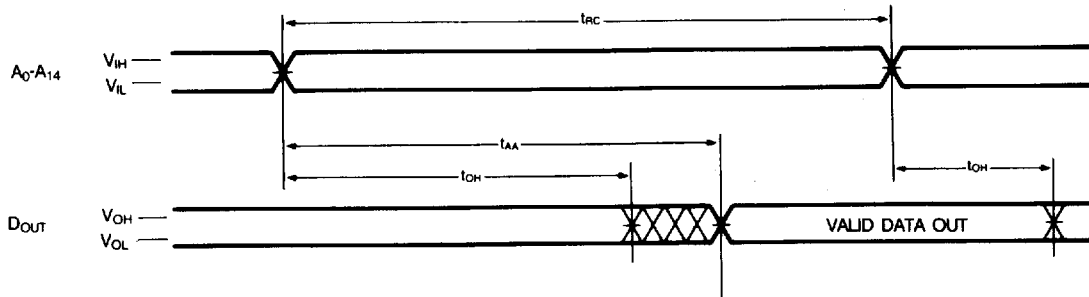
T-46-23-13

TIMING DIAGRAMS

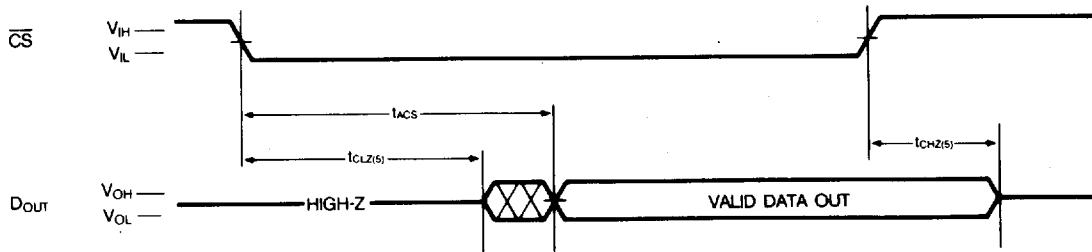
READ CYCLE 1⁽¹⁾



READ CYCLE 2^(1, 2, 4)



READ CYCLE 3^(1, 3, 4)



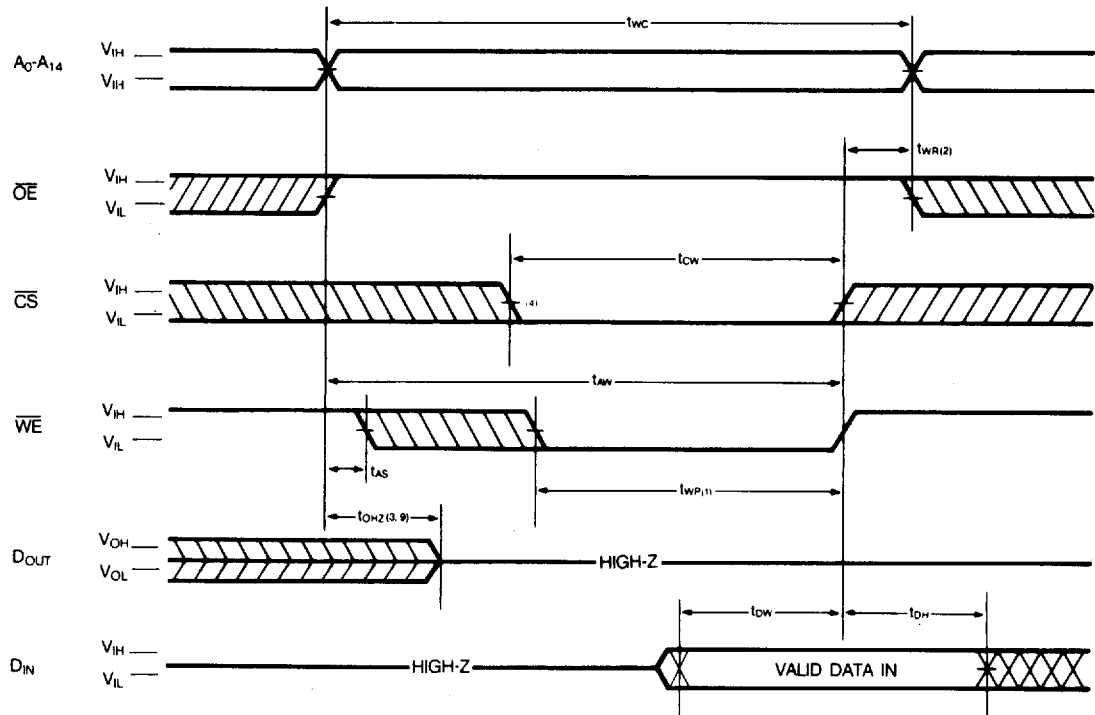
NOTES :

1. \overline{WE} is high for Read Cycle.
2. Device is continuously selected, $\overline{CS}=V_{IL}$.
3. Addresses are valid prior to or coincident with \overline{CS} transition low.
4. $\overline{OE}=V_{IL}$.
5. Transition is measured $\pm 500\text{mV}$ from steady state. This parameter is sampled and not 100% tested.

HY62256A 32,768 × 8-Bit CMOS SRAM

T-46-23-13

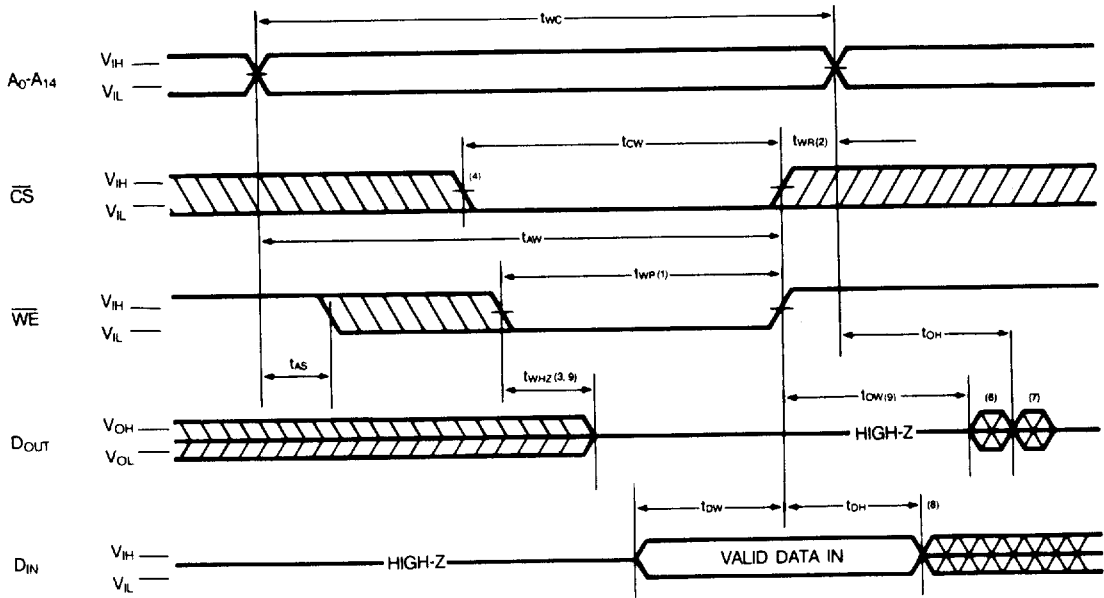
WRITE CYCLE 1



HY62256A 32,768×8-Bit CMOS SRAM

T-46-23-13

WRITE CYCLE 2⁽⁵⁾



NOTES :

1. A write occurs during the overlap (t_{wp}) of low \overline{CS} and low \overline{WE} .
2. t_{wr} is measured from the earlier of \overline{CS} or \overline{WE} going high at the end of write cycle.
3. During this period, I/O pins are in the output state so that the input signals of opposite phase to the outputs must not be applied.
4. If the \overline{CS} low transition occurs simultaneously with the \overline{WE} low transitions or after the \overline{WE} transition, outputs remain in a high impedance state.
5. \overline{OE} is continuously low ($\overline{OE} = V_{IL}$).
6. D_{OUT} is the same phase of write data of this write cycle.
7. D_{OUT} is the read data of next address.
8. If \overline{CS} is low during this period, I/O pins are in the output state. Then the data input signals of opposite phase to the outputs must not be applied to them.
9. Transition is measured $\pm 500mV$ from steady state. This parameter is sampled and not 100% tested.

HY62256A 32,768×8-Bit CMOS SRAM

T-46-23-13

DATA RETENTION CHARACTERISTICS⁽¹⁾

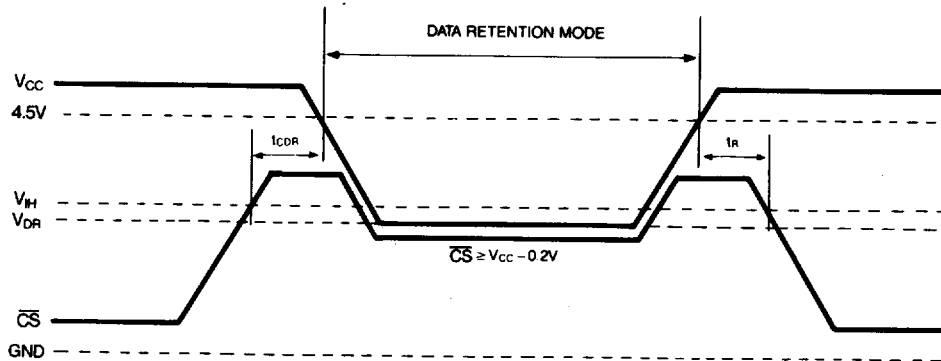
($V_A=0^\circ\text{C}$ to 70°C)

| SYMBOL | PARAMETER | TEST CONDITIONS | MIN. | TYP. | MAX. | UNIT | |
|------------|--------------------------------------|--|----------------|------|------|-------------------|---------------|
| V_{DR} | Data Retention Supply Voltage | $V_{IN}=0$ to V_{CC} , $\overline{CS} \geq V_{CC}-0.2V$ | 2.0 | - | - | V | |
| I_{CCDR} | Data Retention Current | $V_{CC}=3.0V$, $V_{IN}=0$ to V_{CC} , $\overline{CS} \geq V_{CC}-0.2V$ | L | - | 2 | 50 | μA |
| | | | LL | - | 2 | 20 ⁽²⁾ | μA |
| t_{CDR} | Chip Deselect to Data Retention Time | See Data Retention Timing Diagram | 0 | - | - | ns | |
| t_R | Operating Recovery Time | | $t_{RC}^{(3)}$ | - | - | ns | |

NOTES :

1. These characteristics are guaranteed for L and LL-version.
2. $3\mu\text{A}$ max. at $T_A=0^\circ\text{C}$ to 40°C
3. t_{RC} =Read Cycle Time

DATA RETENTION TIMING DIAGRAM

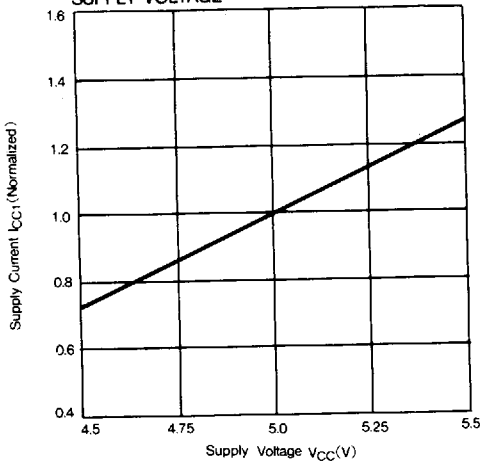


HY62256A 32,768×8-Bit CMOS SRAM

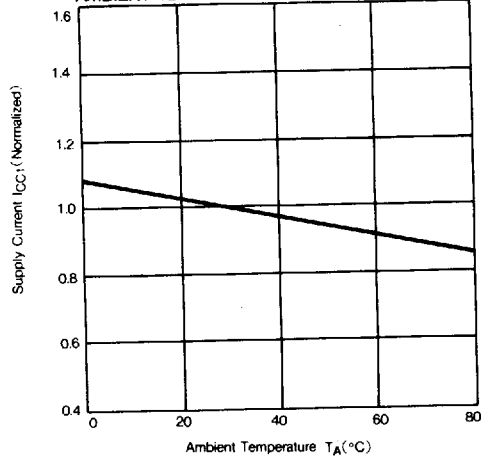
T-46-23-13

ELECTRICAL CHARACTERISTIC CURVES
($V_{CC}=5V$, $T_A=25^\circ C$, unless otherwise noted)

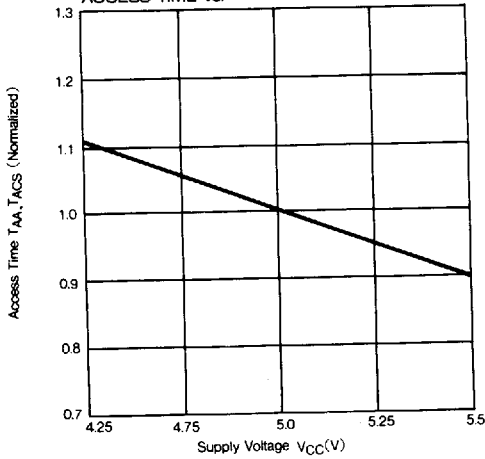
SUPPLY CURRENT vs. SUPPLY VOLTAGE



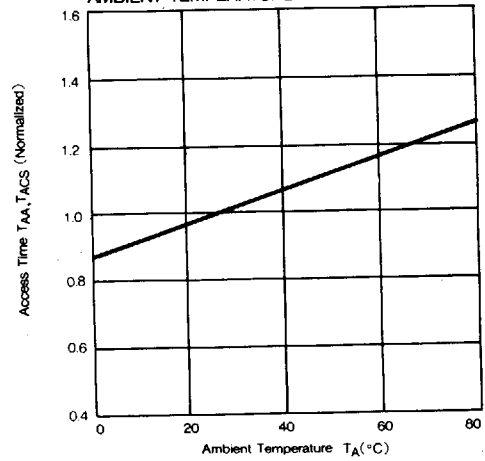
SUPPLY CURRENT vs. AMBIENT TEMPERATURE



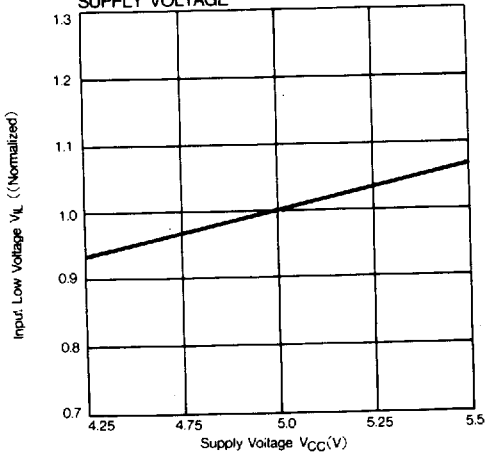
SUPPLY VOLTAGE ACCESS TIME vs.



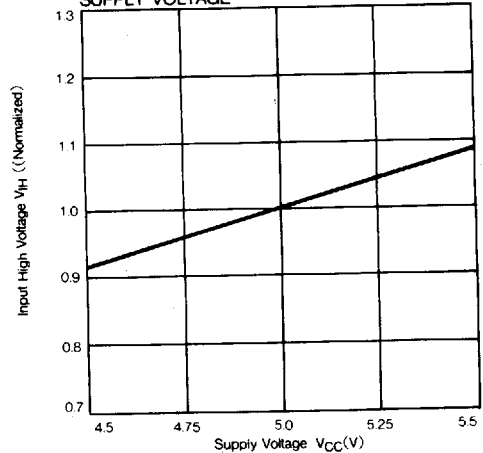
ACCESS TIME vs. AMBIENT TEMPERATURE



INPUT LOW VOLTAGE vs. SUPPLY VOLTAGE

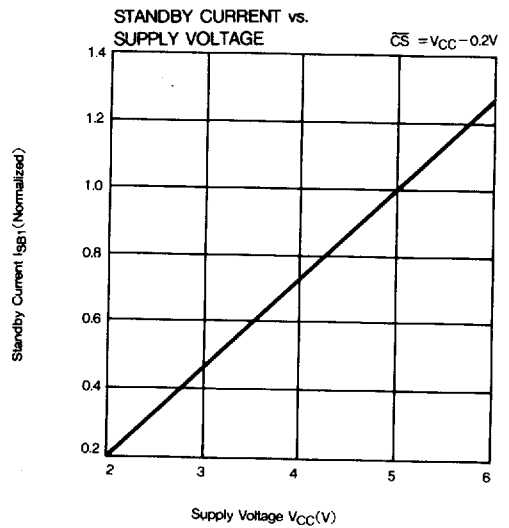
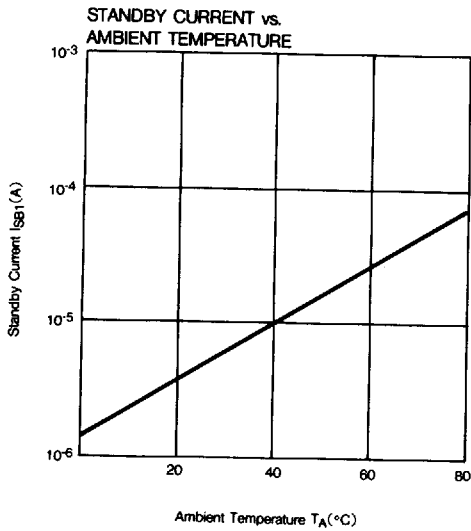
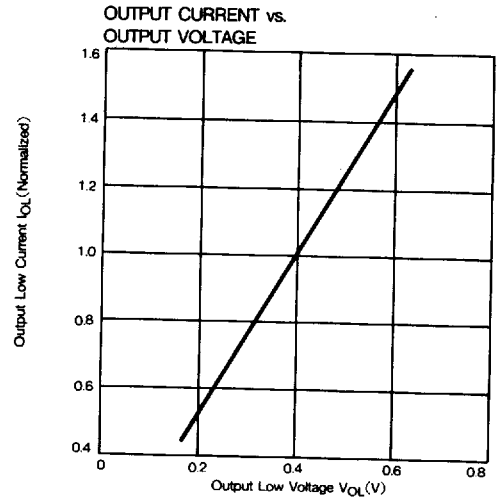
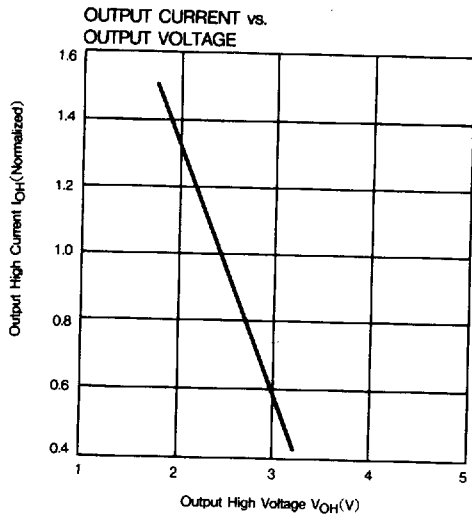


INPUT HIGH VOLTAGE vs. SUPPLY VOLTAGE



HY62256A 32,768×8-Bit CMOS SRAM

T-46-23-13

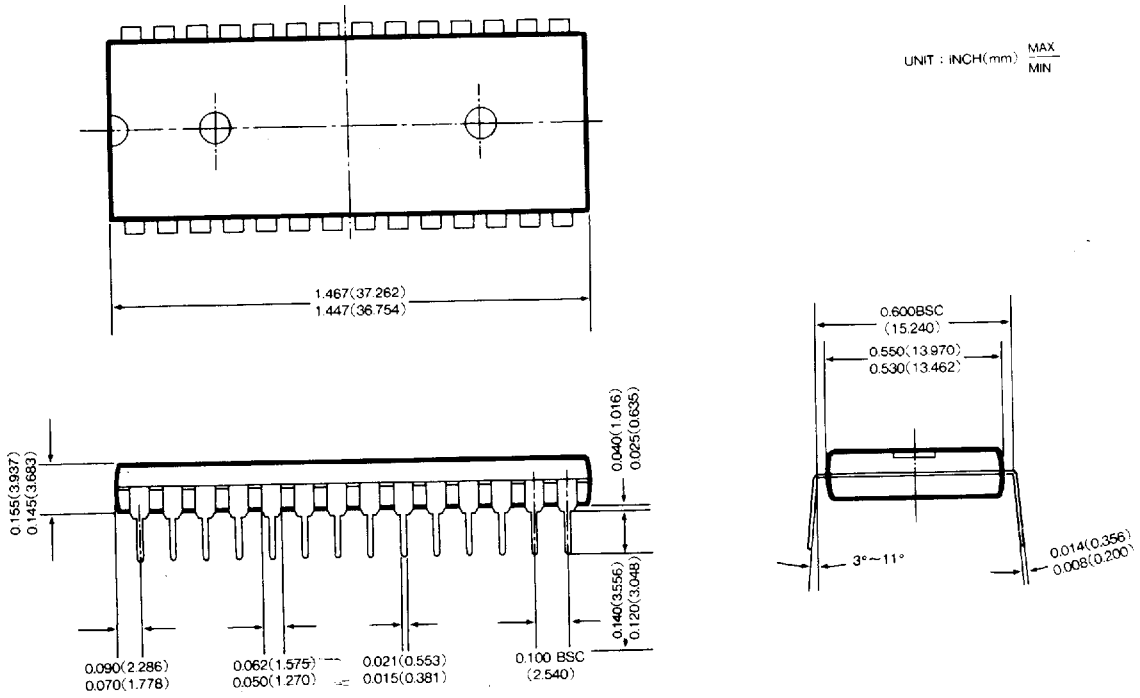


HY62256A 32,768×8-Bit CMOS SRAM

T-46-23-13

PACKAGE INFORMATION

- 28 PIN PLASTIC DUAL IN LINE PACKAGE-600MIL



- 28 PIN SMALL OUTLINE PACKAGE-330MIL

