I C T INC
, INC.

Preliminary Information

T-46-19-07

PEEL™18CV8L-25
CMOS Programmable Electrically Erasable Logic Device

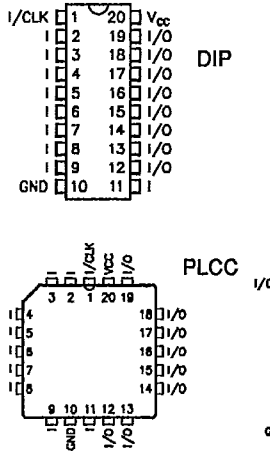
Features

- **Advanced CMOS EEPROM Technology**
- **Low Power Consumption**
  - 22mA at 25MHz
- **High Performance**
  - t_{PD} = 25ns, fmax=33.3MHz
- **EE Instant Reprogrammability**
  - 100% factory tested
  - Cost-effective windowless package
  - Erases and programs in seconds
  - Adds convenience, reduces field retrofit and development costs
- **Foolproof Design Security**
  - Prevents unauthorized reading or copying of design
- **Architectural Flexibility**
  - 74 product term x 36 input array
  - Up to 18 inputs and 8 I/O pins
  - Independent configurable I/O macro cells
  - Synchronous preset, asynchronous clear
  - Independent output enables
- **Application Versatility**
  - Replaces SSI/MSI logic
  - Emulates bipolar PAL® devices, GAL® devices, and EPLDs
  - Simplifies inventory control
  - Allows new design possibilities
- **Development/Programmer Support**
  - Third party software and programmers
  - ICT PEEL Development System and Software

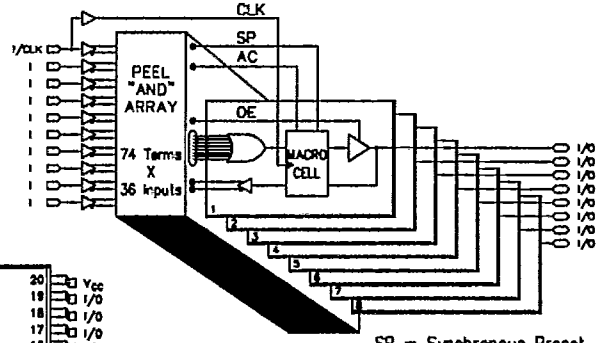
General Description

The ICT PEEL18CV8L-25 is a CMOS Programmable Electrically Erasable Logic device that provides a high-performance, low-power, reprogrammable, and architecturally flexible alternative to early-generation programmable logic devices (PLDs). Designed in advanced CMOS EEPROM technology, the performance of the PEEL18CV8L-25 rivals speed parameters of bipolar PLDs with a dramatic reduction in power consumption. EE reprogrammability simplifies inventory management, reduces development and field retrofit costs, enhances testability to ensure 100% field programmability and function, while allowing for low-cost "windowless" packaging in a 20-pin, 300-mil DIP. The PEEL18CV8L-25's flexible architecture allows the device to replace SSI/MSI logic circuitry. ICT's JEDEC file translator allows the PEEL18CV8L-25 to replace existing 20-pin PLDs without the need to rework the existing design. Development and programming support for the PEEL18CV8L-25 is provided by popular third-party PC-based development tools and programmers from third-party manufacturers. ICT also offers a free design software package and a low-cost development system.

Pin Configuration (Figure 1)



Block Diagram (Figure 2)



SP = Synchronous Preset
AC = Asynchronous Clear
OE = Output Enable

Absolute Maximum Ratings

Exposure to absolute maximum ratings over extended periods of time may affect device reliability. Exceeding absolute maximum ratings may cause permanent damage

Symbol	Parameter	Conditions	Rating	Unit
V_{CC}	Supply Voltage	Relative to GND	− 0.5 to + 7.0	V
V_I, V_O	Voltage Applied to Any Pin	Relative to GND [1]	− 0.5 to V_{CC} + 0.6	V
I_O	Output Current	Per pin (I_{OL}, I_{OH})	± 25	mA
T_{ST}	Storage Temperature		− 65 to+150	°C
T_{LT}	Lead Temperature	Soldering 10 seconds	+ 300	°C

Operating Ranges[2]

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	Supply Voltage	Commercial	4.75	5.25	V
		Industrial	4.5	5.5	V
T_A	Ambient Temperature	Commercial	0	+ 70	°C
		Industrial	− 40	+ 85	°C
T_R	Clock Rise Time	See note 4		250	ns
T_F	Clock Fall Time	See note 4		250	ns
T_{RVCC}	V_{CC} Rise Time	See note 4		250	ms

D.C. Electrical Characteristics

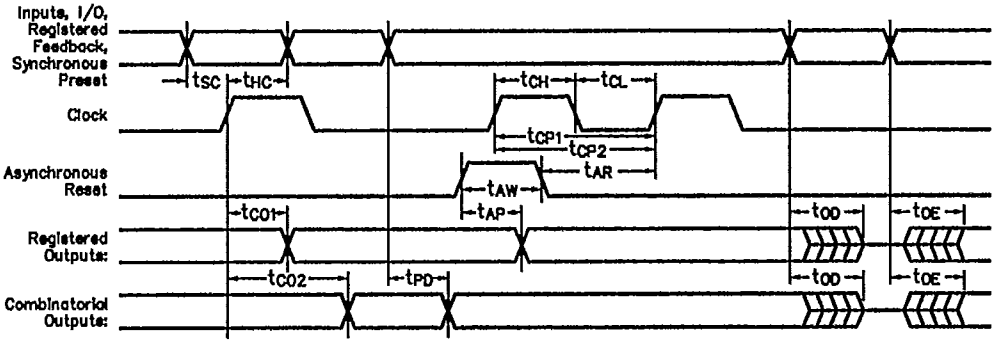
Over the operating range

Symbol	Parameter	Conditions	Min	Max	Unit
V_{OH}	Output HIGH Voltage - TTL	V_{CC} = Min, I_{OH} = − 4.0mA	2.4		V
V_{OHC}	Output HIGH Voltage-CMOS	V_{CC} = Min, I_{OH} = −10µA	V_{CC} − 0.1		V
V_{OL}	Output LOW Voltage - TTL	V_{CC} = Min, I_{OL} = 16mA		0.45	V
V_{OLC}	Output LOW Voltage-CMOS	V_{CC} = Min, I_{OL} = 10µA		0.1	V
V_{IH}	Input HIGH Level		2.0	V_{CC} + 0.3	V
V_{IL}	Input LOW Level		− 0.3	0.8	V
I_{IL}	Input Leakage Current	V_{CC} = Max, GND ≤ V_{IN} ≤ V_{CC}		±10	µA
I_{OZ}	Output Leakage Current	I/O = High-Z, GND ≤ V_O ≤ V_{CC}		±10	µA
I_{SC}	Output Short Circuit Current	V_{CC}=5V, V_O=0.5V[9]	− 30	− 100	mA
I_{CC}[1]	V_{CC} Current	V_{IN} = 0V or 3V[5,10] f = 25MHz All outputs disabled		22	mA
C_{IN}[7]	Input Capacitance	T_A = 25°C, V_{CC} = 5.0V @ f = 1MHz		6	pF
C_{OUT}[7]	Output Capacitance			12	pF

A.C. Electrical Characteristics Over the Operating Range[8,11]

Symbol	Parameter	18CV8L-25		Unit
		Min	Max	
t_{PD}	Input or I/O to non-registered output		25	nS
t_{OE}	Input or I/O to output enable[6]		25	nS
t_{OD}	Input or I/O to output disable[6]		25	nS
t_{CO1}	Clock to output		12	nS
t_{CO2}	Clock to combinatorial output delay via internal registered feedback		35	nS
t_{CF}	Clock to feedback		10	nS
t_{SC}	Input or feedback setup to clock	15		nS
t_{HC}	Input hold after clock	0		nS
t_{CL},t_{CH}	Clock width - clk low time, clk high time [4]	9		nS
t_{CP}	Min clock period External (t_{SC} + t_{CO1})	27		nS
f_{max1}	Max clock freq. - Internal Feedback	40		MHz
f_{max2}	Max Clock freq. External (1/t_{CP})	37		nS
f_{max3}	Max clock freq. No feedback (1/t_{CL} + t_{CH})	55.5		MHz
t_{AW}	Asynchronous clear pulse width	25		nS
t_{AP}	Input to asynchronous clear		25	nS
t_{AR}	Asynchronous Reset Recovery Time		20	nS
t_{RESET}	Power-on reset time for registers in clear state[4]		5	µS

Switching Waveforms



1. Minimum DC input is -0.5V, however inputs may undershoot to -2.0V for periods less than 20ns
2. Contact ICT for other operating ranges.
3. V_I and V_O are not specified for program/verify operation.
4. Test points for Clock and V_{CC} in t_R, t_F, t_{CL}, t_{CH}, and t_{RESET} are referenced at 10% and 90% levels.
5. I/O pins are 0V or 3V.
6. t_{OE} is measured from input transition to $V_{REF} \pm 0.1V$, t_{OD} is measured from input transition to V_{OH}-0.1V or V_{OL}+0.1V; $V_{REF} = V_L$ see test loads at the end of this section.
7. Capacitance are tested on a sample basis.
8. Test conditions assume: signal transition times of 5ns or less from the 10% and 90% points, timing reference levels of 1.5V (unless otherwise specified).
9. Test one output at a time for a duration less than 1 second.
10. ICC for a typical application. This parameter is tested with the device programmed as an 8-bit counter.
11. PEEL Device test loads are specified at the end of this section.