TSS463B
Serial VAN Data Link Controller

ATMEL P/N : TSS463B-TERA

PPAP Submission

Date: 2003 October
Supplier: Atmel Nantes SA

Address: La Chantrerie
BP 70602
44306 NANTES Cedex 3
France
Tel : 33(0) 2 40 18 18 18
Fax : 33(0) 2 40 18 19 20

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Revision history

Rev	Issue	Modification Notice	Applicable from
0	2003 March	Initial release (preliminary document)	2003 April
1	2003 June	Initial release (revised document)	2003 June
2	2003 October	Initial release (revised document) - Add of TSS463B rev 4 reliability assessment	2003 October
3	2003 October	Initial release (revised document) - Add of reliability calculation	2003 October

PPAP Checklist

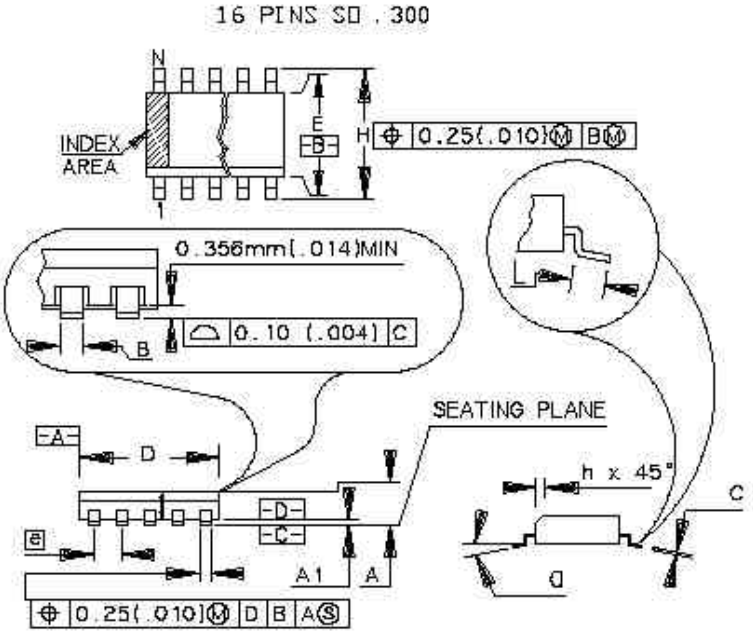
Requirements	Included
Table of contents	yes
PPAP Checklist	yes
1. Design Records	yes
2. Engineering Change Documents	yes
3. Engineering Approval	yes
4. Design FMEA	Project risk analysis
5. Process Flow Diagrams	yes
6. Process FMEA	yes
7. Dimensional Results	Not Applicable
8. Records of Material / Performance Test Results 8.1 Material Test Records 8.2 Performance Test Records	 Not applicable to IC Yes
9. Initial Process Study	Yes
10. Measurement System Analysis Study	Yes
11. Qualified Laboratory Documentation	Yes
12. Control Plan	Yes
13. Part Submission Warrant (PSW)	Yes
14. Appearance Approval Report	Not applicable to IC
15. Bulk Material Requirements Checklist	Not applicable to IC
16. Sample Production Parts	To be ordered separately
17. Master Sample	Not attached
18. Checking Aids	Not Applicable
19. Customer Specific Requirements	Not attached

1 Design Records

1.1 Product Specification

Please refer to ATMEL's Data Sheet: TSS463B VAN Data Link Controller with serial interface
http://www.atmel.com/

1.2 Package Outline



	MM		INCH	
A	2.35	2.65	.093	.104
A1	0.10	0.30	.004	.012
B	0.35	0.49	.014	.019
C	0.23	0.32	.009	.013
D	10.10	10.50	.398	.413
E	7.40	7.60	.291	.299
e	1.27	BSC	.050	BSC
H	10.00	10.65	.394	.419
h	0.25	0.75	.010	.029
L	0.40	1.27	.016	.050
N	16		16	
α	0°		8°	

PACKAGE CODE : N07 - N08
INTERNAL CODE : TE
ATMEL NANTES
REV : F DATE : 03-09-98

2 Engineering Change Documents

2.1 CDC Certificate of Design, Construction and Qualification

2.1.1 General Product Information

Product Name:	TSS463B
Function:	VAN Data Link Controller
Wafer Process:	CMOS 0.5um
Package Type:	SO-L.300 16 leads

Locations:

Process Development	Atmel Nantes , France
Product Development	Atmel Nantes , France
Wafer Plant	Atmel Nantes , France
QC Responsibility	Atmel Nantes, France
Probe Test	Atmel Nantes , France
Assembly	ASE Chung Li, Taiwan CHIPPAC, China AMKOR, Korea
Final Test	TSTI Philippines
Lot Release	Atmel Nantes, France
Shipment Control	Global Logistic Center, Philippines
Quality Assurance	Atmel Nantes, France
Reliability Testing	Atmel Nantes, France
Failure Analysis	Atmel Nantes, France

2.1.2 Process Technology Information

Process Type (Name):	Z92 (SCMOS3 : 0.5um Logic CMOS technology)
Base Material:	Bulk silicon
Wafer Thickness (final)	475µm
Wafer Diameter	150 mm
Number Of Masks	14
Gate Oxide (Logic transistors)	
Material	Silicon Dioxide
Thickness	110 A

Polysilicon

Number of Layers	1
Thickness	2000A

Metal

Number of Layers	3
Material	AlCu
Layer 1 Thickness	5150A
Layer 2 Thickness	5150A
Layer 3 Thickness	7650A

Passivation

Material	SiO2 / Nitride
Thickness	2600A / 6400A

2.2 Product Design

2.2.1 Product Design Information

Die Size	2200µm * 2790 µm (6.14mm^2)
Pad Size Opening	100µm * 100µm
Logic Effective Channel Length	0.5µm
Gate Poly Width (min.)	0.50µm
Gate Poly Spacing (min.)	0.60µm
Metal 1 Width	0.60µm
Metal 1 Spacing	0.70µm
Metal 2 Width	0.80µm
Metal 2 Spacing	0.70µm
Metal 3 Width	0.80µm
Metal 3 Spacing	0.70µm
Contact size	0.60µm
Via 1 size	0.60µm
Via 2 size	0.60µm

2.2.2 Product Design Validation

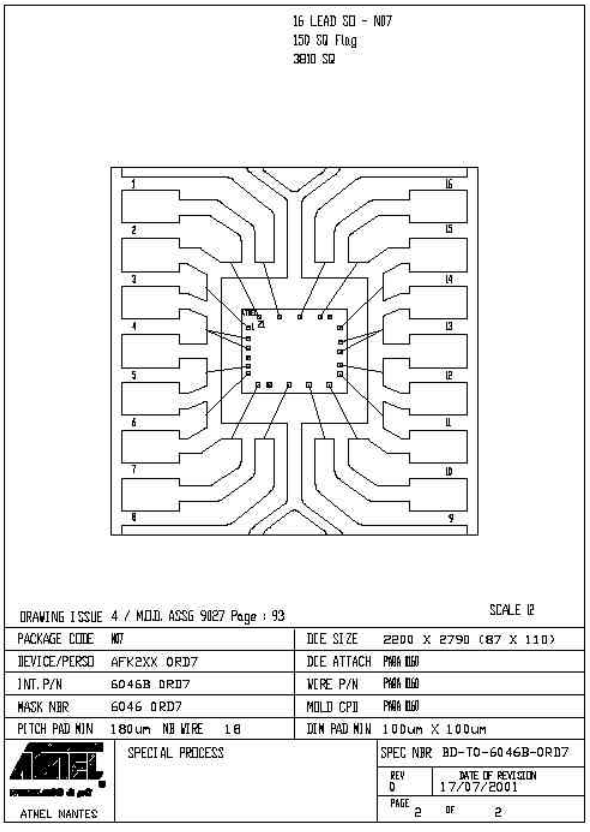
Design validation done according to Atmel Nantes development procedure and documented in the following documents:

VAN protocol assessment	DASSAULT Test Plan Results TSS463B Rev4 ATD-TS-GU-R001 – October 2002 Laurentiu BIRSAN
Third Party Application assessment	VAN Device TSS463B NSI Test Report DCL-MUX-0077 /V1.0 Jacques TELLIER
EMC Evaluation	TSS463B Dynamic Current Analysis APP/LAB/JLL/01/67-0.2 Jean Luc LEVANT

2.2.3 Package Technology Information

Package weight	0.43 g
Chip separation method	Sawing
Lead frame	
Material	Cu
Thickness	10 mils
Size	270*270 mils^2
Lead plating	Electroplated Sn/Pb 85/15
Die attach	
Material	Silver epoxy
Type	Ablestick 84-1 LMISR4
Wire bonding	
Material	Au
Diameter	1.0 mil
Method	Thermosonic
Molding	
Material	NITTO MP8000AN
Flammability rating	UL94V-0
Marking	
Method	Printed ink (top) and Laser (back)
Drawing example	Atmel TSS463B-TERA YYMM Zxxxxxxx

Bonding Diagram



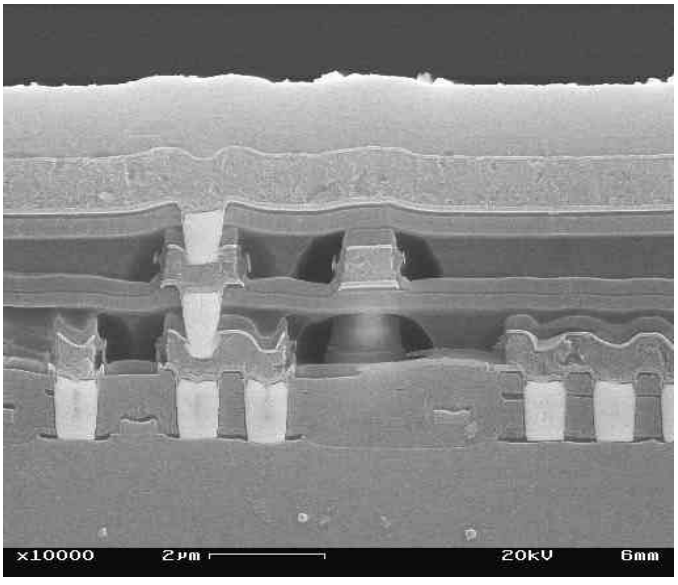
2.2.4 Packing Delivery Information

Dry packing	No
Tube packed	
Primary	Tube
Material	Antistatic PVC
Number per unit	36
Secondary	Box
Material	Cardboard
Number per unit	1692
Labeling (minimum)	Device type, quantity, Date code, Production code
Bar coding	Code 39 to EIA-556-A
Reel packed	
Primary	Reel
Material	
Carrier tape	Conductive black polystyrene
Cover tape	Antistatic film
Number per unit	1500
Secondary	Box
Number per unit	1
Labeling (minimum)	Device type, quantity, Date code, Production code

2.2.5 Final Test Information

Probe equipment	NEXTEST Maverick
Probe temperature	125° C
Test equipment	NEXTEST Maverick
Test temperature	25° C, 125° C

2.2.6 Device Cross Section



2.3 Qualification and Change Procedure

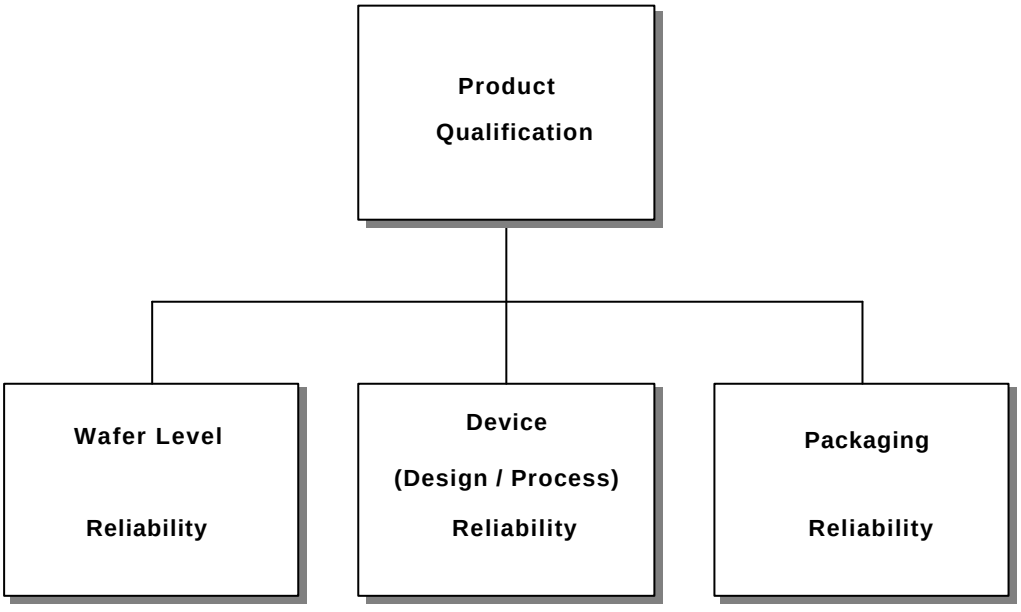
2.3.1 Qualification methodology

All product qualifications are split into three distinct steps as shown below. Before a product is released for use, successful qualification testing are required at wafer, device and package level.

Wafer Level Reliability consists in testing individually basic process modules regarding their well known potential limitations (Electromigration, Hot Carriers Injection, Oxide Breakdown, NVM Data Retention). Each test is performed using a dedicated wafer process structure.

Device reliability is covering either dice design and processing aspects. The tests are performed on device under qualification, and generic data may also be considered for reliability calculation.

For each package type proposed in the Datasheet, it is verified that qualification data are available. If not qualification tests are carried out for the new package types. At least one package type is selected to verify packaging reliability of the device under qualification.



2.3.2 Change Procedure

All changes are controlled by ECN (Engineering Change Notice). Major changes are notified to customers using products affected by the change.

Major changes are defined as changes which may affect the electrical and/or mechanical product specification. The following checklist provides the minimum list of items to be considered.

1	**General Changes**
1-1	Manufacturing line
1-2	Sequence of fabrication process cycle
1-3	Material type
1-4	Electrical parameter
1-5	External physical dimension
1-6	Die size

2	**Changes Specific to Wafer Fabrication**
2-1	Doping method
2-2	Gate oxide formation method
2-3	Equipment change
2-4	Layer Thickness
2-5	Module dimensions

3	**Changes Specific to Assembly**
3-1	Sawing method
3-2	Die attach method
3-3	Wiring method
3-4	Molding process
3-5	Lead finish / MSL classification

4	**Changes Specific to Test**
4-1	Specification limit
4-2	Test coverage reduction
4-2	Product identification
4-3	Final conditioning

2.3.3 Qualification test methods

General Requirements for Plastic Encapsulated CMOS Ics.

Standard	Test Description	Acceptance
MIL-STD 883 Method 1005	**Electrical Life Test (Early Failure Rate)** 48 hours 140°C	0/800 - 48h
MIL-STD 883 Method 1005	**Electrical Life Test (Latent Failure Rate)** 1000 hours 140°C Dynamic or Static	0/77 - 1000h
MIL-STD 883 Method 3015.7	**Electrostatic Discharge HBM** +/-2000v 1.5kOhm/100pF/3 pulses	0/3 per level
JEDEC 78	**Latch up** 50mW power injection, 50% overvoltage @125°C	0/5 per stress
AEC Q100 Method 005	**NVM Endurance** Program Erase Cycles 125°C	0/77 - 100kc
AEC Q100 Method 005	**NVM Data Retention** High Temperature Storage 165°C	0/77 - 1000h
MIL-STD 883 Method 1010	**Temperature Cycling** 1000 cycles –65°C/150°C air/air	0/77 - 500c
EIA JESD22-A110	**Autoclave** 96 hours 130°C/85%RH	0/77 – 96h
EIA JESD22-A101	**85/85 Humidity Test** 1000 hours 85°C/85%RH	0/77 - 1000h
EIA JESD22-A110	**HAST** 96 hours 130°C/85%RH/biased	0/50 - 96h
EIA JESD20	**Preconditioning** Soldering Stress 220°C/235°c/3 times	0/11 per class
MIL-STD 883 Method 2003	**Solderability**	0/3
MIL-STD 883 Method 2015	**Marking Permanency**	0/5

3 Engineering Approval

TSS463B is qualified since 2003 March

Released to production review was done in 2003 May

Release to Production is approved by:

- Head of Technical Center
- Project Leader
- Product Engineering
- Operation Back-end
- Operation Front-end
- Quality Management
- Marketing
- Business Planning

4 Design FMEA

Project Risk Analysis has been initiated at Feasibility stage and followed under Project Leader responsibility, all over project development stages.

Project Risk Analysis report may be consulted in Atmel Nantes upon request.

5 Process Flow Diagrams

5.1 Wafer Processing

1. Incoming inspection of silicon wafers
2. Locos (Z92) Isolation
3. MOS N-Well implants and N Well diffusion
4. MOS P-Well Implants
5. MOS Gate oxidation
6. Polysilicon deposition and MOS gate definition
7. MOS Implants with Spacer definition
8. Salicide Hard mask definition
9. Salicide module
10. ILD deposition and SOG planarization
11. Contact etching and Plug1 filling
12. Metal 1 deposition and etching
13. IMD1 and REB planarization
14. Via1 etching and Plug2 filling
15. Metal 2 deposition and etching
16. IMD2 and REB planarization
17. Via2 etching and Plug3 filling

18. Metal 3 deposition and etching
19. Passivation deposition and Pad etching
20. E-Test
21. Back grinding
22. Wafer sort

5.2 Assembly

1. Wafer mount
2. Wafer saw
3. First optical
4. Die bonding
5. Wire bonding
6. Molding
7. Solder plating
8. Top marking
9. Trim and form
10. Final visual inspection

5.3 Test and Packing

1. Room temperature initial test
2. Final quality checks
3. Packing

6 Process FMEA

Process FMEA for 0.5um Z92 may be consulted in Atmel Nantes upon request.

7 Dimentional Results

SO-L.300 16 leads package comply with JEDEC standard outline.

Package dimensions were checked during Package Qualification.

8 Performance Test Results

8.1 Qualification Results

8.1.1 Wafer Process Qualification

ATMEL 0.5µm SCMOS3 wafer process is qualified since 1997, September.

8.1.2 Package Qualification

Package qualification measurements carried out on VAN DLC devices are detailed in the table below:

Lots	Device Type	Test Description	Step	Result	Comment
Z40807C	TSS463B SO-L.300 16 AMKOR K	85/85 Humidity	500h 1000h	0/77 0/77	Post preconditioning level1
		Thermal Cycles	500c 1000c	0/77 0/5 0/5 0/72	Post preconditioning level1 Ball shear cpk:1.70 (30 pads) Wire pull cpk:2.35 (30 wires)
		HAST after Thermal Shocks	96h	0/77	Post preconditioning level1
		High Temperature Storage 165°C	500h 1000h	0/77 0/77	
		Moisture sensitivity JESD20 – level1	CSAM Elect	0/11 0/231	
Z41393J	TSS461E SO-L.300 24 AMKOR K	85/85 Humidity	500h 1000h	0/50 0/50	Post preconditioning level1
		Thermal Cycles	500c 1000c	0/50 0/72	Post preconditioning level1
		HAST after Thermal Shocks	96h	0/77	Post preconditioning level1
		High Temperature Storage 165°C	500h 1000h	0/50 0/50	
		Moisture sensitivity JESD20 – level1	CSAM Elect	0/11 0/231	
Z45925A (Note 1)	TSS463B rev4 SO-L.300 16 ASE CL	85/85 Humidity	500h 1000h	0/77 0/77	Post preconditioning level1
		Thermal Cycles	500c 1000c	0/77 0/77	Post preconditioning level1 WP-Cpk= 1.67, BS-Cpk=1.89
		HAST after Thermal Shocks	96h	0/77	Post preconditioning level1
		Moisture sensitivity JESD20 – level1	CSAM Elect	0/11 0/231	
		High Temperature Storage 165°C	500h 1000h	0/77 0/77	

Additional assembly qualification reports are available under the following references:

- ASE Chung Li : QR0813 (2002/09/23)
- CHIPPAC China : QR0726 (2002/05/13)

8.1.3 Device Qualification

Device qualification is based upon HTOL results of 3 lots as detailed in the table below:

Lot	Device Type	Test Description	Step	Result	Comment
Z40807C	TSS463B SO-L.300 16 AMKOR K	EFR Dynamic Life Test 140°c/5.75v	48h	0/774	
		LFR Life Test 140°c/5.75v	500h 1000h	0/77 0/77	
Z41393J	TSS461E SO-L.300 24 AMKOR K	EFR Dynamic Life Test 140°c/5.75v	48h	0/795	
		LFR Life Test 140°c/5.75v	500h 1000h	0/77 0/77	
Z45925A (Note 1)	TSS463B rev4 SO-L.300 16 ASE CL	EFR Dynamic Life Test 140°c/5.75v	48h	0/800	
		LFR Life Test 140°c/5.75v	500h 1000h	0/100 0/100	

Note 1:

In this revision of the TSS463B PPAP, are reported the reliability results of the final production version of the circuit (Rev 4 design). The measurements have been carried out on lot Z45925A DC0327.

8.1.4 Failure Mechanisms and Corrective Actions

No failure mechanism reported in this document.

The table here below presents additional Reliability Monitor Data performed during the first quarter of 2003.

Lot	Device Type	Test Description	Step	Result	Comment
Z44574F	TSSIO16E SO-L.300 28 AMKOR K	EFR Dynamic Life Test 140°c/5.75v	48h	0/300	
		LFR Life Test 140°c/5.75v	500h 1000h	0/77 0/77	
		Moisture sensitivity JESD20 – level1	CSAM Elect	0/11 0/150	
		85/85 Humidity	500h 1000h	0/50	Post preconditioning level1 (Test in progress)
		Thermal Cycles	500c 1000c	0/50 0/50	Post preconditioning level1
		Autoclave post Thermal Shocks	96h	0/50	Post preconditioning level1

8.1.5 Electrical Distribution in Operating Life-Test

In order to assess the drift of product performance under HTOL stress 30 parts have been submitted to 1000 hours 140°c/5.75v aging. All specified AC and DC Parameters have been recorded prior (initial) and post stress (final) for the lot Z41521. The table below summarizes the results with total drift ratio and final Cpk.

No significant drift noticed after HTOL aging. Final Cpk values are higher than 1.33.

HTOL performance records for the rev 4 design (lot Z45925A) have been included in the table as well. The records do not indicate any change in the performance of the circuit.

Symbol	Parameter	Specification	Vcc (*)	Typical	Initial	Final	Drift (%)	Cpk	Z45925A
ICCSB	Static Consumption	50uA max	5.5V	**0.050**	**0.049**	**0.046**	**-6.1**	**>20**	**0.051**
ICCOP	Active Consumption	9 mA max	5.5V	**2.20**	**2.23**	**2.25**	**0.9**	**>20**	**2.24**
VIL CMOS	Input Low Level	1.5V min	4.5V	**1.51**	**1.51**	**1.54**	**2.0**	**1.6**	**1.63**
VIL1	XTAL 1 Low Level	1.5V min	4.5V	**1.66**	**1.70**	**1.69**	**0.6**	**3.4**	**1.70**
VIH CMOS	Input High Level	3.5V max	5.5V	**3.16**	**3.12**	**3.23**	**3.5**	**1.5**	**3.11**
VIH1	XTAL 1 In High Level	3.5V max	5.5V	**3.15**	**3.11**	**3.21**	**3.2**	**1.6**	**3.10**
VOL TXD	TXD Out Low Level	0.4V max	4.5V	**0.22**	**0.21**	**0.23**	**9.5**	**10.2**	**0.23**
VOL INTB	INTB Out Low Level	0.4V max	4.5V	**0.22**	**0.21**	**0.23**	**9.5**	**9.3**	**0.24**
VOH TXD	TXD Out High Level	2.4V min	4.5V	**4.1**	**4.0**	**4.0**	**0.0**	**3.7**	**4.0**
IIL RESET	RESET Low Leakage	78.5uA max	5.5V	**20.6**	**21.3**	**22.6**	**6.1**	**>20**	**20.8**
TCYC	Cycle Time SPI	250ns max	4.5V	**9.3**	**9.3**	**9.4**	**1.1**	**>20**	**9.3**
TW SCKH	Clock High Time	100ns max	4.5V	**3.41**	**3.41**	**3.47**	**1.8**	**>20**	**3.41**
TW SCKL	Clock Low Time	100ns max	4.5V	**5.9**	**5.9**	**5.9**	**0.0**	**>20**	**5.9**
TSU	Data Setup Time	40ns max	4.5V	**0.80**	**0.80**	**0.86**	**7.5**	**>20**	**0.79**
TH	Data Hold Time	40ns max	5.5V	**-0.52**	**-0.52**	**.052**	**0.0**	**>20**	**-0.52**
TV	Enable to Data Valid	60ns max	4.5V	**30.1**	**32.6**	**31.5**	**-3.4**	**7.5**	**31.6**

8.1.6 Reliability Calculation

Reliability calculation requires a large base of measurement data in prospect of targeting the objectives of Automotive Market. Therefore the data source is enlarged to 2003 records of digital 0.5um Nantes products.

	Sample size	Failures	Failure Rate	Projected Failure Rate	Unit
Early Life Failures	1.9E6	7	4	3	PPM
Latent Failures	2880E3	0	2	1	FIT

8.1.7 ESD Results (HBM) - MIL-STD 883 method 3015.7

Lot	Device Type	Test Description	Step	Result	Comment
Z40807C	TSS463B SO-L.300 16 AMKOR K	ESD HBM	2000v 3000v 4000v	0/3 0/3 0/3	Class 3 of MIL STD 883 Method 3015 (ESD0113)

8.1.8 Latch-up Results

Lot	Device Type	Test Description	Step	Result	Comment
Z40807C	TSS463B SO-L.300 16 AMKOR K	LATCH-UP Power Injection Over voltage	 50mw 10v	 0/5 0/5	 Latch-up free (min value: 180mW at 125°c)

8.2 Product Characterization

8.2.1 Characterization environment

Tester: Sentry 15

Lot: Z43525

Process: Z92

Perso Code: 0RD7 (design Rev 4)

Assy package: TE (SO-L.300 16 leads)

8.2.2 Corner lot's splits

In order to characterize the product with the maximum excursion of the process, corner run splits have been manufactured using :

- Variations on LeffP and LeffN
- Variations on VTP and VTN

The sample size is 3 parts per corner plus 6 parts in the group of typical values (Total 21 parts).

8.2.3 Results / Parameter capability

All specified AC and DC Parameters have been characterized for Rev 4 design version. They present Cpk values higher than 1.6. The comparison of Rev 1 and Rev 4 characteristics does not point out any difference.

Characterization results have been submitted to a detailed customer review (TSS463B Test Review) held in Nantes on 27/11/2001.

The next table provides the main product characteristics based upon Mask 6046 Rev 4 evaluation results.

All TSS463B AC parameters are reported in this table.

Symbol	Parameter	Specification (1)	Vcc (*)	Temp (*)	Average	Cpk
ICCSB	Static Consumption	50uA max	5.5V	125	2.9uA	9.6
ICCOP	Active Consumption	9 mA max	5.5V	-40	2.7mA	> 20
VIL CMOS	Input Low Level	1.5V min	4.5V	-40	1,6V	1.61
VIL1	XTAL 1 Low Level	1.5V min	4.5V	-40	1,7V	4.0
VIH CMOS	Input High Level	3.5V max	5.5V	-40	3.2V	5.7
VIH1	XTAL 1 In High Level	3.5V max	5.5V	-40	3.2V	4.7
VOL TXD	TXD Out Low Level	0.4V max	4.5V	125	0.22V	18.0
VOL INTB	INTB Out Low Level	0.4V max	4.5V	125	0.23V	12.3
VOH TXD	TXD Out High Level	2.4V min	4.5V	125	3.9V	> 20
IIL RESET	RESET Low Leakage	78.5uA max	5.5V	-40	26.5uA	> 20
TCYC	Cycle Time SPI	250ns max	4.5V	125	10ns	> 20
TW SCKH	Clock High Time	100ns max	4.5V	125	5.5ns	14.7
TW SCKL	Clock Low Time	100ns max	4.5V	125	5.9ns	>20
TSU	Data Setup Time	40ns max	4.5V	125	0.8ns	>20
TH	Data Hold Time	40ns max	5.5V	-40	-0.5ns	>20
TV	Enable to Data Valid	60ns max	4.5V	125	36.7ns	14.1

(*) worst case condition

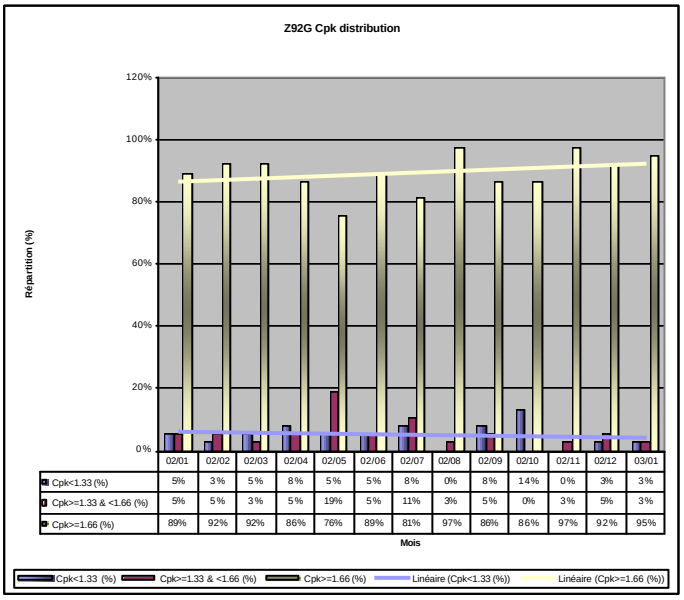
9 Initial Process Study

9.1 SCMOS3 process (Z92G)

Parameters controlled during Electrical Test :

NMOS/PMOS :junction Breakdown Voltage, Threshold voltage, electrical width & length, Thin oxide Breakdown Voltage, Sub-threshold current.
Sheet Resistance : N+, P+, WELL, PolyN, PolyP, Unsalicided Poly
Metal continuity / isolation: metal1, metal2, metal3
Contacts/ Vias1 & Vias2 resistance
Contacts Breakdown Voltage
Salicide isolation

Cpk history (Last update 23/01/2003) :



	02/01	02/02	02/03	02/04	02/05	02/06	02/07	02/08	02/09	02/10	02/11	02/12	03/01
Cpk<1.33 (%)	5%	3%	5%	8%	5%	5%	8%	0%	8%	14%	0%	3%	3%
Cpk>=1.33 & <1.66 (%)	5%	5%	3%	5%	19%	5%	11%	3%	5%	0%	3%	5%	3%
Cpk>=1.66 (%)	89%	92%	92%	86%	76%	89%	81%	97%	86%	86%	97%	92%	95%

10 Measurement System Analysis Study

Repeatability and Reproducibility tests are performed on all the manufacturing equipments.
Critical parameters and equipments are followed under SPC system. In addition Equipment performance is assessed by GRR and through regular maintenance activity.

11 Qualified Laboratory Documentation

Internal Lab – COMPLIANT QS-9000 3rd edition

	Scope
Application Lab	Check the functionality of products to customer applications
Calibration Lab	Standard Gage Calibration
Characterization Lab	Product and process characterization before completing industrialization
Chemical Lab	Incoming inspection on chemical products and process monitoring on DI water , gases
Environmental Lab	Product Reliability Testing
Technology Analysis Lab	Failure Analysis and Yield enhancement

12 Control Plan

Control plan is composed of the following:

- Wafer fab Control Plan for Z92G process
- Assembly Control Plan
- Test Control Plan

Front-end and Back-end operation control plans may be consulted in Atmel Nantes upon request.

Test Control Plan:

CONTROL PLAN

Prototype :	Pre-launch :		Production	X	Key Contacts /Phone	P.LECUYER					Date (Orig.) 24/03/2003		Date (Rev.) 24/03/2003		
Control Plan Number	TSS463B_TEST_FLOW														
Part Number /Latest Change Level	TSS463B-TERA				Core team	VANUATU / G.COIGNARD					Customer Engineering Approval /Date (if req'd)				
Part Name /Description	VAN DATALINK CONTROLLER WITH SERIAL INTERFACE				Supplier /Plant Appproval /Date	ECN and TRB approval					Customer Quality Approval /Date (if req'd)				
Supplier /Plant :	ATMEL MCU NANTES		Supplier Code RD7		Other Approval/Date (if req'd)						Other Approval/Date (if req'd)				

Part Process Number	Process name/operation description	Machine, device,jig,tools for Mfg	Characteristics			Special characteristics	Methods							Reaction Plan
			N°	Product	Process		Product/ Process Specification/ Tolerance Min	Max	Unit	Evaluation Measurement Technique	Sample Size	Freq.	Control Method	
1	E-TEST	KLA	360	KERF	PERFORMANCE	Y	0	2	SPEC	PROCESS TEST MODULE MEASUREMENT	5 x 5	100%	SPC	PAC
2	PROBE	NEXTEST MAVERICK	990C	WAFER	SORTING	N	-	0	SPEC	125°C DICE PROBING	100%	100%	Go / Nogo	PAC
3	WAFER SORT	POST PROBING YIELD VERIFICATION	IFA	WAFER	OUTLIERS SCREENING	N	-3 STD	-	avg Y	YIELD RECORDS VERIFICATION	100%	100%	Go / Nogo	PAC
4	FINAL TEST	NEXTEST MAVERICK	6000	FG	SORTING	N	-	0	SPEC	25°C FINAL TESTING	100%	100%	Go / Nogo	SSTQA
5	QA GATE	NEXTEST MAVERICK	6800	FG	CONTROL	N	-	0	SPEC	125°C ELECTRICAL CONTROL	200p	100%	AQL = 0,065	SSTQA
6	T&R INSPECTION	ST585	8000	FG	VISUAL EXAMINATION	N	-	4	mils	COPLANARITY AUTOMATIC INSPECTION	100%	100%	Go / Nogo	SSTQA

13 Part Submission Warrant

Part Name **TSS463B** Part Number **TSS463B-TERA**

Safety and/or Government Regulation ☐ Yes ☒ No Engineering Drawing Change Level _____ Dated _____

Additional Engineering Changes _____ Dated _____

Shown on Drawing No. _____ Purchase Order No. _____ Weight _____ kg

Checking Aid No. _____ Engineering Change Level _____ Dated _____

SUPPLIER MANUFACTURING INFORMATION

ATMEL Nantes SA
Supplier Name Supplier Code

La Chantrerie Route de Gachet BP 70602
Street Address

44306 Nantes Cedex 3 FRANCE
City/State/Postal Code

SUBMISSION INFORMATION

☐ Dimensional ☐ Materials/Functional ☐ Appearance

Customer Name/Division _____

Buyer/Buyer Code _____

Application _____

REASON FOR SUBMISSION

☐ Initial Submission
☒ Engineering Change(s)
☐ Tooling: Transfer, Replacement, Refurbishment, or additional
☐ Correction of Discrepancy
☐ Change to Optional Construction or Material
☐ Sub-Supplier or Material Source Change
☐ Change in Part Processing
☐ Parts Produced at Additional Location
☐ Other - please specify _____

REQUESTED SUBMISSION LEVEL (Check one)

☐ Level 1 - Warrant, Appearance Approval Report (for designated appearance items only).

☐ Level 2 - Warrant, Parts, Drawings, Inspection Results, Laboratory and Functional Results, Appearance Approval Report.

☒ Level 3 - At Customer Location - Warrant, Parts, Drawings, Inspection Results, Laboratory and Functional Results, Appearance Approval Report, Process Capability Results, Capability Study, Process Control Plan, Gage Study, FMEA.

☐ Level 4 - Per Level 3, but without parts.

☐ Level 5 - At Supplier Location - Warrant, Parts, Drawings, Inspection Results, Laboratory and Functional Results, Appearance Approval Report, Process Capability Results, Capability Study, Process Control Plan, Gage Study, FMEA.

SUBMISSION RESULTS

The results for ☒ dimensional measurements ☒ material and functional tests and ☒ appearance criteria and ☒ statistical process package meet all drawing and specification requirements: ☒ Yes ☐ No (If "No" - Explanation Required)

DECLARATION

I affirm that the samples represented by this warrant are representative of our parts and have been made to the applicable customer drawings and specifications and in the case of production samples, are made from specified materials on regular production tooling with no operations other than the regular production process. I have noted any deviations from this declaration below:

EXPLANATION/COMMENTS:

Print Name **Pascal LECUYER** Title **Products Qualification Manager** Phone No. **33 2 4018 1773**

Supplier Authorized Signature _____ Date _____

FOR CUSTOMER USE ONLY

Part Disposition ☐ Approved ☐ Rejected ☐ Other _____

Customer Name _____ Customer Signature _____ Date _____

14 Appearance Approval Report

Not Applicable for IC

15 Bulk Material Requirements

Not Applicable for IC

16 Sample Production Parts

Not attached, delivered previously

17 Master Sample

Not attached.

18 Checking Aids

Not applicable

19 Customer-Specific Requirements

Not attached.