0.8 GHz–2.7 GHz Direct Conversion Quadrature Demodulator

AD8347*

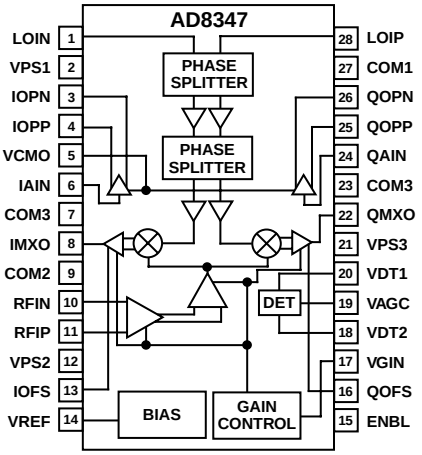
FEATURES

Integrated RF and Baseband AGC Amplifiers
Quadrature Phase Accuracy 1° Typ
I/Q Amplitude Balance 0.3 dB Typ
Third Order Intercept (IIP3) +11.5 dBm @ Min Gain
Noise Figure 11 dB @ Max Gain
AGC Range 69.5 dB
Baseband Level Control Circuit
Low LO Drive –8 dBm
ADC Compatible I/Q Outputs
Single Supply 2.7 V–5.5 V
Power-Down Mode
Package 28-Lead TSSOP

APPLICATIONS

Cellular Basestations
Radio Links
Wireless Local Loop
IF Broadband Demodulator
RF Instrumentation
Satellite Modems

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The AD8347 is a broadband Direct Quadrature Demodulator with RF and baseband Automatic Gain Control (AGC) amplifiers. It is suitable for use in many communications receivers, performing Quadrature demodulation directly to baseband frequencies. The input frequency range is 800 MHz to 2.7 GHz. The outputs can be connected directly to popular A-to-D converters such as the AD9201 and AD9283.

The RF input signal goes through two stages of variable gain amplifiers prior to two Gilbert-cell Mixers. The LO quadrature phase splitter employs polyphase filters to achieve high quadrature accuracy and amplitude balance over the entire operating frequency range. Separate I & Q channel variable-gain amplifiers follow the baseband outputs of the mixers. The RF and baseband amplifiers together provide 69.5 dB of gain control. A precision control circuit sets the Linear-in-dB RF gain response to the gain control voltage.

Baseband level detectors are included for use in an AGC loop to maintain the output level. The demodulator dc offsets are minimized by an internal loop, whose time constant is controlled by external capacitor values. The offset control can also be overridden by forcing an external voltage at the offset nulling pins.

The baseband variable gain amplifier outputs are brought off-chip for filtering before final amplification. By inserting a channel selection filter before each output amplifier high-level out-of-channel interferers can be eliminated. Additional internal circuitry also allows the user to set the dc common-mode level at the baseband outputs.

*U.S. Patents Issued and Pending

REV. 0

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781/329-4700 **www.analog.com**
Fax: 781/326-8703

AD8347—SPECIFICATIONS

(V_S = 5 V; T_A = 25°C; F_{LO} = 1.9 GHz; V_{VCMO} = 1 V; F_{RF} = 1.905 GHz; P_{LO} = –8 dBm, R_{LOAD} = 10 kΩ, dBm with respect to 50 Ω, unless otherwise noted.)

Parameter	Conditions	Min	Typ	Max	Unit
OPERATING CONDITIONS					
LO/RF Frequency Range		0.8		2.7	GHz
LO Input Level		–10		0	dBm
VGIN Input Level		0.2		1.2	V
V_{SUPPLY} (V_S)		2.7		5.5	V
Temperature Range		–40		+85	°C
RF AMPLIFIER/DEMODULATOR	From RFIP/RFIN to IMXO and QMXO (IMXO/QMXO Load >1 kΩ)				
AGC Gain Range			69.5		dB
Conversion Gain (Max)	V_{VGIN} = 0.2 V (Max Gain)		39.5		dB
Conversion Gain (Min)	V_{VGIN} = 1.2 V (Min Gain)		–30		dB
Gain Linearity	V_{VGIN} = 0.3 V to 1 V		±2		dB
Gain Flatness	F_{LO} = 0.8 GHz – 2.7 GHz, F_{BB} = 1 MHz		0.7		dB p-p
Input P1 dB	V_{VGIN} = 0.2 V		–30		dBm
	V_{VGIN} = 1.2 V		–2		dBm
Third Order Input Intercept (IIP3)	F_{RF1} = 1.905 GHz, F_{RF2} = 1.906 GHz, –10 dBm Each Tone, (Min Gain)		+11.5		dBm
Second Order Input Intercept (IIP2)	F_{RF1} = 1.905 GHz, F_{RF2} = 1.906 GHz, –10 dBm Each Tone, (Min Gain)		+25.5		dBm
LO Leakage (RF)	At RFIP		–60		dBm
LO Leakage (MXO)	At IMXO/QMXO		–42		dBm
Demodulation Bandwidth	–3 dB		90		MHz
Quadrature Phase Error	F_{RF} = 1.9 GHz	–3	±1	+3	Degree
I/Q Amplitude Imbalance	F_{RF} = 1.9 GHz		0.3		dB
Noise Figure	Max Gain		11		dB
Mixer AGC Output Level	See TPC 30		24		mV p-p
Baseband DC Offset	At IMXO/QMXO, Max Gain (Corrected, Ref to VREF)		2		mV
Mixer Output Swing	Level at which IMD3 = 45 dBc				
	R_{LOAD} = 200 Ω		65		mV p-p
	R_{LOAD} = 1 kΩ		65		mV p-p
Mixer Output Impedance			3		Ω
BASEBAND OUTPUT AMPLIFIER	From IAIN to IOPP/IOPN and QAIN to QOPP/QOPN R_{LOAD} = 10 kΩ				
Gain			30		dB
Bandwidth	–3 dB (See TPC 18)		65		MHz
Output DC Offset (Differential)	(V_{IOPP} – V_{IOPN})	–200	±50	+200	mV
Common-Mode Offset	(V_{IOPP} + V_{IOPN})/2 – V_{VCMO}	–40	±5	+40	mV
Group Delay Flatness	0 MHz–50 MHz		1.8		ns p-p
Second Order Intermod. Distortion	F_{IN}1 = 5 MHz, F_{IN}2 = 6 MHz, V_{IN}1 = V_{IN}2 = 8 mV p-p		–49		dBc
Third Order Intermod. Distortion	F_{IN}1 = 5 MHz, F_{IN}2 = 6 MHz, V_{IN}1 = V_{IN}2 = 8 mV p-p		–67		dBc
Input Bias Current			2		µA
Input Impedance			1‖3		MΩ‖pF
Output Swing Limit (Upper)		V_S – 1.3			V
Output Swing Limit (Lower)				0.4	V

Parameter	Conditions	Min	Typ	Max	Unit
CONTROL INPUT/OUTPUTS					
VCMO Input	@ V_S = 2.7 V		1		V
	@ V_S = 5 V	0.5	1	2.5	V
Gain Control Input Bias Current	VGIN		<1		µA
Offset Input Overriding Current	IOFS, QOFS		10		µA
VREF Output	R_{LOAD} = 10 kΩ	0.95	1.00	1.05	V
RESPONSE FROM RF INPUT TO FINAL BB AMP	IMXO/QMXO Connected Directly to IAIN/QAIN Respectively				
Gain @ V_{VGIN} = 0.2 V		65.5	69.5	72.5	dB
Gain @ V_{VGIN} = 1.2 V		–3	+0.5	+4	dB
Gain Slope		–96.5	–89	–82.5	dB/V
Gain Intercept	Linear extrapolation back to theoretical value at VGIN = 0	88	94	101	dB
LO/RF INPUT	(See TPC 26 Through 29 for More Detail)				
LOIP Input Return Loss	Measuring LOIP LOIN, ac-coupled to Ground with 100 pF.		–4		dB
	Measuring Through Evaluation Board Balun with Termination		–9.5		dB
RFIP Input Return Loss	RFIP Input Pin		–10		dB
ENABLE					
Power-Up Control	Low = Standby	0		0.5	V
Power-Up Control	High = Enabled	$+V_S$ – 1		$+V_S$	V
Power-Up Time	Time for Final BB Amps to be Within 90% of Final Amplitude				
	@ V_S = 5 V		20		µs
	@ V_S = 2.7 V		10		µs
Power-Down Time	Time for Supply Current to be <4 mA				
	@ V_S = 5 V		30		µs
	@ V_S = 2.7 V		1.5		ms
POWER SUPPLIES	V_{PS1}, V_{PS2}, V_{PS3}				
Voltage		2.7		5.5	V
Current (Enabled)	@ 5 V	48	64	80	mA
Current (Standby)	@ 5 V		400		µA
Current (Standby)	@ 3.3 V		80		µA

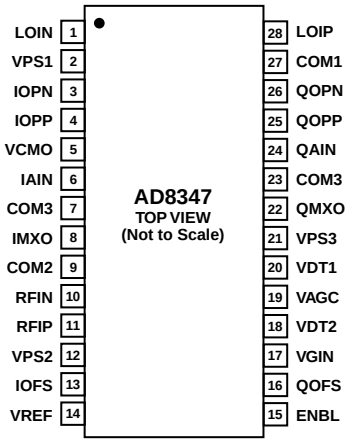
Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS*

Supply Voltage V_{PS1}, V_{PS2}, V_{PS3}	5.5 V
LO and RF Input Power	10 dBm
Internal Power Dissipation	500 mW
θ_{JA}	68°C/W
Maximum Junction Temperature	150°C
Operating Temperature Range	–40°C to +85°C
Storage Temperature Range	–65°C to +150°C
Lead Temperature (Soldering 60 sec)	300°C

*Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

PIN CONFIGURATION



ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
AD8347ARU	–40°C to +85°C	Tube (28-Lead TSSOP) Thin Shrink Small Outline Package	RU-28
AD8347ARU-REEL		13" Tape and Reel	
AD8347ARU-REEL7		7" Tape and Reel	
AD8347-EVAL		Evaluation Board	

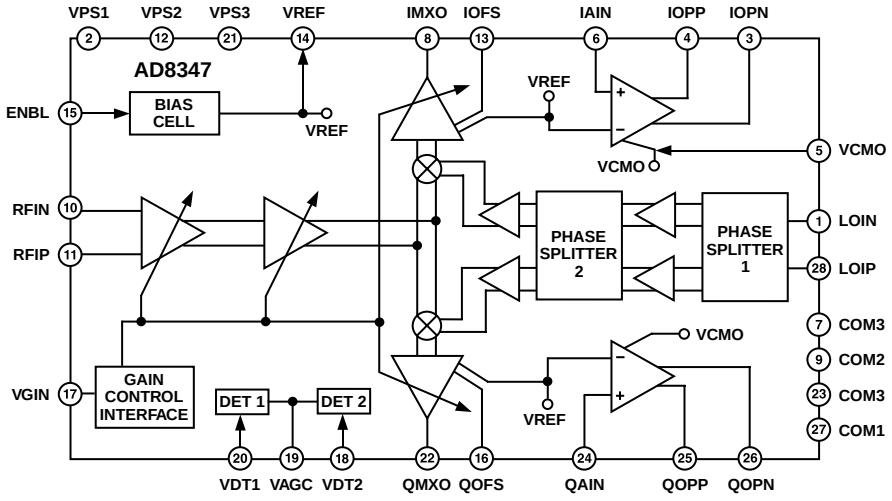


Figure 1. Block Diagram

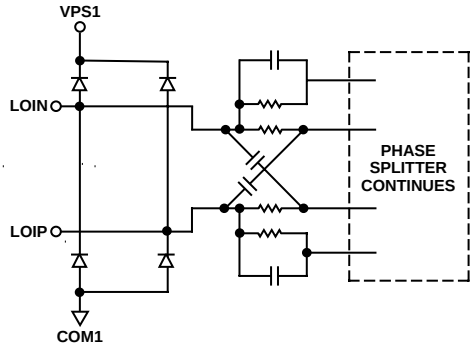
CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD8347 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high-energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

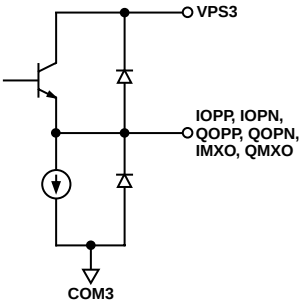
PIN FUNCTION DESCRIPTIONS

Pin No.	Mnemonic	Equiv. Cir.	Description
1, 28	LOIN, LOIP	A	LO Input. For optimum performance, these inputs should be driven differentially. Typical input drive level is equal to –8 dBm. To improve the match to a 50 Ω source, connect a 200 Ω shunt resistor between LOIP and LOIN. A single-ended drive is also possible but this will slightly increase LO leakage.
2	VPS1		Positive Supply for LO Section. This pin should be decoupled with 0.1 μF and 100 pF capacitors.
3, 4	IOPN, IOPP	B	I Channel Differential Baseband Output. Typical output swing is equal to 760 mV p-p differential in AGC mode. The common mode level on these pins is programmed by the voltage on VCMO.
5	VCMO	C	Baseband Amplifier Common-Mode Voltage. The voltage applied to this pin sets the output common-mode level of the baseband amplifiers. This pin can either be connected to VREF (Pin 14) or to a reference voltage from another device (typically an ADC).
6	IAIN	D	I Channel Baseband Amplifier Input. This pin, which has a high input impedance, should be biased to VREF (approximately 1 V). If IAIN is connected directly to IMXO, biasing will be provided by IMXO. If an ac-coupled filter is placed between IMXO and IAIN, this pin can be biased from VREF through a 1 kΩ resistor. The gain from IAIN to the differential outputs IOPN/IOPP is 30 dB.
7, 23	COM3		Ground for Biasing and Baseband Sections
8, 22	IMXO, QMXO	B	I & Q Channel Baseband Mixer/VGA Outputs. These are low impedance outputs whose bias levels are equal to VREF. IMXO and QMXO are typically connected to IAIN and QAIN respectively, either directly or through filters. These outputs have a maximum current limit of about 1.5 mA. This allows for a 600 mV p-p swing into a 200 Ω load. This corresponds to an input level of –40 dBm @ max gain of 39.5 dB. At lower output levels, IMXO and QMXO, can drive a lower load resistance, subject to the same current limit.
9	COM2		RF Section Ground
10, 11	RFIN, RFIP	E	RF Input. RFIN must be ac-coupled to ground. The RF input signal should be ac-coupled into RFIP. For a broadband 50 Ω input impedance, connect a 200 Ω resistor from the signal side of RFIP's coupling capacitor to ground. Please note that RFIN and RFIP are not interchangeable differential inputs. RFIN is the ground reference for the input system.
12	VPS2		Positive Supply for RF Section. This pin should be decoupled with 0.1 μF and 100 pF capacitors.
13, 16	IOFS, QOFS	F	I Channel and Q Channel Offset Nulling Inputs. To null the dc-offset on the I Channel and Q Channel Mixer Outputs (IMXO, QMXO), connect a 0.1 μF capacitor from these pins to ground. Alternately, a forced voltage of approximately 1 V on these pins will disable the offset compensation circuit.
14	VREF	G	Reference Voltage Output. This output voltage (1 V) is the main bias level for the device and can be used to externally bias the inputs and outputs of the baseband amplifiers.
15	ENBL	H	Chip Enable Input. Active high.
17	VGIN	C	Gain Control Input. The voltage on this pin controls the gain on the RF and baseband VGAs. The gain control is applied in parallel to all VGAs. The gain control voltage range is from 0.2 V to 1.2 V and corresponds to a gain range from +39.5 dB to –30 dB. This is the gain to the output of the baseband VGAs (i.e., QMXO and IMXO). There is an additional 30 dB of gain in the baseband amplifiers. Note that the gain control function has a negative sense (i.e., increasing control voltage decreases gain). In AGC mode, this pin is connected directly to VAGC.
18, 20	VDT2, VDT1	D	Detector Inputs. These pin are the inputs to the on-board detector. VDT2 and VDT1, which have high input impedances, are normally connected to IMXO and QMXO respectively.
19	VAGC	I	AGC Output. This pin provides the output voltage from the on-board detector. In AGC mode, this pin is connected directly to VGIN.
21	VPS3		Positive Supply for Biasing and Baseband Sections. This pin should be decoupled with 0.1 μF and 100 pF capacitors.
24	QAIN	D	Q Channel Baseband Amplifier Input. This pin, which has a high input impedance, should be biased to VREF (approximately 1 V). If QAIN is connected directly to QMXO, biasing will be provided by QMXO. If an ac-coupled filter is placed between QMXO and QAIN, this pin can be biased from VREF through a 1 kΩ resistor. The gain from QAIN to the differential outputs QOPN/QOPP is 30 dB.
25, 26	QOPP, QOPN	B	Q Channel Differential Baseband Output. Typical output swing is equal to 1 V p-p differential. The common-mode level on these pins is programmed by the voltage on VCMO.
27	COM1		LO Section Ground

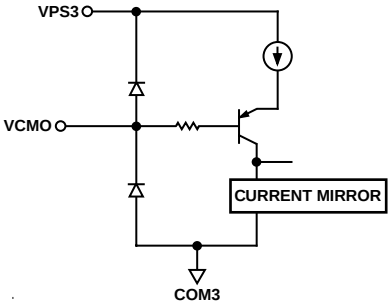
EQUIVALENT CIRCUITS



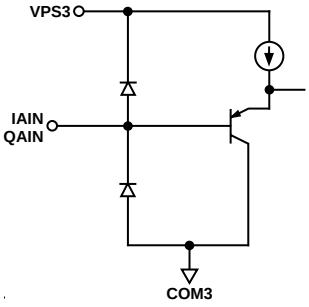
Circuit A



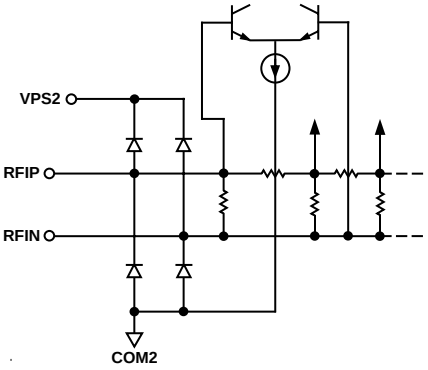
Circuit B



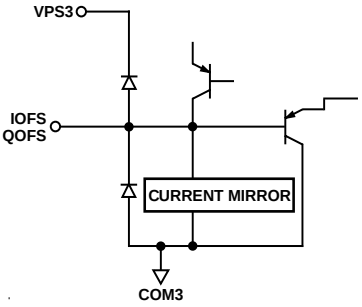
Circuit C



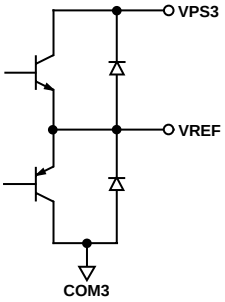
Circuit D



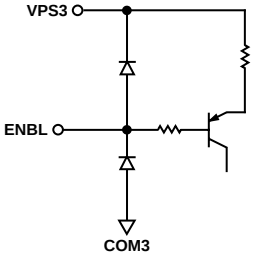
Circuit E



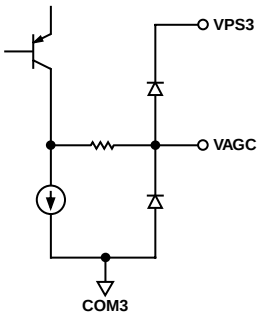
Circuit F



Circuit G



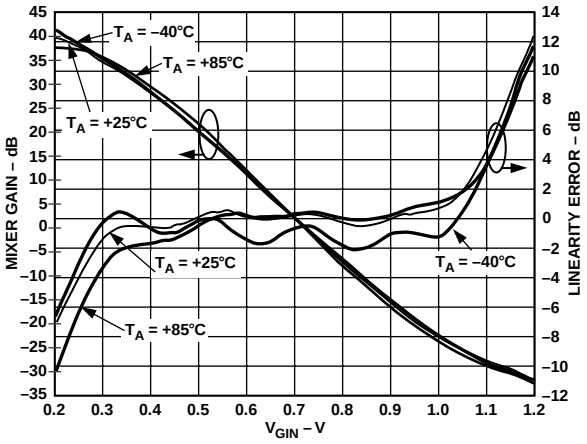
Circuit H



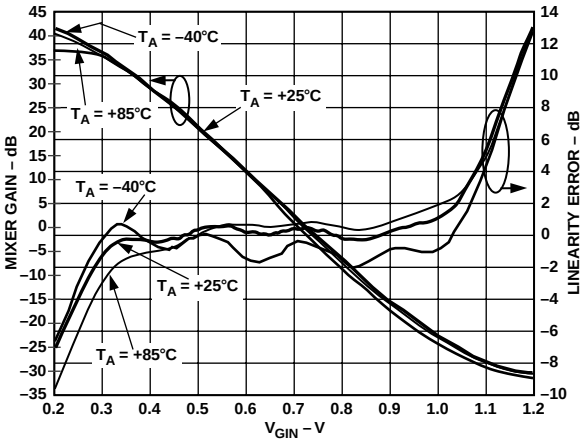
Circuit I

Figure 2. Equivalent Circuits

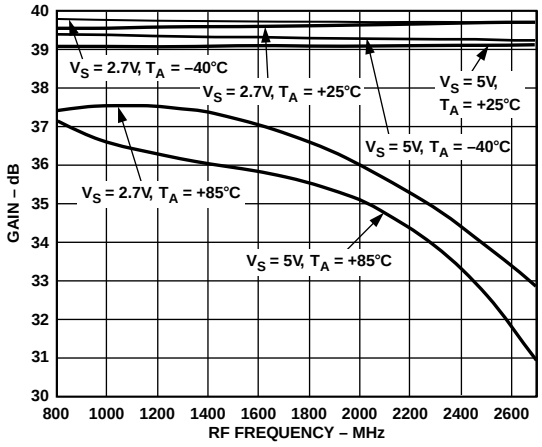
RF AMP AND DEMODULATOR



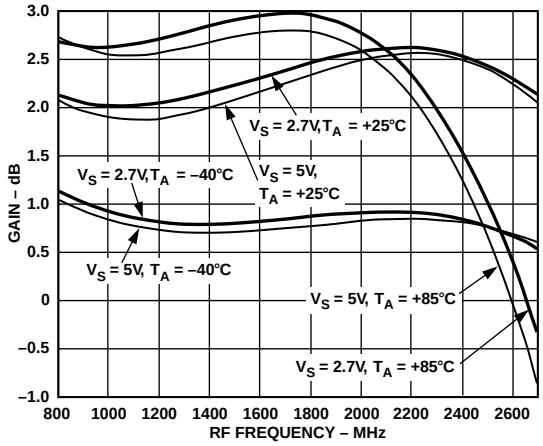
TPC 1. Gain and Linearity Error vs. V_{GIN}, V_S = 5 V, F_{LO} = 1900 MHz, F_{BB} = 1 MHz



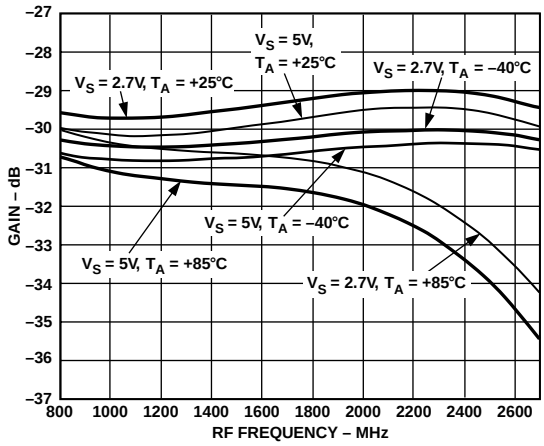
TPC 2. Gain and Linearity Error vs. V_{GIN}, V_S = 2.7 V, F_{LO} = 1900 MHz, F_{BB} = 1 MHz



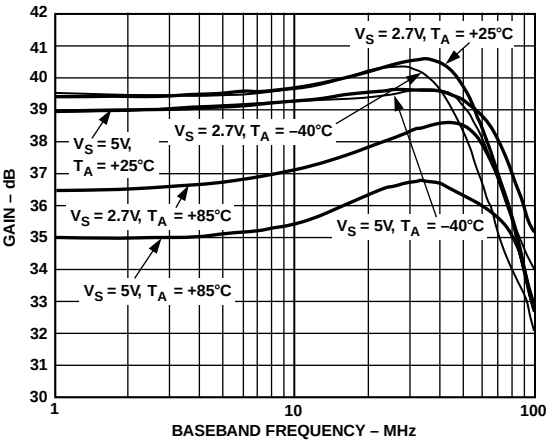
TPC 3. Gain vs. F_{LO}, V_{GIN} = 0.2 V , F_{BB} = 1 MHz



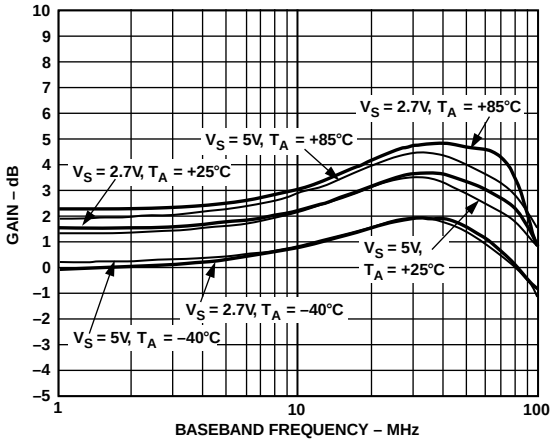
TPC 4. Gain vs. F_{LO}, V_{GIN} = 0.7 V, F_{BB} = 1 MHz



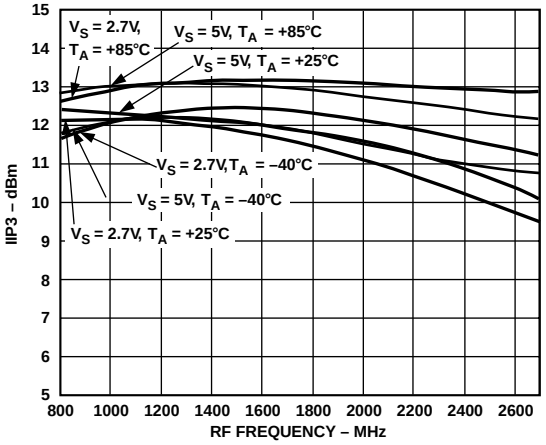
TPC 5. Gain vs. F_{LO}, V_{GIN} = 1.2 V, F_{BB} = 1 MHz



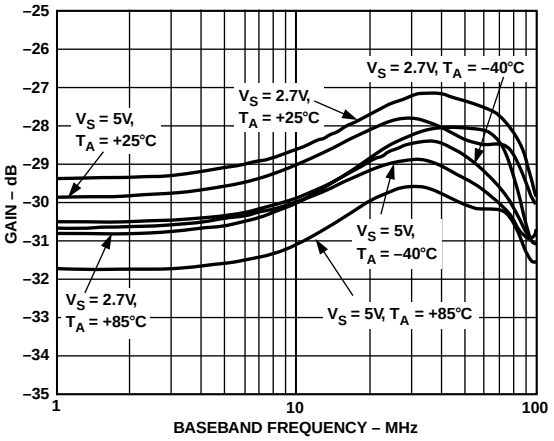
TPC 6. Gain vs. F_{BB}, V_{GIN} = 0.2 V, F_{LO} = 1900 MHz



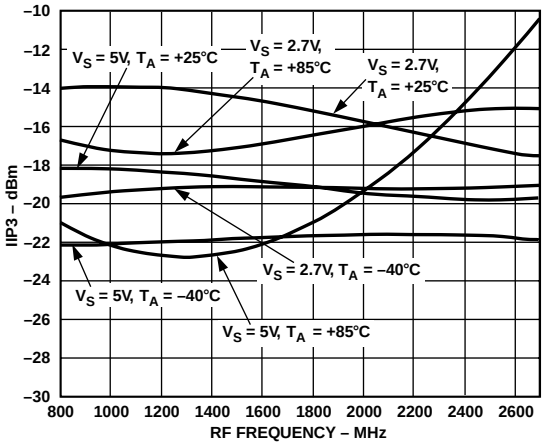
TPC 7. Gain vs. F_{BB}, V_{GIN} = 0.7 V, F_{LO} = 1900 MHz



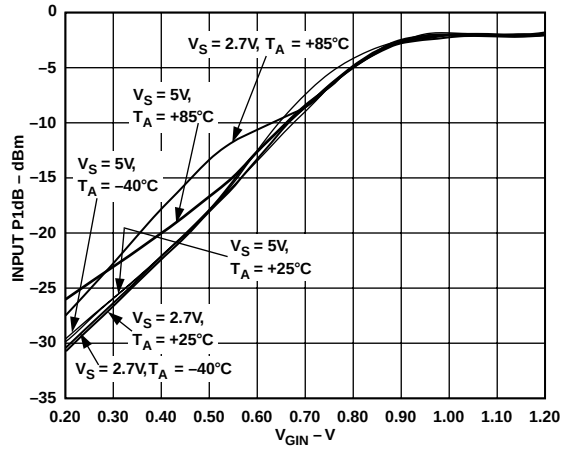
TPC 10. IIP3 vs. F_{LO}, V_{GIN} = 1.2 V, F_{BB} = 1 MHz



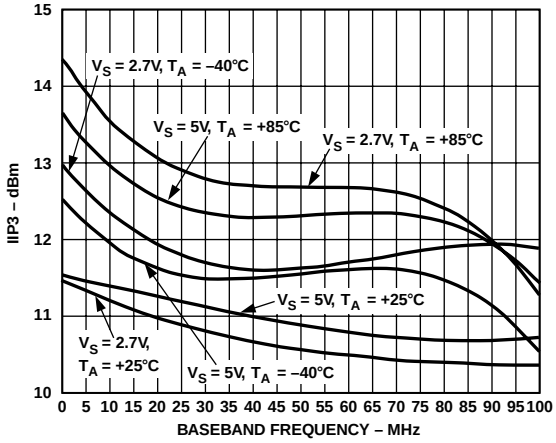
TPC 8. Gain vs. F_{BB}, V_{GIN} = 1.2 V, F_{LO} = 1900 MHz



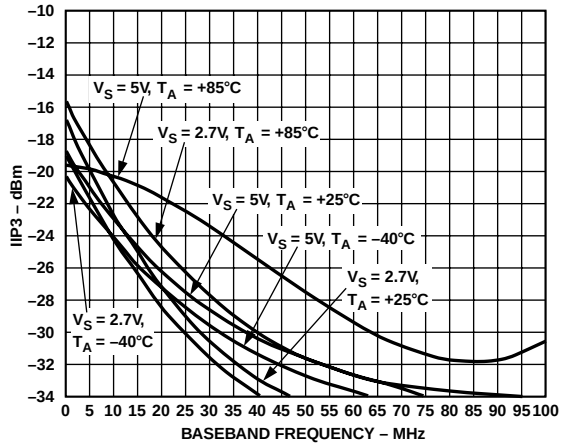
TPC 11. IIP3 vs. F_{LO}, V_{GIN} = 0.2 V, F_{BB} = 1 MHz,



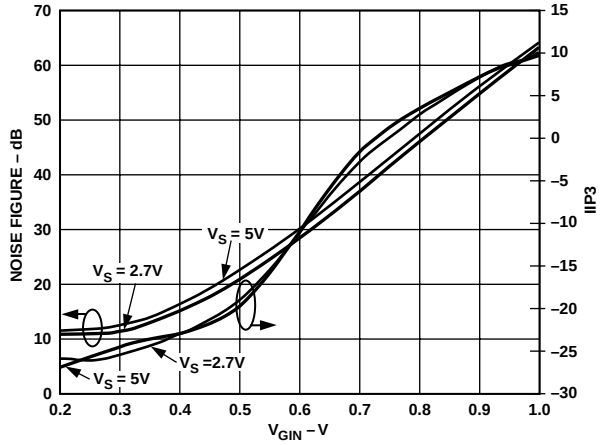
TPC 9. Input 1 dB Compression Point (OP1 dB) vs. V_{GIN}, F_{LO} = 1900 MHz, F_{BB} = 1 MHz



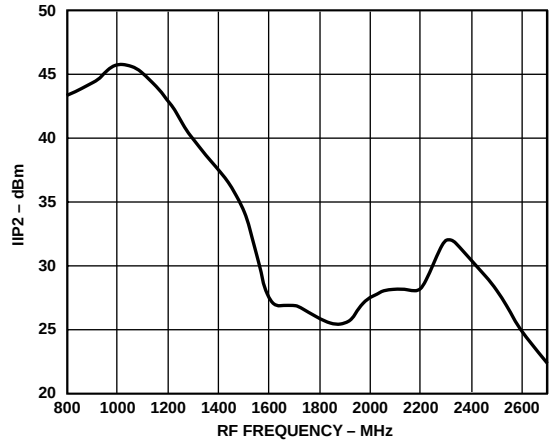
TPC 12. IIP3 vs. F_{BB}, V_{GIN} = 1.2 V, F_{LO} = 1900 MHz



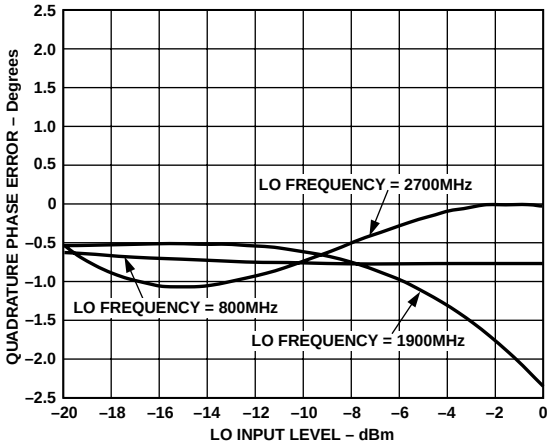
TPC 13. IIP3 vs. F_{BB}, V_{GIN} = 0.2 V, F_{LO} = 1900 MHz



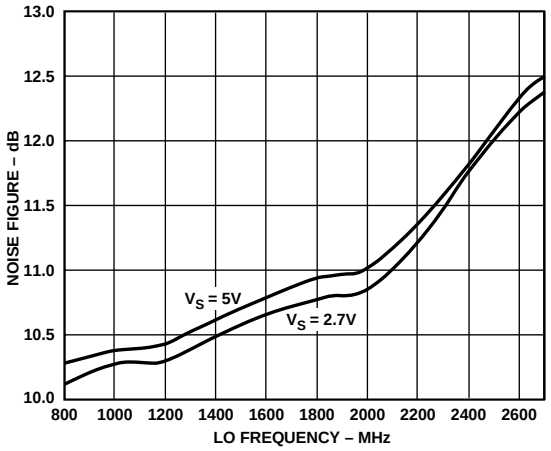
TPC 16. Noise Figure and IIP3 vs. V_{GIN}, Temperature = 25°C, F_{LO} = 1900 MHz, F_{BB} = 1 MHz



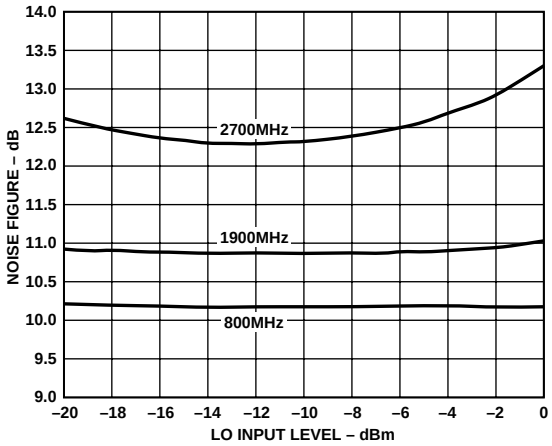
TPC 14. IIP2 vs. F_{LO}, V_{GIN} = 1.2 V, Baseband Tone1 = 5 MHz, –10 dBm, Baseband Tone2 = 6 MHz, –10 dBm, Temperature = 25°C, V_S = 5 V



TPC 17a. Quadrature Error vs. LO Power Level, Temperature = 25°C, V_{GIN} = 0.2 V, V_S = 5 V

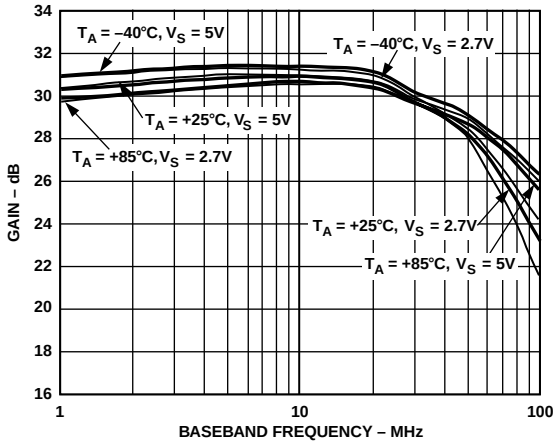


TPC 15. Noise Figure vs. LO Frequency (F_{LO}), Temperature = 25°C, V_{GIN} = 0.2 V, F_{BB} = 1 MHz

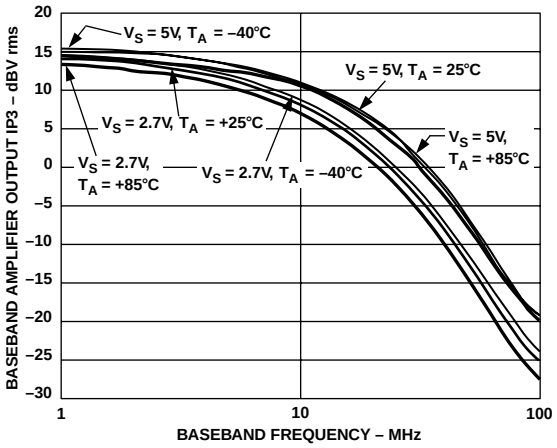


TPC 17b. Noise Figure vs. LO Input Level, Temperature = 25°C, V_{GIN} = 0.2 V, V_S = 5 V

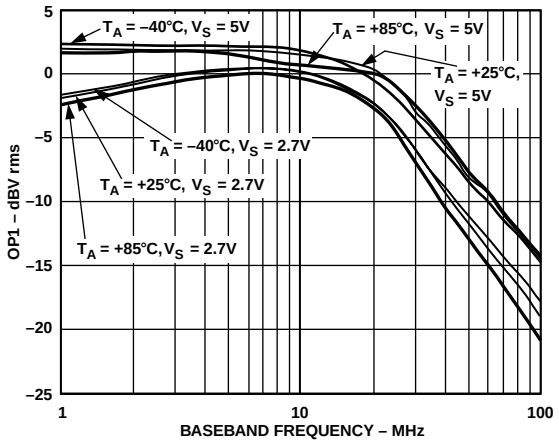
BASEBAND OUTPUT AMPLIFIERS



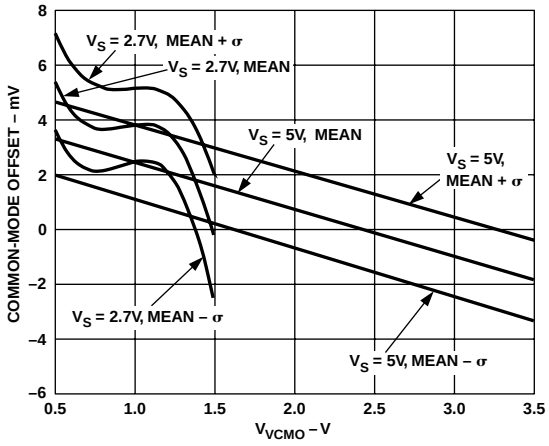
TPC 18. Gain vs. F_{BB}, V_{VCMO} = 1 V



TPC 20. OIP3 vs. F_{BB}, V_{VCMO} = 1 V

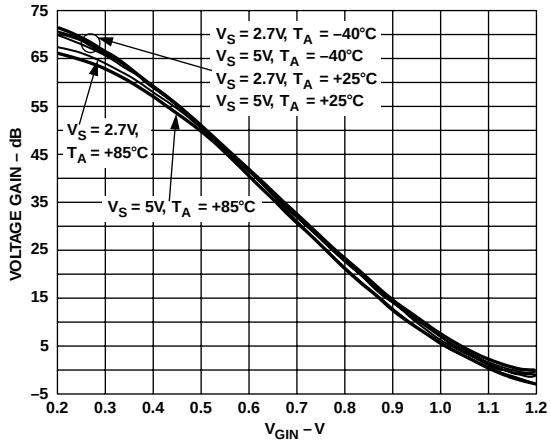


TPC 19. OP1 vs. F_{BB}, V_{VCMO} = 1 V

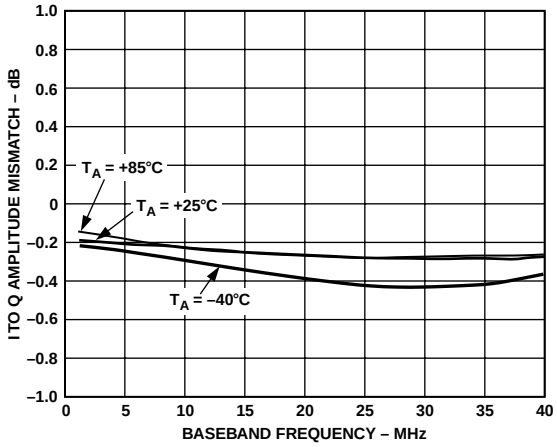


TPC 21. Common-Mode Output Offset Voltage vs. V_{VCMO}, Temperature = 25°C (σ = 1 Standard Deviation)

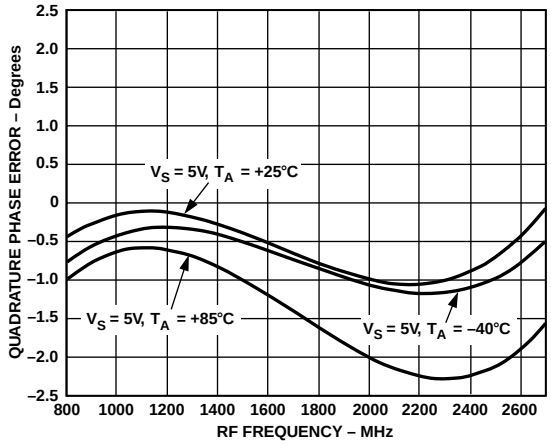
RF AMP/DEMOD AND BASEBAND OUTPUT AMPLIFIERS



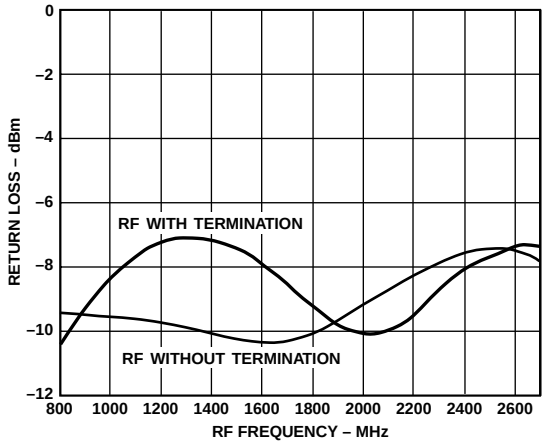
TPC 22. Voltage Gain vs. V_{VGIN}, F_{LO} = 1900 MHz, F_{BB} = 1 MHz



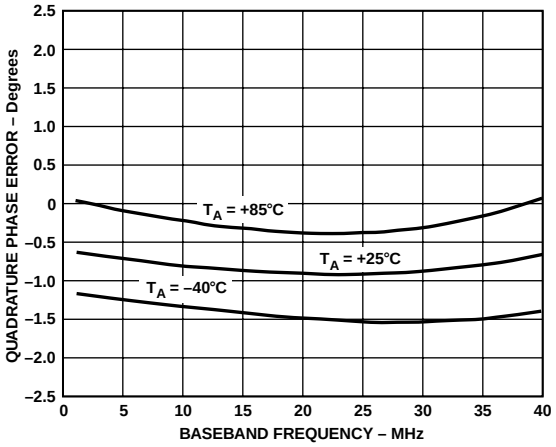
TPC 25. I/Q Amplitude Imbalance vs. F_{BB}, Temperature = 25°C, V_S = 5 V



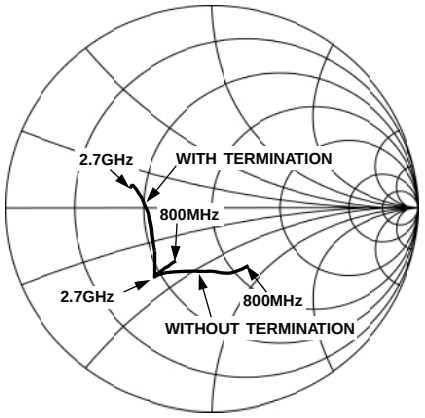
TPC 23. Quadrature Phase Error vs. F_{LO}, V_{VGIN} = 0.7 V, V_S = 5 V



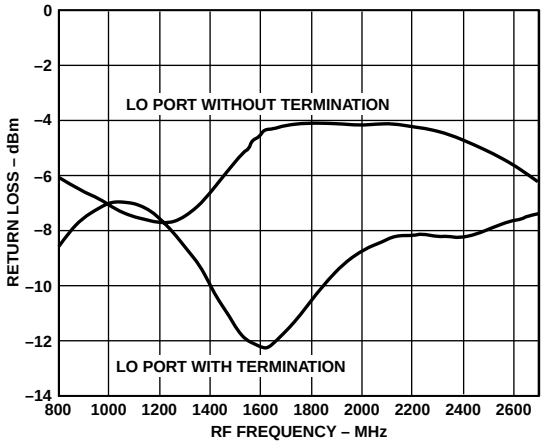
TPC 26. Return Loss of RFIP vs. F_{RF}, V_{VGIN} = 0.7 V, V_S = 5 V



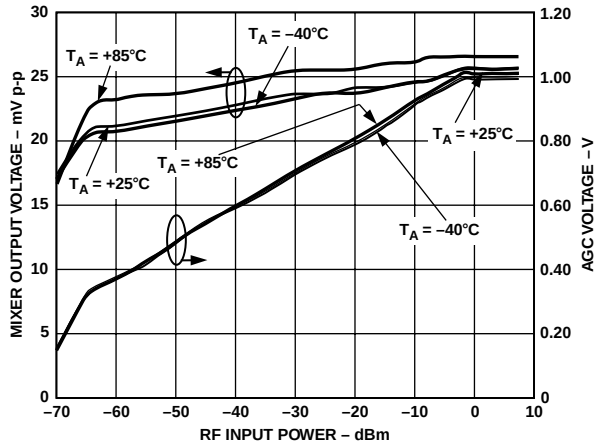
TPC 24. Quadrature Phase Error vs. F_{BB}, V_{VGIN} = 0.7 V, V_S = 5 V



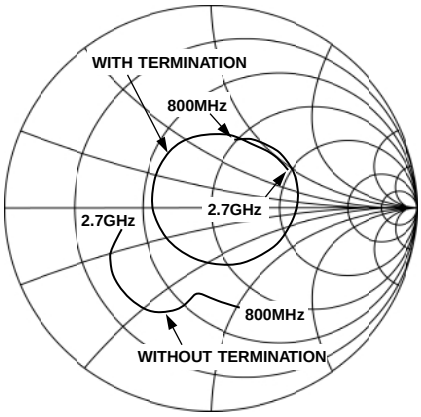
TPC 27. S11 of RFIN vs. F_{RF}, V_{VGIN} = 0.7 V, V_S = 5 V



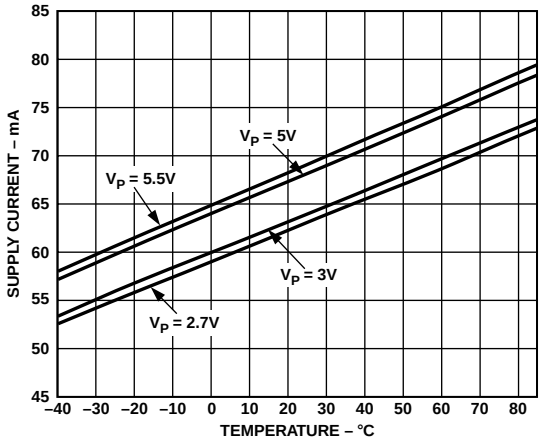
TPC 28. Return Loss of LOIP vs. F_{LO}, V_{VGIN} = 0.7 V, V_P = 5 V



TPC 30. AGC Voltage and Mixer Output Level vs. RF Input Power, F_{LO} = 1900 MHz, F_{BB} = 1 MHz, V_S = 5 V



TPC 29. S11 of LOIN vs. F_{LO}, V_{VGIN} = 0.7 V, V_S = 5 V



TPC 31. Supply Current vs. Temperature, V_{VGIN} = 0.7 V, V_{VCMO} = 1 V

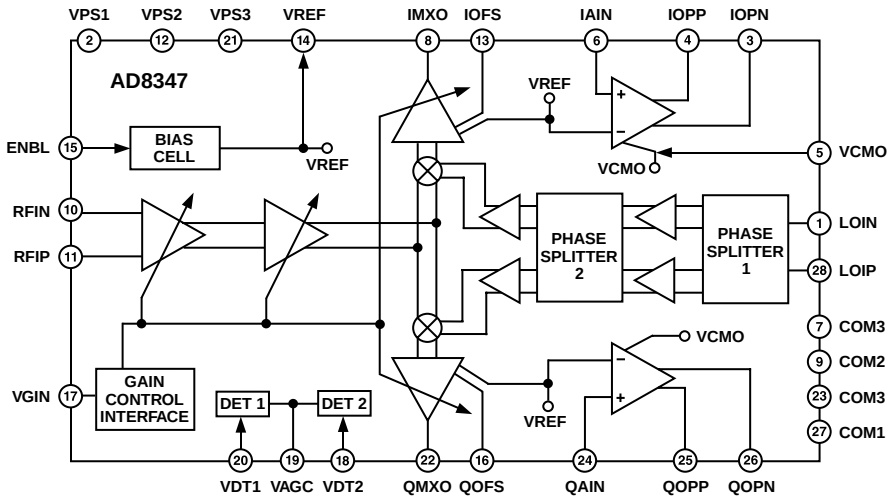


Figure 3. Block Diagram

CIRCUIT DESCRIPTION

OVERVIEW

The AD8347 is a direct I/Q demodulator usable in digital wireless communication systems including Cellular, PCS, and Digital Video receivers. An RF signal in the frequency range of 800 MHz–2700 MHz is directly downconverted to the I & Q components at baseband using a Local Oscillator (LO) signal at the same frequency as the RF signal.

The RF input signal goes through two stages of variable gain amplifiers before splitting up to reach two Gilbert-cell Mixers. The mixers are driven by a pair of Local Oscillator (LO) signals which are in quadrature (90 degrees of phase difference). The outputs of the mixers are applied to baseband I & Q channel variable-gain amplifiers. The outputs from these baseband variable gain amplifiers are brought out to pins for external filtering. The filter outputs are then applied to a pair of on-chip, fixed-gain baseband amplifiers. These amplifiers gain up the outputs from the external filters to a level compatible with most A-to-D Converters. A sum-of-squares detector is available for use in an Automatic Gain Control (AGC) loop to set the output level. The RF and baseband amplifiers provide approximately 69.5 dB of gain control range. Additional on-chip circuits allow the setting of the dc level at the I & Q channel baseband outputs, as well as nulling the dc offset at each channel.

RF Variable Gain Amplifiers (VGA)

These amplifiers use the patented X-AMP® approach with NPN-differential pairs separated by sections of resistive attenuators. The gain control is achieved through a gaussian interpolator where the control voltage sets the tail currents to be supplied to the different differential pairs according to the gain desired. In the first amplifier, the combined output currents from the transconductance cells go through a cascode stage to resistive loads with inductive peaking. In the second amplifier the differential currents are split and fed to the two Gilbert-cell mixers through separate cascode stages.

Mixers

Two double balanced Gilbert-cell mixers, one for each channel, perform the In-phase (I) and Quadrature (Q) down conversion. Each mixer has four cross-connected transistor pairs which are terminated in resistive loads and feed the differential baseband variable gain amplifiers for each channel. The bases of the mixer transistors are driven by the quadrature LO signals.

Baseband Variable Gain Amplifiers

The baseband VGA's also use the X-AMP approach with NPN-differential pairs separated by sections of resistive attenuators. The same interpolator controlling the RF amplifiers controls the tail currents of the differential pairs. The outputs of these amplifiers are provided off chip for external filtering. Automatic offset nulling minimizes the dc offsets at both I & Q channels. The common-mode output voltage is set to be the same as the reference voltage (1.0 V) generated in the Bias section, also made available at the VREF pin.

Output Amplifiers

The output amplifiers gain up the signal coming back from each of the external filters to a level compatible with most high speed A-to-D converters. These amplifiers are based on an active-feedback design to achieve the high gain bandwidth and low distortion.

LO and Phase-Splitters

The incoming LO signal is applied to a polyphase phase-splitter to generate the LO signals for the I channel and Q channel mixers. The polyphase phase-splitters are RC networks connected in a cyclical manner to achieve gain balance and phase quadrature. The wide operating frequency range of these phase-splitters is achieved by cascading multiple sections of these networks with staggered RC constants. Each branch goes through a buffer to make up for the loss and high frequency roll-off. The output from the buffers then go into another polyphase phase-splitter to enhance the accuracy of phase quadrature. Each LO signal gets buffered again to drive the mixers.

Output Level Detector

Two signals proportional to the square of each output channel are summed together and compared to a built-in threshold to create an AGC voltage (VAGC). The inputs to this rms detector are referenced to VREF.

Bias

An accurate reference circuit generates the reference currents used by the different sections. The reference circuit is controlled by an external power-up (ENBL) logic signal which, when set low, puts the whole chip into a sleep mode typically requiring

X-AMP is a registered trademark of Analog Devices, Inc.

less than 400 μA of supply current. The reference voltage (VREF) of 1.0 V, which serves as the common-mode reference for the baseband circuits, is made available for external use.

OPERATING THE AD8347

Basic Connections

Figure 4 shows the basic connections for operating the AD8347. The device is powered through three power supply pins: VPS1, VPS2, and VPS3. These pins supply current to different parts of the overall circuit. VPS1 and VPS2 power the Local Oscillator (LO) and RF sections, respectively, while VPS3 powers the baseband amplifiers. While all of these pins should be connected to the same supply voltage, each pin should be separately decoupled using two capacitors. 100 pF and 0.1 μF are recommended (values close to these may also be used).

A supply voltage in the range 2.7 V to 5.5 V should be used. The quiescent current is 64 mA when operating from a 5 V supply. By pulling the ENBL pin low, the device goes into its power- down mode. The power-down current is 400 μA when operating on a 5 V supply and 80 μA on a 2.7 V supply.

Like the supply pins, the individual sections of the circuit are separately grounded. COM1, COM2, and COM3 provide ground for the LO, RF, and baseband sections respectively. All of these pins should be connected to the same low impedance ground.

RF Input and Matching

The RF input signal should be ac-coupled into the RFIP pin and RFIN should be ac-coupled to ground. To improve broadband matching to a 50 Ω source, a 200 Ω resistor may be connected from the signal side of RFIP's coupling capacitor to ground.

LO Drive Interface

For optimum performance the LO inputs, LOIN and LOIP, should be driven differentially. M/A-COM balun, ETC1-1-13 is recommended. Unless an (ac-coupled) transformer is being used to generate the differential LO, the inputs must be ac-coupled as shown. To improve broadband matching to a 50 Ω source, a 200 Ω shunt resistor may be connected between LOIP and LOIN.

An LO drive level of –8 dBm is recommended. TPC 17a shows the relationship between LO drive level, LO frequency, and quadrature error for a typical device.

A single-ended drive is also possible as shown in Figure 5, but this will slightly increase LO leakage. The LO signal should be applied through a coupling capacitor to LOIP, and LOIN should be ac-coupled to ground. Because the inputs are fully differential, the drive orientation can be reversed. As in the case of the differential drive, a 200 Ω resistor connected across LOIP and LOIN improves the match to a 50 Ω source.

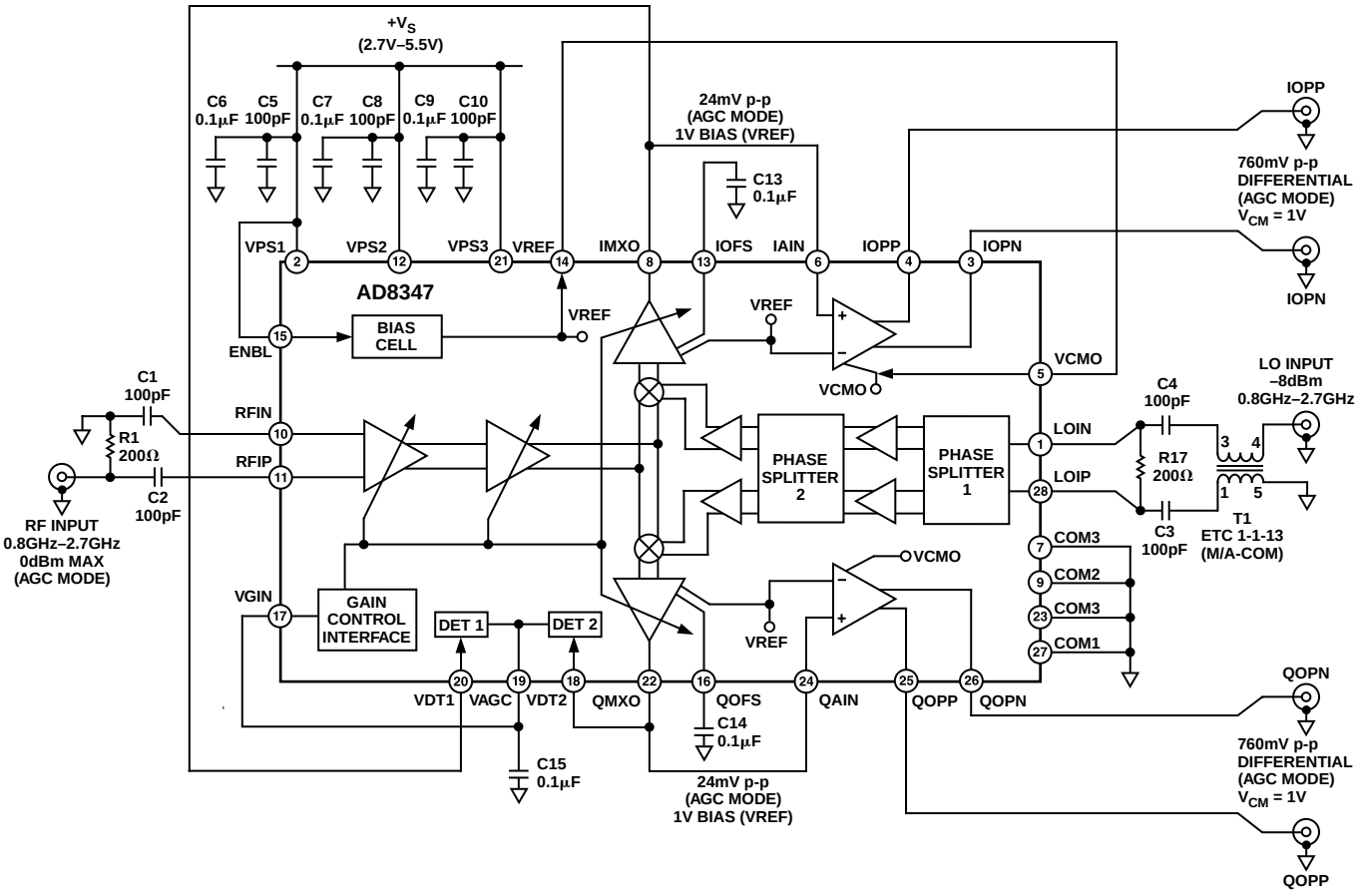


Figure 4. Basic Connections

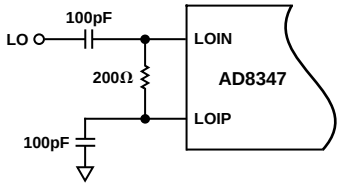


Figure 5. Single-Ended LO Drive

Operating the VGA

A three-stage VGA sets the gain in the RF section. Two of the three stages come before the mixer while the third amplifies the mixer output. All three stages are driven in parallel. The gain range of the first RF VGA and that of the second RF VGA combined with the mixer are both –13 dB to +10 dB. The gain range of the baseband VGA is –4 dB to +19.5 dB. So the overall gain range from the RF input to the IMXO/QMXO pins is –30 dB to approximately +39.5 dB.

The gain of the VGA is set by the voltage on the VGIN pin, which is a high impedance input. The gain control function (which is linear-in-dB) and linearity are shown in TPC 1 and TPC 2 at 1.9 GHz. Note that the sense of the gain control voltage is negative so as the gain control voltage ranges from 0.2 V to 1.2 V, the gain *decreases* from +39.5 dB to –30 dB.

Mixer Output Level and Drive Capability

I & Q channel baseband outputs, IMXO and QMXO are low impedance outputs (R_{OUT} @ 3 Ω) whose bias level is equal to V_{VREF}, the voltage on Pin 14. The achievable output level on IMXO/QMXO is limited by their current drive capability of 1.5 mA max. This would allow for a 600 mV p-p swing into a 200 Ω load. At lower output levels, IMXO and QMXO can drive smaller load resistances, subject to the same current limit. These output stages are not, however, designed to drive 50 Ω loads directly.

Operating the VGA in AGC Mode

While the VGA can be driven by an external source such as a DAC, the AD8347 has an on-board sum of squares detector which allows the AD8347 to operate in an automatic leveling mode. The connections for operating in this mode are shown in Figure 4. The two mixer outputs are connected to the detector inputs VDT1 and VDT2. The summed detector output drives an internal integrator which in turn delivers a gain correction voltage to the VAGC pin. A 0.1 µF capacitor from VAGC to ground sets the dominant pole of the integrator circuit. VAGC, which should be connected to VGIN, adjusts gain until an internal threshold is reached. This threshold corresponds to a level at the IMXO/QMXO pins of approximately 8.5 mV rms. This level will change slightly as a function of RF input power (see TPC 30). For a CW (sine wave) input this corresponds to

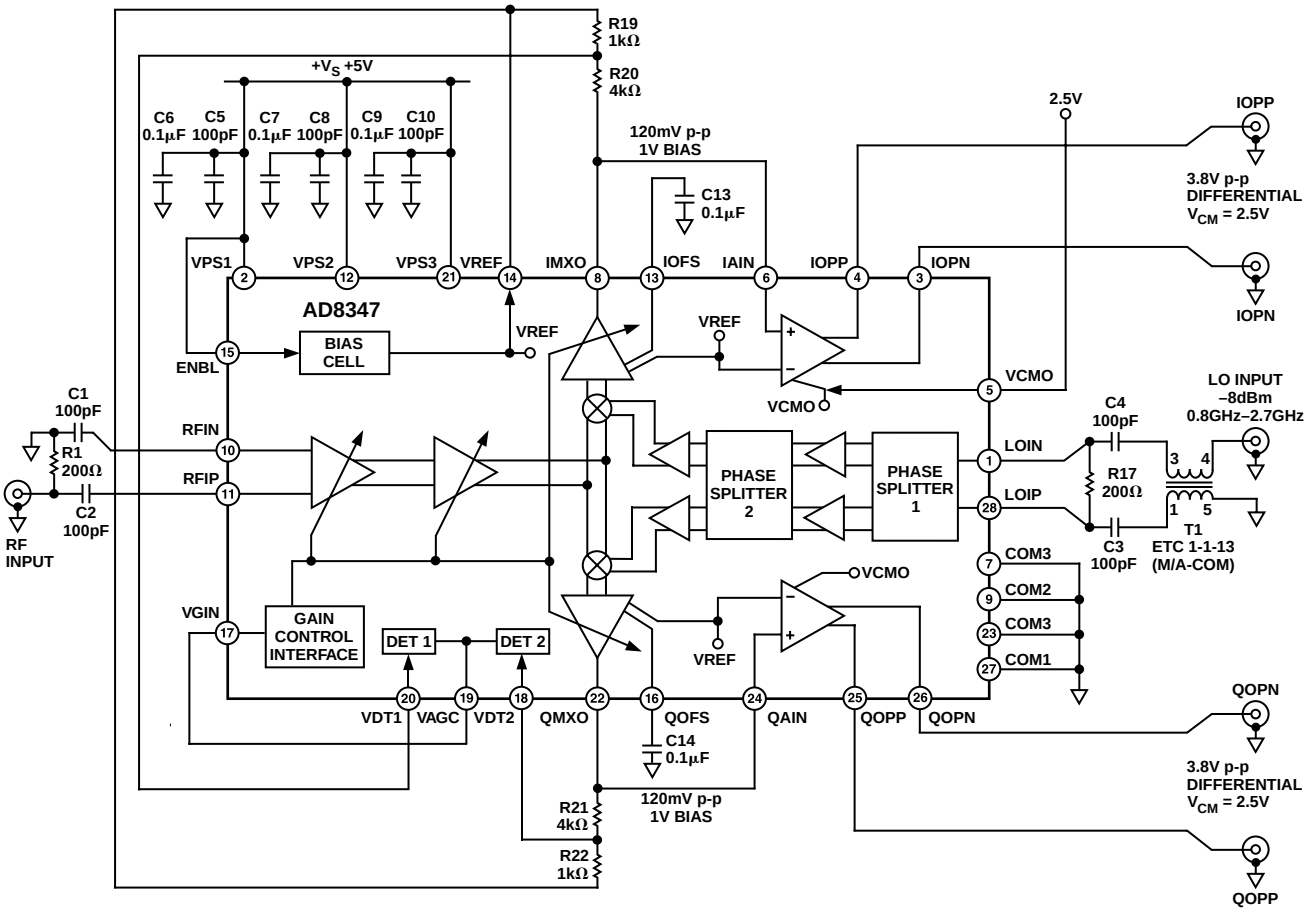


Figure 6. Adjusting AGC Level to Increase Baseband Amplifier Output Swing

approximately 24 mV p-p. If this signal is applied directly to the subsequent baseband amplifier stage, the final baseband output is 760 mV p-p differential. (See Baseband Amplifier section.)

If the VGA gain is being set from an external source, the on-board detector inputs (VDT1 and VDT2) are not used and should be tied to VREF.

Note that in subsequent sections, peak-to-peak calculations assume a sine wave input. If the input signal has a higher peak-to-average ratio, the mixer output peak-to-peak voltage at which the AGC loop settles will be higher.

Changing the AGC Setpoint

The AGC circuit can be easily set up to level at voltages higher than the nominal 24 mV p-p as shown in Figure 6. The voltages on Pins IMXO and QMXO are attenuated before being applied to the detector inputs. In the example shown, an attenuation factor of 0.2 (–14 dB) between IMXO/QMXO and the detector inputs, will cause the VGA to level at approximately 120 mV p-p (note that resistor divider network must be referenced to V_{VREF}). This results in a peak-to-peak output swing at the baseband amplifier outputs of 3.8 V differential, that is, 1.6 V to 3.4 V on each side. Note that V_{VCMO} has been increased to 2.5 V to avoid signal clipping at the baseband outputs. Due to the attenuation between the mixer output and the detector input, the variation in the settled mixer output level, versus RF input power, will be greater than the variation shown in TPC 30. The variation will be greater by a factor equal to the inverse of the attenuation factor.

Baseband Amplifiers

The final baseband amplifier stage takes the signals from IMXO/QMXO and amplifies them by 30 dB, or a factor of 31.6. This results in a maximum system gain of 69.5 dB. When the VGA is in AGC mode, the baseband I & Q outputs (IOPN, IOPP, QOPN, and QOPP) deliver a differential voltage of approximately 760 mV p-p (380 mV p-p on each side).

The single-ended input signal to the baseband amplifiers is applied at the high impedance inputs IAIN and QAIN. As can be seen in Figure 4, the baseband amplifier operates internally as a differential amplifier, with the second input being driven by V_{VREF}. As a result, the input signal to the baseband amplifier should be biased at V_{VREF}.

The output common-mode level of the baseband amplifiers is set by the voltage on Pin 5, VCMO. This pin can either be connected to VREF (Pin 14) or to an external reference voltage from a device such as an analog-to-digital converter (ADC). V_{VCMO} has a nominal range from 0.5 V to 2.5 V. However, since the baseband amplifiers can only swing down to 0.4 V, higher values of V_{VCMO} will generally be required to avoid low-end signal clipping. On the other hand, the positive swing at each output is limited to 1.3 V below the supply voltage. So the max p-p swing is given by $2 \times (V_{PS} – 1.3 – 0.4)$ V differentially.

For example, in order for the baseband output amplifier to be able to deliver an output swing of 2 V p-p (1 V p-p on each side), V_{VCMO} must be in the range from 0.9 V to 2.5 V.

The differential output offset voltages of the baseband amplifiers are typically ±50 mV. This offset voltage results from both input and output effects.

The overall signal-to-noise ratio can be improved by increasing the VGA gain by driving it with an external voltage or by changing the setpoint of the AGC circuit. (See Changing the AGC Setpoint.)

Driving Capacitive Loads

In applications where the baseband amplifiers are driving unbalanced capacitive loads, some series resistance should be placed between the amplifier and the capacitive load. For example, for a 10 pF load, four 220 Ω series resistors (one in each baseband output) should be used.

External Baseband Amplification

The baseband output offset voltage and noise can be reduced by bypassing the internal baseband amplifiers and amplifying the mixer output signal using a high quality differential amplifier. In the example shown in Figure 7, two AD8132 differential amplifiers are used to gain the mixer output signals up by 20 dB. In this example, the setpoint of the AGC circuit has been increased so that the input to the external amplifiers is approximately 72 mV p-p. This results in final baseband output signals of 720 mV p-p.

The closed-loop bandwidth of the amplifiers in Figure 7 is equal to roughly 20 MHz. Higher bandwidths are achievable, but at the cost of lower closed-loop gain. In Figure 7, the output common mode levels (VOCM, Pin 2) of the differential amplifiers are set by the AD8347's VREF (approximately 1 V). The output common mode levels can also be set externally (e.g., by the reference voltage from an ADC).

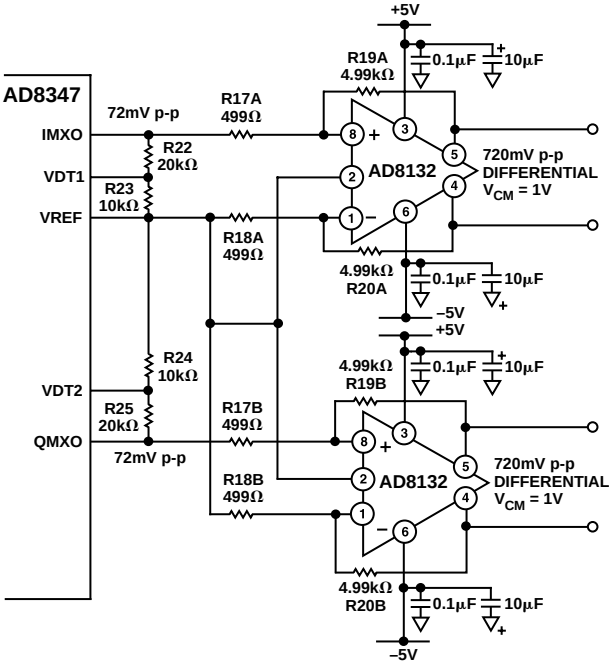


Figure 7. External Baseband Amplification Example

Filter Design Considerations

Baseband low-pass or band-pass filtering can be conveniently performed between the mixer outputs (IMXO/QMXO) and the input to the baseband amplifiers. Because the output impedance of the mixer is low (roughly 3 Ω) and the input impedance of the baseband amplifier is high, it is not practical to design a filter which is reactively matched to these impedances. An LC filter can be matched by placing a series resistor at the mixer output and a shunt resistor (terminated to V_{VREF}) at the input to the baseband amplifier.

Because the mixer output drive level is limited to a maximum current of 1.5 mA, the characteristic impedance of the filter should be greater than 50 Ω, especially if larger signal swings are to be achieved.

Figure 8 shows the schematic for a 100 Ω, fourth order elliptic low-pass filter with a 3 dB cutoff frequency of 20 MHz. Source and load impedances of approximately 100 Ω ensure that the filter sees a matched source and load. This also ensures that the mixer output is driving an overall load of 200 Ω. Note that the shunt termination resistor is tied to VREF and not to ground. The frequency response and group delay of this filter are shown in Figures 9 and 10.

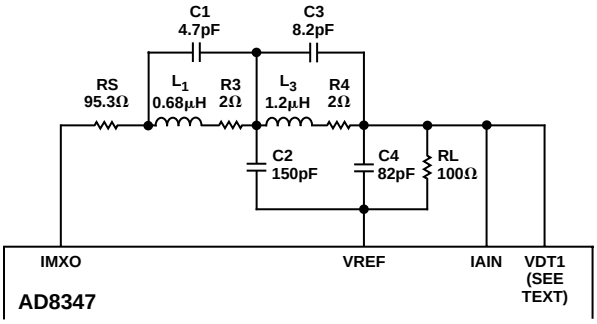


Figure 8. Typical Baseband Low-Pass Filter

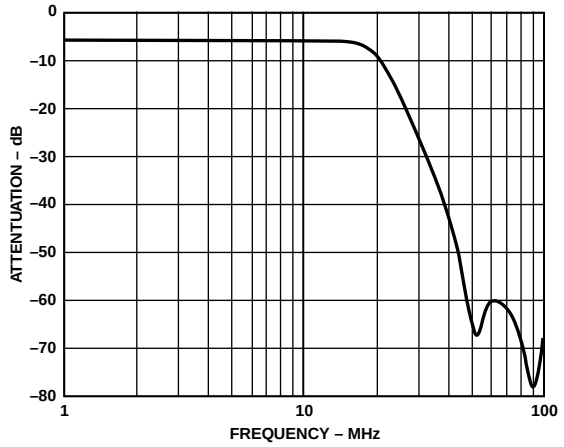


Figure 9. Frequency Response of 20 MHz Baseband Low-Pass Filter

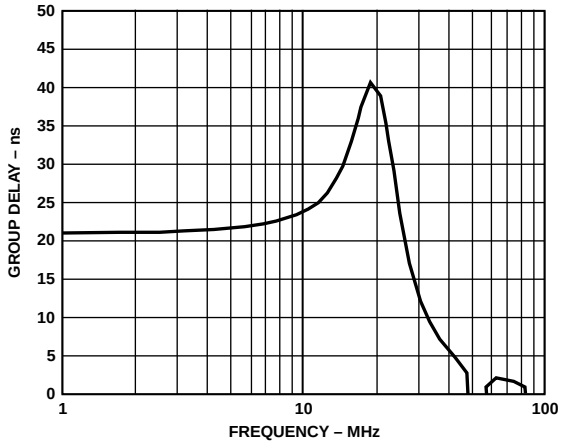


Figure 10. Group Delay of 20 MHz Baseband Low-Pass Filter

If the VGA is operating in AGC mode, the detector input (VDT1/VDT2) can be tied either to the input or output of the filter. Connecting the detector input to the input of the filter (i.e., IMXO and QMXO) will cause the VGA leveling point to be determined by the composite of the wanted signal and any unfiltered components such as blockers or signal harmonics. Connecting VDT1/VDT2 to the *outputs* of the filters ensures that the leveling point of the AGC circuit is based upon the amplitude of the filtered output only. The latter option is more desirable as it results in a more constant baseband output. However, when using this method, the leveling point of the AGC should be set so that out-of-band blockers do not overdrive the mixer output.

DC Offset Compensation

Feedthrough of the LO signal to the RF input port results in self-mixing of the LO signal. This produces a dc component at the mixer output that is frequency-dependent.

The AD8347 includes an internal circuit which actively nulls out any dc offsets that appear at the mixer output. The dc-bias level of the mixer output (which should ideally be equal to V_{VREF}, the bias level for the baseband sections of the chip) is continually being compared to V_{VREF}. Any differences between the mixer output level and V_{VREF}, will force a compensating voltage on to the mixer output.

The time constant of this correction loop is set by the capacitors which are connected to pins IOFS and QOFS (each output can be compensated separately). For normal operation 0.1 µF capacitors are recommended. The corner frequency of the compensation loop is given approximately by the equation

$$f_{3\,dB} = \frac{40}{C_{OFS}}\left(C_{OFS}\ in\ \mu F\right)$$

The corner frequency must be set to a frequency that is much lower than the symbol rate of the demodulated data. This prevents the compensation loop from falsely interpreting the data stream as a changing offset voltage.

To disable the offset compensation circuits, IOFS and QOFS should be tied to VREF.

Evaluation Board

Figure 11 shows the schematic of the AD8347 evaluation board. Note that uninstalled components are indicated with the "open" designation. The board is powered by a single supply in the range of 2.7 V to 5.5 V. Table I details the various configuration options of the evaluation board.

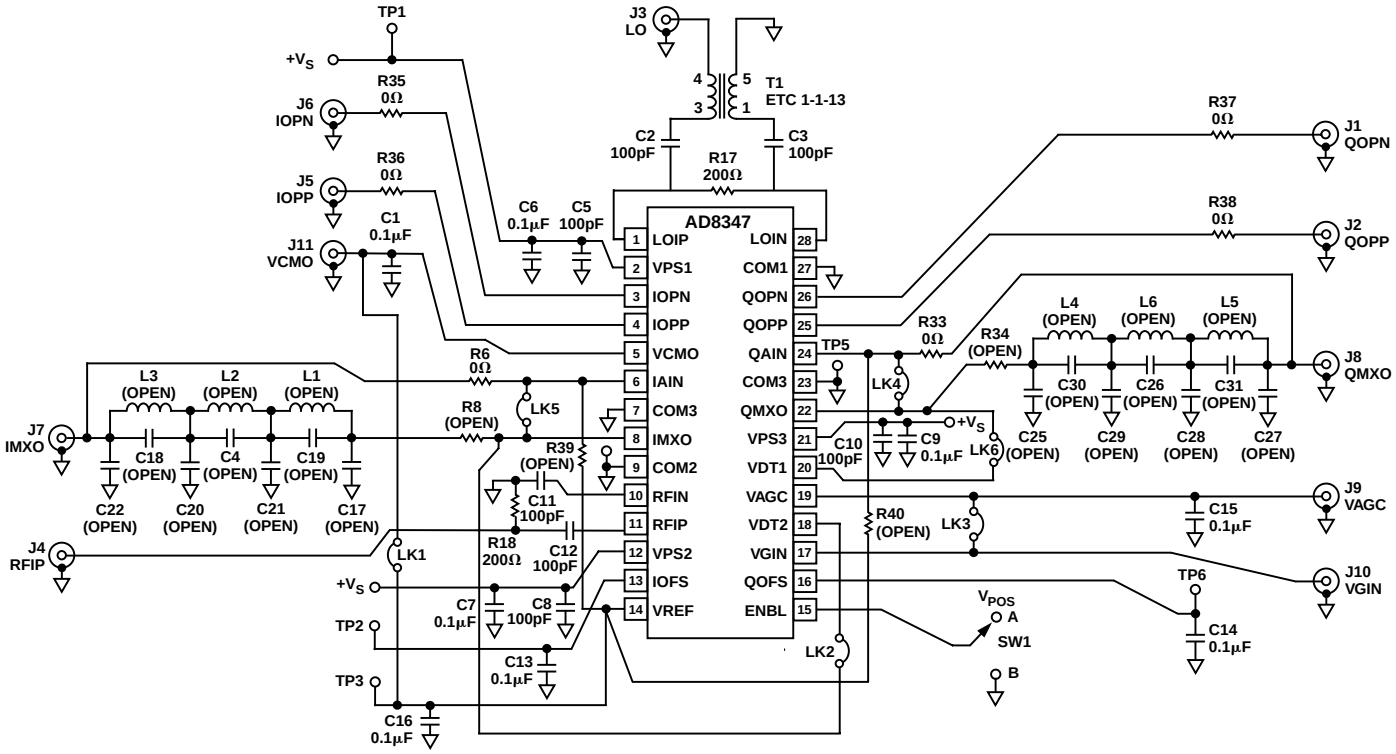


Figure 11. Evaluation Board Schematic

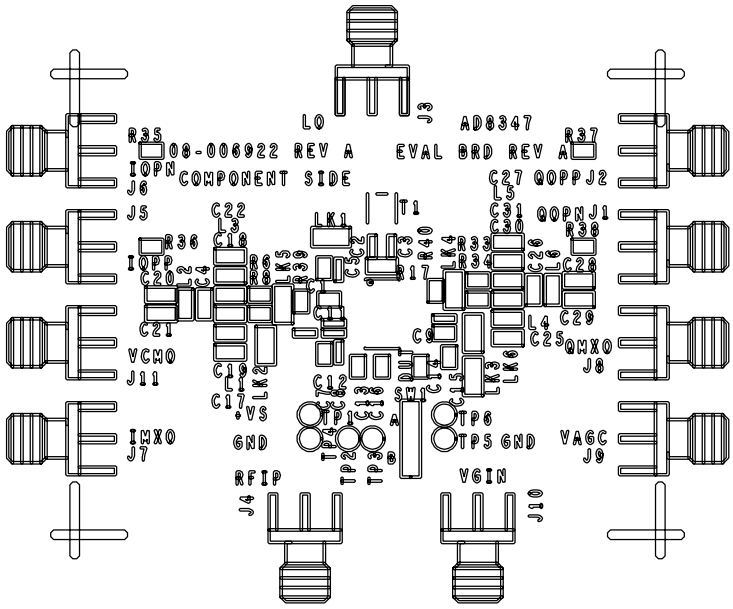


Figure 12. Silkscreen of Component Side

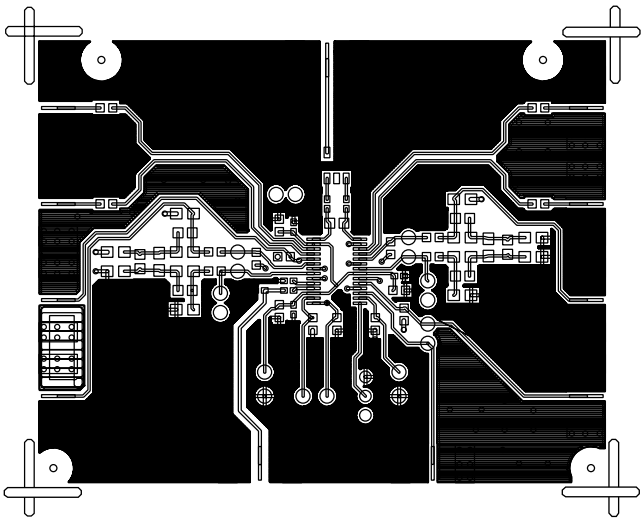


Figure 13. Layout of Component Side

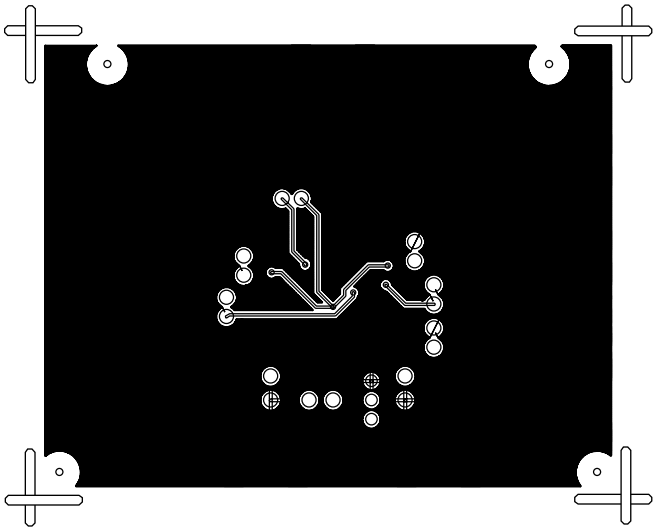


Figure 14. Layout of Circuit Side

Table I. Evaluation Board Configuration Options

Component	Function	Default Condition
TP1, TP4, TP5	Power Supply and Ground Vector Pins	Not Applicable
TP2, TP6	IOFS and QOFS Probe Points	Not Applicable
TP3	VREF Probe Point	Not Applicable
LK1, J11	Baseband Amplifier Output Bias: Installing this link connects VREF to VCMO. This sets the bias level on the baseband amplifiers to VREF, which is equal to approximately 1 V. Alternatively, the bias level of the baseband amplifiers can be set by applying an external voltage to SMA connector J11.	LK1 Installed
LK2, LK6, LK3, J9, J10	AGC Mode: Installing LK2 and LK6 connects the mixer outputs IMXO and QMXO to the detector inputs VDT2 and VDT1. By installing LK3, which connects VGIN to VAGC, the AGC mode is activated. The AGC voltage can be observed on SMA connector J9. With LK3 removed, the gain control signal for the internal variable gain amplifiers should be applied to SMA connector J10.	LK2, LK6, LK3 Installed
LK4, LK5 R6, R33, L1–L5 C4, C17–C22, C25–C31 R8, R34, R39, R40	Baseband Filtering: Installing LK4 and LK5, connects the mixer outputs IMXO and QMXO directly to the baseband amplifier inputs IAIN and QAIN. With R6 and R33 installed (0 Ω), IAIN and QAIN can be observed on SMA connectors J7 and J8. By removing LK4 and LK5 and installing R8 and R34, LC filters can be inserted between the mixer outputs and the baseband amplifier inputs. R8 and R34 can be used to increase the effective output impedance of IMXO and QMXO. (These outputs have low output impedances.) R39 and R40 can be used to provide terminations for the filter at IAIN and QAIN. (IAIN and QAIN are high impedance inputs.) R39 and R40 are terminated to VREF.	LK4, LK5 Installed R6 = R33 = 0 Ω (Size 0603) L1–L5 = Open (Size 0805) C4, C17–C22, C25–C31 = Open (Size 0805) R8 = R34 = Open (0603) R39 = R40 = Open (0603)
R35, R36, R37, R38	Baseband Amplifier Output Series Resistors	R35 = R36 = R37 = R38 = 0 Ω (Size 0603)
SW1	Device Enable: When in position A, the ENBL pin is connected to $+V_S$ and the AD8347 is in operating mode. In position B, the ENBL pin is grounded, putting the device in power-down mode.	SW1 = A

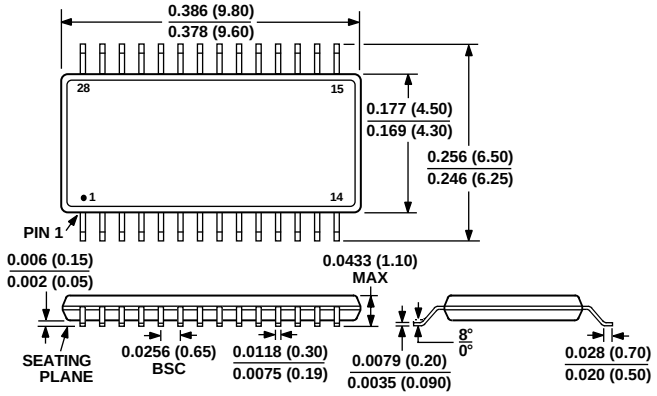
C02675–.8–10/01(0)

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

28-Lead TSSOP

(RU-28)



PRINTED IN U.S.A.