

Description

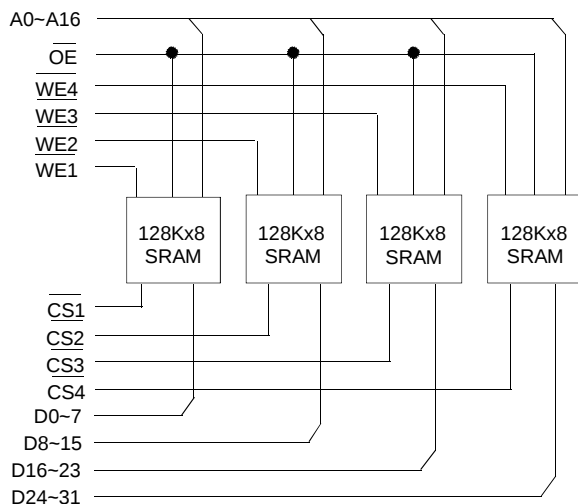
Available in PGA (PUMA 2), JLCC (PUMA 67) and Gullwing (PUMA 77) footprints. The PUMA **S4000 is a 4 Mbit SRAM module, user configurable as 128K x 32, 256K x 16 or 512K x 8. The device is available with fast access times of 20, 25 and 30ns. A low power standby and Data Retention mode is available. The device may be screened in accordance with MIL-STD-883C.

Features

- 4 Megabit SRAM module.
- Fast Access Times of 20/25/35 ns.
- Output Configurable as 32 / 16 / 8 bit wide.
- Upgradeable footprint.
- Operating Power 3740 / 2310 / 1595 mW (Max). Low Power Standby (L version) 220 mW (Max).
- 3.0V Battery Back-up Capability.
- TTL Compatible Inputs and Outputs.
- May be screened in accordance with MIL-STD-883.
- PUMA 2 - 66 pin ceramic PGA.
- PUMA 67 - 68 pin ceramic JLCC.
- PUMA 77 - 68 pin ceramic Gullwing.

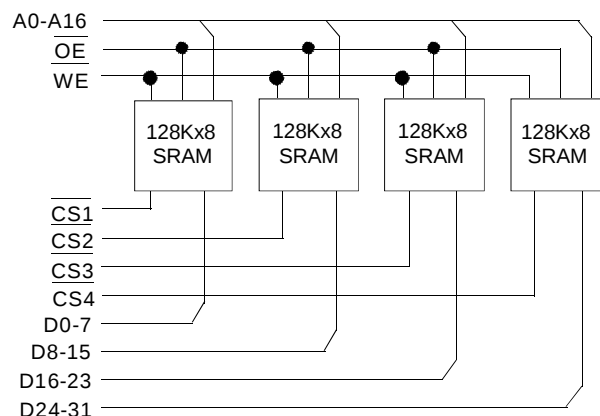
Block Diagram

PUMA 2S4000, 67S4000A and 77S4000A



Block Diagram

PUMA 67S4000 and 77S4000



Pin Functions

A0~A16 Address Input
CS1~4 Chip Select
OE Output Enable
GND Ground

D0~D31 Data Inputs/Outputs
WE1~4 Write Enables
Vcc Power (+5V)

DC OPERATING CONDITIONS**Absolute Maximum Ratings** ⁽¹⁾

Voltage on any pin relative to GND ⁽²⁾	V_T	-0.5V to +7.0	V
Power Dissipation	P_T	4	W
Storage Temperature	T_{STG}	-65 to +150	°C

Notes (1) Stresses above those listed may cause permanent damage. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

(2) Pulse width: -3.0V for less than 10ns.

Recommended Operating Conditions

		<i>min</i>	<i>typ</i>	<i>max</i>	
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Input High Voltage	V_{IH}	2.2	-	6.0	V
Input Low Voltage	V_{IL}	-0.5	-	0.8	V
Operating Temperature	T_A	0	-	70	°C
	T_{AI}	-40	-	85	°C (Suffix I)
	T_{AM}	-55	-	125	°C (Suffix M, MB)

DC Electrical Characteristics ($V_{CC}=5V\pm10\%$, $T_A=-55^\circ\text{C}$ to $+125^\circ\text{C}$)

Parameter	Symbol	Test Condition	<i>min</i>	<i>typ</i>	<i>max</i>	Unit
Input Leakage Current	I_{LI1}	$V_{IN}=0V$ to V_{CC}	-8	-	8	μA
Output Leakage Current	I_{LO}	$\overline{CS}^{(1)}=V_{IH}$ or $\overline{OE}=V_{IH}$, $V_{IO}=0V$ to V_{CC} $\overline{WE}=V_{IL}$	-8	-	8	μA
Operating Supply Current	32 bit I_{CC32}	Min cycle, duty=100%, $I_{IO}=0\text{mA}$, $\overline{CS}=V_{IL}$	-	-	680	mA
	16 bit I_{CC16}	As above	-	-	420	mA
	8 bit I_{CC8}	Min cycle, duty=100%, $I_{IO}=0\text{mA}$, $\overline{CS}=V_{IL}$	-	-	290	mA
Standby Supply Current (TTL)	I_{SB1}	$\overline{CS}^{(1)} \geq V_{IH}$, $V_{CC} = 5.5V$	-	-	160	mA
-L Version	I_{SB2}	$\overline{CS}^{(1)} \geq V_{IH}$, $V_{IL} \leq V_{IN} \leq V_{IH}$, $f = 0\text{ Hz}$	-	-	40	mA
Output Voltage Low	V_{OL}	$I_{OL} = 8.0\text{mA}$	-	-	0.4	V
Output Voltage High	V_{OH}	$I_{OH} = -4.0\text{mA}$	2.4	-	-	V

Notes: (1) $\overline{CS}$ and $\overline{WE}$ above are accessed through $\overline{CS1-4}$ and $\overline{WE1-4}$ respectively. These inputs must be operated simultaneously for 32 bit mode, in pairs for 16 bit mode and singly for 8 bit mode.

Capacitance ($V_{CC}=5V\pm10\%$, $T_A=25^\circ\text{C}$) Note: (1) On the standard module, $\overline{WE} = 30\text{ pF}$ max.

Parameter	Symbol	Test Condition	<i>typ</i>	<i>max</i>	Unit
Input Capacitance Address, $\overline{OE}$	C_{IN1}	$V_{IN}=0V$	-	30	pF
$\overline{WE1-4}^{(1)}$, $\overline{CS1-4}$	C_{IN2}	$V_{IN}=0V$	-	16	pF
I/O Capacitance D0-D31	C_{IO}	$V_{IO}=0V$	-	30	pF (8 bit mode)

These parameters are calculated, not measured.

Operating Modes

The table below shows the logic inputs required to control the operating modes of each of the SRAMs on the modules.

Mode	$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	V_{CC} Current	I/O Pin	Reference Cycle
Not Selected	1	X	X	I_{SB1}, I_{SB2}	High Z	Power Down
Output Disable	0	1	1	I_{CC}	High Z	-
Read	0	0	1	I_{CC}	D_{OUT}	Read Cycle
Write	0	X	0	I_{CC}	D_{IN}	Write Cycle

1 = V_{IH} ,

0 = V_{IL} ,

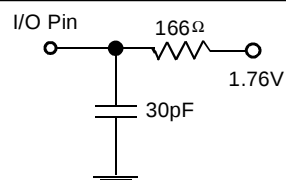
X = Don't Care

Note: $\overline{CS}$ above is accessed through $\overline{CS1-4}$ (and $\overline{WE}$ by $\overline{WE1-4}$ on the PUMA 2S4000, 67S4000A, 77S4000A). For correct operation, $\overline{CS1-4}$ (and $\overline{WE1-4}$) must operate simultaneously for 32 bit operation, in pairs for 16 bit operation, or singly for 8 bit operation.

AC Test Conditions

Output Load

- *Input pulse levels: 0.0V to 3.0V
- *Input rise and fall times: 3 ns
- *Input and Output timing reference levels: 1.5V
- * $V_{CC} = 5V \pm 10\%$
- *PUMA module is tested in 32 bit mode.



Low V_{CC} Data Retention Characteristics - L Version Only ($T_A = -55^\circ\text{C}$ to $+125^\circ\text{C}$)

Parameter	Symbol	Test Condition	min	typ	max	Unit
V_{CC} for Data Retention	V_{DR}	$\overline{CS1-4} \geq V_{CC} - 0.2V$	2	-	-	V
Data Retention Current	I_{CCDR}	$V_{CC} = 3.0V, \overline{CS1-4} \geq V_{CC} - 0.2V,$ $V_{IN} \geq V_{CC} - 0.2V$ or $\leq 0.2V$	-	-	20	mA
Chip Deselect to Data Retention	t_{CDR}	See Retention Waveform	-	-	-	ns
Operation Recovery Time	t_R	See Retention Waveform	-	-	-	ns

AC OPERATING CONDITIONS**Read Cycle**

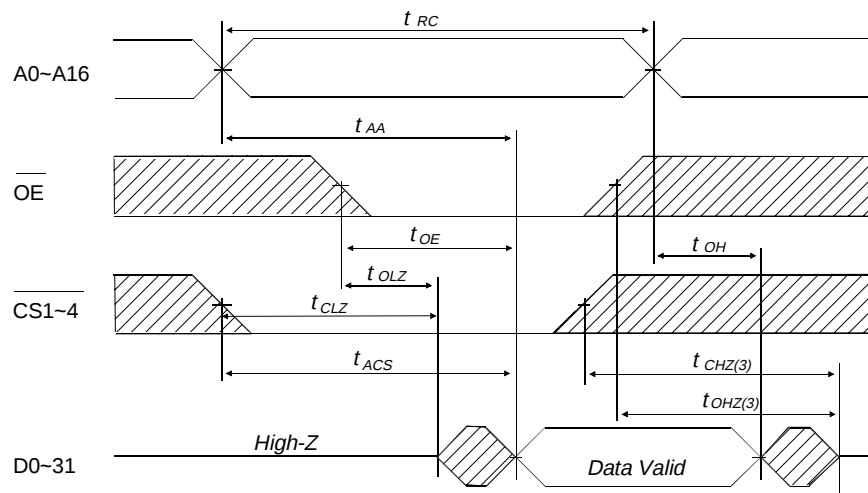
<i>Parameter</i>	<i>Symbol</i>	<i>020</i>		<i>025</i>		<i>35</i>		<i>Units</i>
		<i>min</i>	<i>max</i>	<i>min</i>	<i>max</i>	<i>min</i>	<i>max</i>	
Read Cycle Time	t_{RC}	20	-	25	-	35	-	ns
Address Access Time	t_{AA}	-	20	-	25	-	35	ns
Chip Select Access Time	t_{ACS}	-	20	-	25	-	35	ns
Output Enable to Output Valid	t_{OE}	-	9	-	8	-	12	ns
Output Hold from Address Change	t_{OH}	5	-	5	-	5	-	ns
Chip Selection to Output in Low Z	t_{CLZ}	6	-	5	-	5	-	ns
Output Enable to Output in Low Z	t_{OLZ}	0	-	0	-	0	-	ns
Chip Deselection to Output in High Z ⁽³⁾	t_{CHZ}	0	9	-	15	-	15	ns
Output Disable to Output in High Z ⁽³⁾	t_{OHZ}	0	9	-	15	-	15	ns

Write Cycle

<i>Parameter</i>	<i>Symbol</i>	<i>020</i>		<i>025</i>		<i>35</i>		<i>Unit</i>
		<i>min</i>	<i>max</i>	<i>min</i>	<i>max</i>	<i>min</i>	<i>max</i>	
Write Cycle Time	t_{WC}	20	-	25	-	35	-	ns
Chip Selection to End of Write	t_{CW}	15	-	16	-	20	-	ns
Address Valid to End of Write	t_{AW}	15	-	16	-	20	-	ns
Address Setup Time	t_{AS}	0	-	0	-	0	-	ns
Write Pulse Width	t_{WP}	15	-	15	-	20	-	ns
Write Recovery Time	t_{WR}	0	-	5	-	5	-	ns
Data to Write Time Overlap	t_{DW}	0	15	10	-	15	-	ns
Output Active from End of Write	t_{OW}	15	-	3	-	3	-	ns
Data Hold from Write Time	t_{DH}	2*	-	2*	-	2*	-	ns
Write to Output High Z	t_{WHZ}	5	-	0	10	0	10	ns

* Note : Only applies to PUMA 67S4000/A otherwise t_{DH} (min) = 0

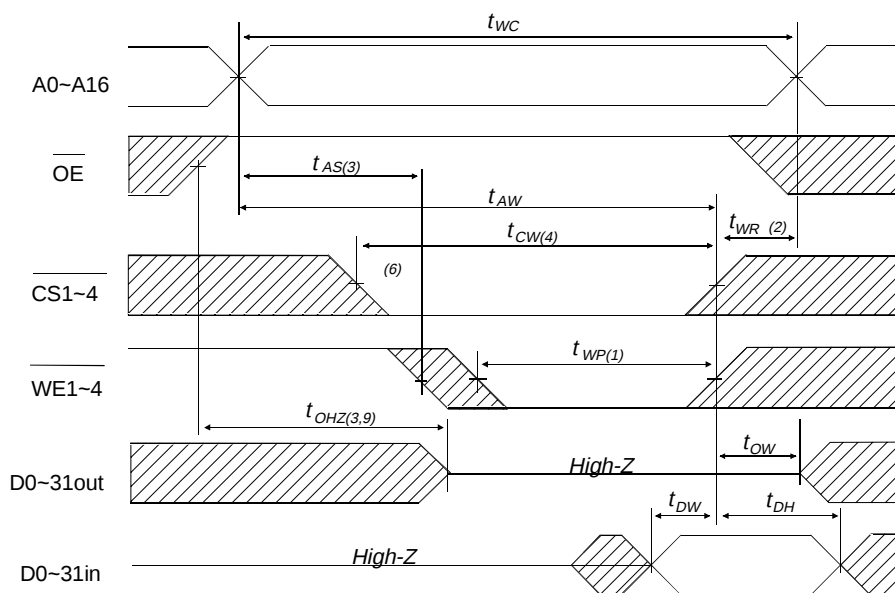
Read Cycle Timing Waveform ^(1,2)



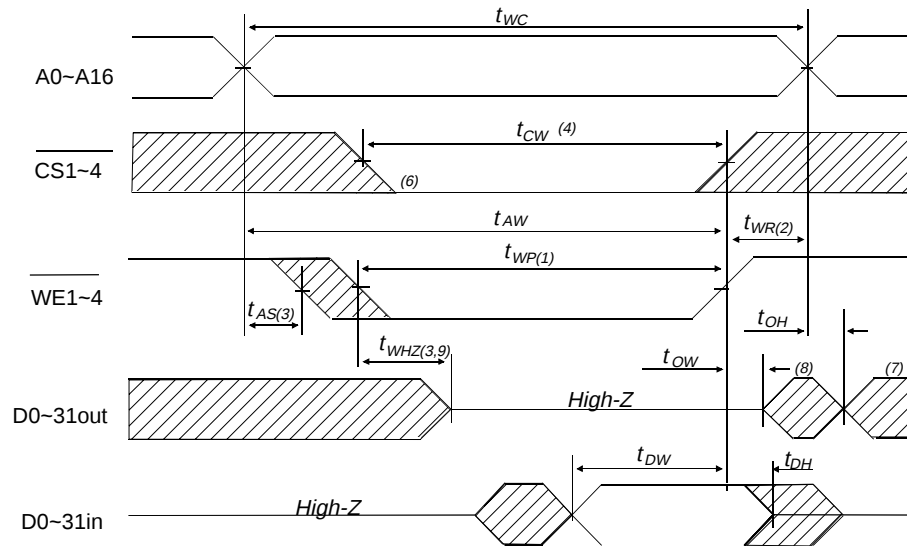
Notes:

- (1) During the Read Cycle, $\overline{WE}$ is high for the modules.
- (2) Address valid prior to or coincident with $\overline{CS}$ transition Low.
- (3) t_{CHZ} and t_{OHZ} are defined as the time at which the outputs achieve the open circuit conditions and are not referenced to output voltage levels. These parameters are sampled and not 100% tested.

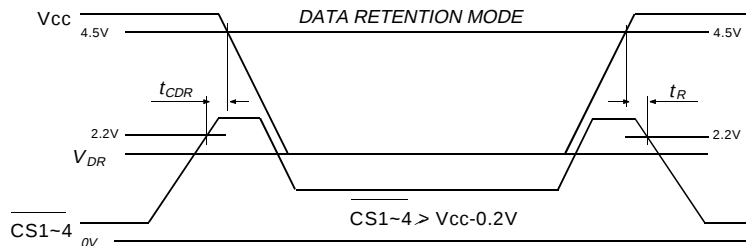
Write Cycle No.1 Timing Waveform



Write Cycle No.2 Timing Waveform ⁽⁵⁾



Low V_{CC} Data Retention Timing Waveform



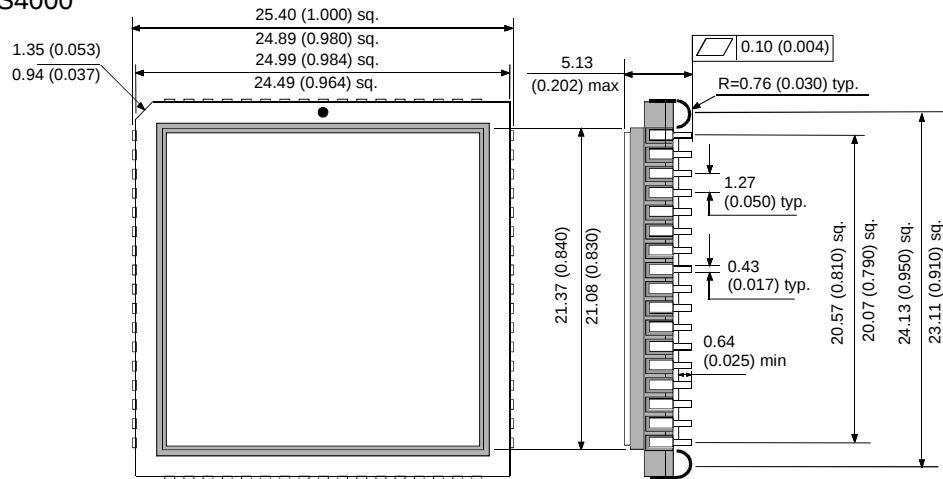
AC Characteristics Notes

- (1) A write occurs during the overlap (t_{WP}) of a low $\overline{CS}$ and a low $\overline{WE}$.
- (2) t_{WR} is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ going high to the end of write cycle.
- (3) During this period, I/O pins are in the output state. Input signals out of phase must not be applied.
- (4) If the $\overline{CS}$ low transition occurs simultaneously with the $\overline{WE}$ low transition or after the $\overline{WE}$ low transition, outputs remain in a high impedance state.
- (5) $\overline{OE}$ is continuously low. ($\overline{OE}=V_{IL}$)
- (6) D_{OUT} is in the same phase as written data of this write cycle.
- (7) D_{OUT} is the read data of next address.
- (8) If $\overline{CS}$ is low during this period, I/O pins are in the output state. Input signals out of phase must not be applied.
- (9) t_{WHZ} and t_{OHZ} are defined as the time at which the outputs achieve the open circuit conditions and are not referenced to output voltage levels. These parameters are sampled and not 100% tested.

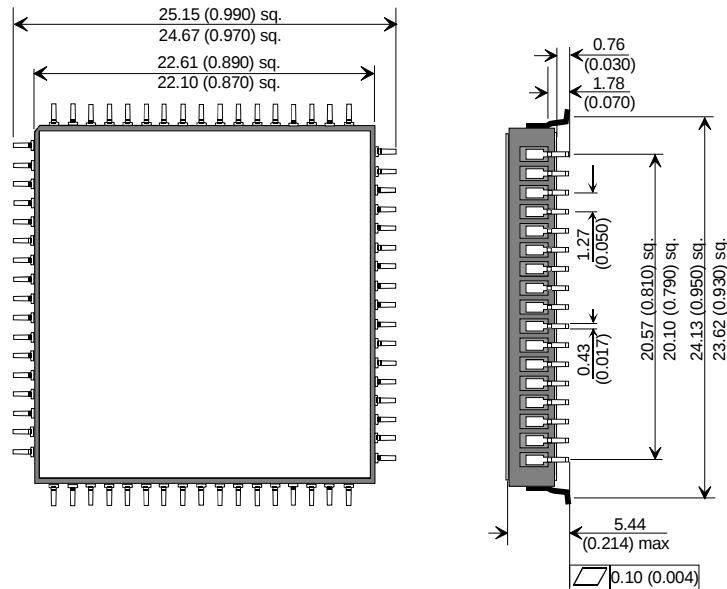
$\overline{WE}$ above refers to $\overline{WE1-4}$ on the PUMA 2S4000, 67S4000A AND 77S4000A.

Package Details

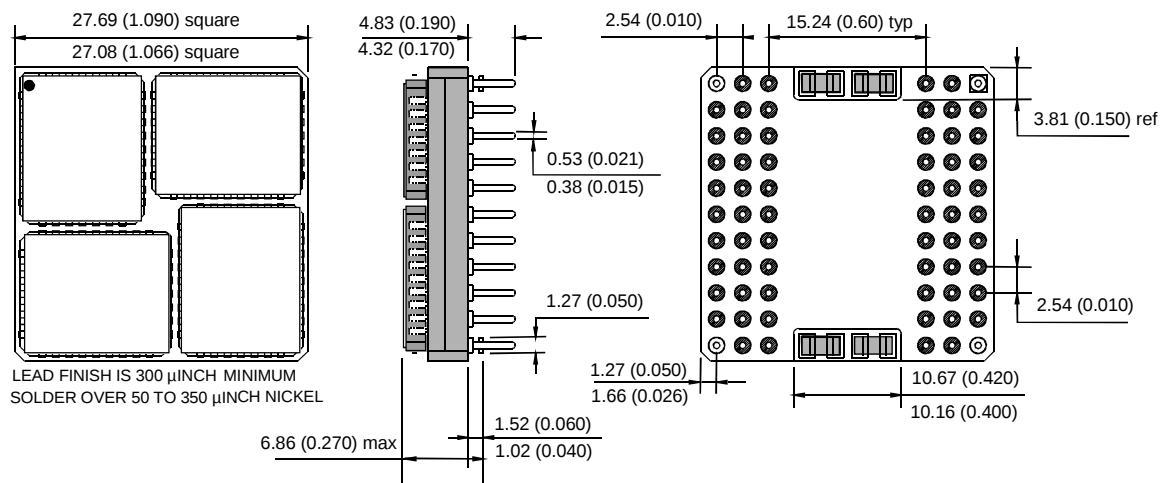
PUMA 67S4000



PUMA 77S4000

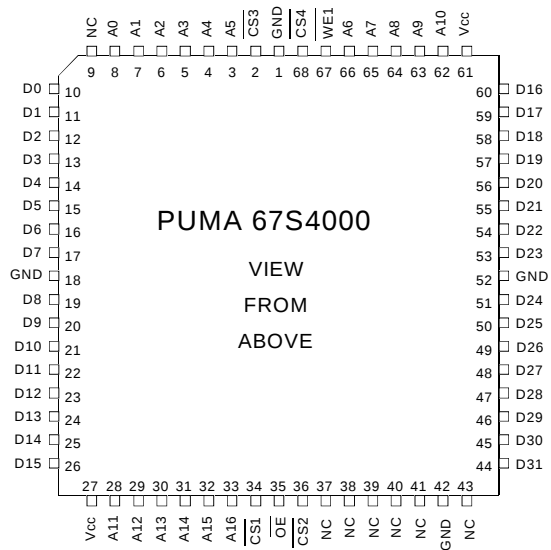


PUMA 2S4000

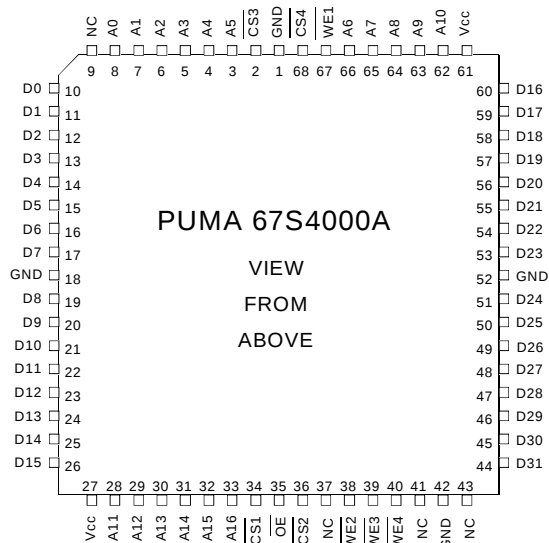


Pin Definitions

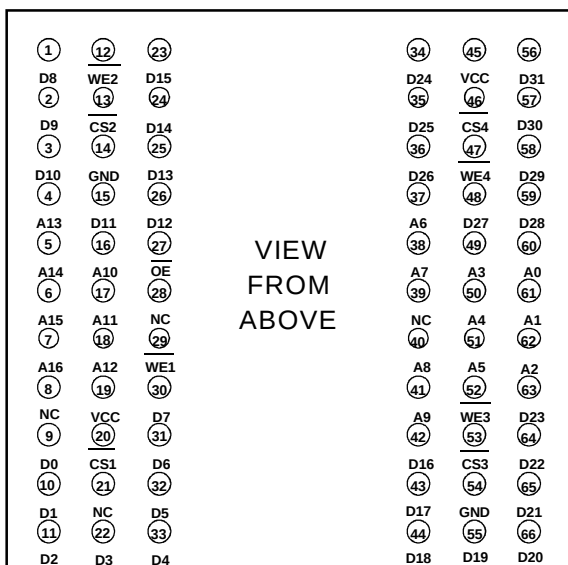
PUMA 67S4000 / PUMA 77S4000



PUMA 67S4000A / PUMA 77S4000A



PUMA 2S4000



SCREENING**Military Screening Procedure**

MultiChip Screening Flow for high reliability product is in accordance with Mil-883 method 5004 .

MB MULTICHIP MODULE SCREENING FLOW		
SCREEN	TEST METHOD	LEVEL
Visual and Mechanical Internal visual Temperature cycle Constant acceleration	2010 Condition B or manufacturers equivalent 1010 Condition C (10 Cycles, -65°C to +150°C) 2001 Condition B (Y1 & Y2) (10,000g)	100% 100% 100%
Burn-In Pre-Burn-in electrical Burn-in	Per applicable device specifications at $T_A = +25^\circ\text{C}$ $T_A = +125^\circ\text{C}$, 160hrs minimum.	100% 100%
Final Electrical Tests Static (DC) Functional Switching (AC)	Per applicable Device Specification a) @ $T_A = +25^\circ\text{C}$ and power supply extremes b) @ temperature and power supply extremes a) @ $T_A = +25^\circ\text{C}$ and power supply extremes b) @ temperature and power supply extremes a) @ $T_A = +25^\circ\text{C}$ and power supply extremes b) @ temperature and power supply extremes	100% 100% 100% 100% 100% 100%
Percent Defective allowable (PDA)	Calculated at post-burn-in at $T_A = +25^\circ\text{C}$	10%
Hermeticity Fine Gross	1014 Condition A Condition C	100% 100%
Quality Conformance	Per applicable Device Specification	Sample
External Visual	2009 Per vendor or customer specification	100%

Ordering Information

PUMA 2S4000ALMB-020

	Speed	020 = 20 ns 025 = 25 ns 35 = 35 ns
	Temp. range/screening	Blank = Commercial Temperature I = Industrial Temperature M = Military Temperature MB = May be processed in accordance with MIL-STD-883
	Power Consumption	Blank = Standard Power L = Low Power
	$\overline{WE}$ Option	Blank = Single $\overline{WE}$ (PUMA 67 / 77 only) $\overline{WE1-4}$ (PUMA 2 only) A = $\overline{WE1-4}$ (PUMA 67 / 77 only)
	Organisation	4000 = 128Kx 32, user configurable as 256K x 16 and 512K x 8
	Technology	S = SRAM MEMORY
	Package	PUMA 2 = JEDEC 66 Pin Ceramic PGA package PUMA 67 = JEDEC 68 J-Leaded Ceramic Surface Mount package PUMA 77 = JEDEC 68 Leaded Gull Wing Ceramic Surface Mount package

Note :

Although this data is believed to be accurate, the information contained herein is not intended to, and does not create any warranty of merchantability or fitness for a particular purpose.

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