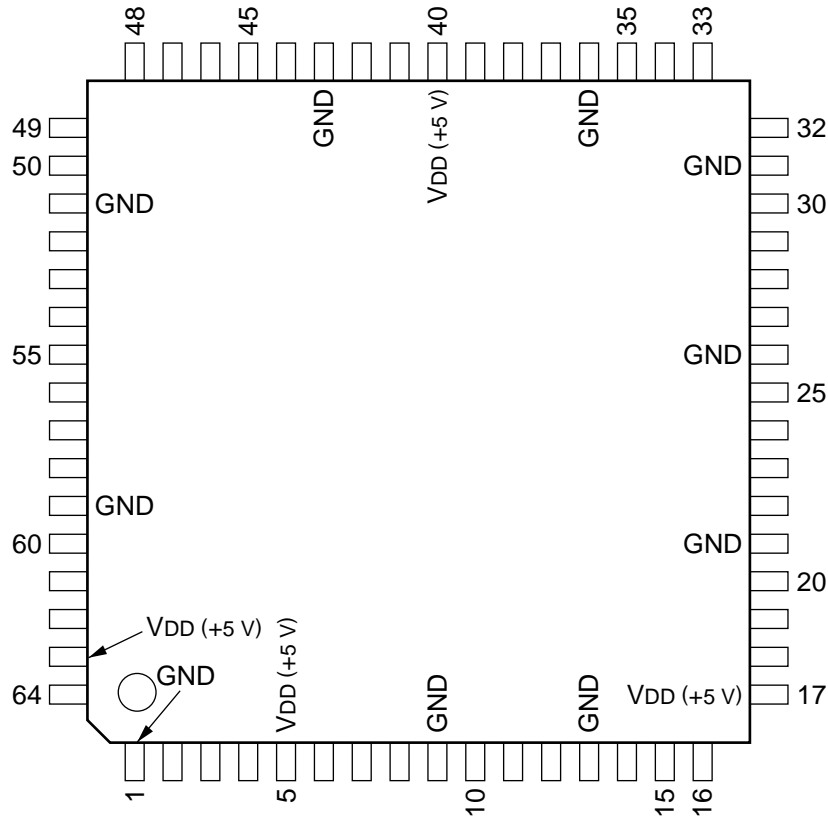

C-MOS SCSI PROTOCOL CONTROLLER

—TOP VIEW—



(VDD = +5 V)

PIN NO.	I/O	SIGNAL	PIN NO.	I/O	SIGNAL	PIN NO.	I/O	SIGNAL	PIN NO.	I/O	SIGNAL
1	—	GND	17	—	VDD	33	I/O	RST	49	I	A0
2	O	DREQ	18	I/O	SD0	34	I/O	MSG	50	I	A1
3	I	DACK	19	I/O	SD1	35	I/O	SEL	51	—	GND
4	I	DBWR	20	I/O	SD2	36	—	GND	52	I	A2-DBRD
5	—	VDD	21	—	GND	37	I/O	CD	53	I	A3-ALE
6	I/O	DB0	22	I/O	SD3	38	I/O	REQ	54	I	TESTIN
7	I/O	DB1	23	I/O	SD4	39	I/O	IO	55	I/O	PAD0
8	I/O	DB2	24	I/O	SD5	40	—	VDD	56	I/O	PAD1
9	—	GND	25	I/O	SD6	41	I	MODE	57	I/O	PAD2
10	I/O	DB3	26	—	GND	42	O	INT	58	I/O	PAD3
11	I/O	DB4	27	I/O	SD7	43	—	GND	59	—	GND
12	I/O	DB5	28	I/O	SDP	44	I	RESET	60	I/O	PAD4
13	—	GND	29	I/O	ATN	45	I	WR	61	I/O	PAD5
14	I/O	DB6	30	I/O	BSY	46	I	RD	62	I/O	PAD6
15	I/O	DB7	31	—	GND	47	I	CS	63	I/O	PAD7
16	I/O	DBP	32	I/O	ACK	48	I	CLK	64	—	VDD

INPUT

A0, A1	; ADDRESS
A2 - DBRD	; ADDRESS/READ SIGNAL FOR THE DMA DATA BUS
A3 - ALE	; ADDRESS
CLK	; CLOCK
CS	; CHIP SELECT
DACK	; DMA ACKNOWLEDGE
DBWR	; DMA WRITE SIGNAL
MODE	; MODE SELECT (PAD BUS/ADDRESS CONTROL BUS)
RD	; REGISTER READ SIGNAL
RESET	; CHIP RESET
TESTIN	; TEST
WR	; REGISTER WRITE SIGNAL

OUTPUT

DREQ	; DMA REQUEST SIGNAL
INT	; OPEN-DRAIN INTERRUPT SIGNAL

INPUT/OUTPUT

ACK	; SCSI I/O
ATN	; OPEN-DRAIN OUTPUT, SCHMITT TRIGGER INPUT
BSY	; OPEN-DRAIN SCSI I/O
CD	; SCSI PHASE SIGNAL
DB0 - DB7	; DMA DATA BUS
DBP	; ODD PARITY FOR DB0-DB7
IO	; SCSI PHASE SIGNAL
MSG	; SCSI PHASE SIGNAL
PAD0 - PAD7	; PROCESSOR ADDRESS-DATA BUS
REQ	; SCSI I/O
RST	; OPEN-DRAIN SCSI I/O
SD0 - SD7	; SCSI DATA BUS
SDP	; SCSI DATA/PARITY OUTPUT BUS
SEL	; OPEN-DRAIN SCSI I/O

