Preliminary Information

AMD-761™ System Controller

Data Sheet

Publication # **24088** Rev: **B**
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Revision History

Date	Rev	Description
8/2001	B	Public release with added bidirectional WSC# feature description. Added electricals.
5/2001	A-2	Modified descriptions of WSC# pin. NDA version only.
2/2001	A-1	Initial public release.
11/2000	A	Initial release (NDA).

1 Features

The AMD Athlon™ processor powers the next generation in computing platforms, delivering the ultimate performance for cutting-edge applications and an unprecedented computing experience.

The AMD-760™ chipset is a highly integrated system logic solution that delivers enhanced performance for the AMD Athlon™ processor and other AMD Athlon system bus-compatible processors. The AMD-760 chipset consists of the AMD-761™ system controller in a 569-pin plastic ball-grid array (PBGA) package and the AMD-766™ peripheral bus controller. The AMD-761 system controller features the AMD Athlon system bus, system memory controller, Accelerated Graphics Port (AGP) controller, and Peripheral Component Interconnect (PCI) bus controller. Figure 1 on page 5 shows a block diagram for the AMD-760 chipset.

The AMD-761 system controller is designed with the following features:

- The AMD Athlon system bus supports the high-speed, split-transaction AMD Athlon system bus interface. This bus is designed to operate at 100/200-MHz or 133/266-MHz double-data rate.
- The 33-MHz 32-bit PCI 2.2-compliant bus interface supports up to seven bus masters plus the AMD-766 peripheral bus controller.
- The 66-MHz AGP 2.0-compliant interface supports 1x, 2x, and 4x data transfer mode.
- High-speed memory—The AMD-761 system controller is designed to support DDR SDRAM DIMMs, operating at either 100/200-MHz or 133/266-MHz double-data rate. Note that the DDR interface speed is locked to the front-side bus speed.

This document describes the features and operation of the AMD-761 system controller. For a description of the AMD-766 peripheral bus controller, see the *AMD-766™ Peripheral Bus Controller Data Sheet*, order# 23167. Key features of the AMD-761 system controller are provided in this section.

1.1 AMD Athlon™ Processor System Bus

The AMD Athlon processor system bus has the following features:

- High-performance point-to-point system bus topology
- Source-synchronous clocking for high-speed transfers
- 200- or 266-MHz, split-transaction AMD Athlon system bus interface
- 1.6 Gbytes/s peak data transfer rates at 100/200 MHz, 2.1 Gbytes at 133/266 MHz
- Large 64-byte (cache line) data burst transfers

1.2 Integrated Memory Controller

The integrated memory controller has the following features:

- The AMD-761 system controller supports the following concurrencies:
  - Processor-to-main-memory with PCI-to-main-memory
  - Processor-to-main-memory with AGP-to-main-memory
  - Processor-to-PCI with PCI-to-main-memory or AGP-to-main-memory
- Memory error correcting code (ECC) support
- Supports the following DRAM:
  - Up to two unbuffered DIMMs or four registered DIMMs
  - 64-Mbit, 128-Mbit, 256-Mbit, and 512-Mbit technology
  - 64-bit data width, plus 8-bit ECC paths
  - Flexible row and column addressing
- Supports up to 4 Gbytes of memory
- Four open pages within one CS (device selected by chip select)
- BIOS-configurable memory-timing parameters and configuration parameters
- 2.5-V memory interface operation with no external buffers or PLLs
- Concurrent DRAM writeback and read-around-write
- Burst read and write transactions

- Decoupled and burst DRAM refresh with staggered CS timing
- Provides the following refresh options:
  - Programmable refresh rate
  - CAS-before-RAS
  - Populated banks only
  - Automatic refresh of idle slots—improves bus availability for memory access by the processor or system

1.3 PCI Bus Controller

The PCI bus controller has the following features:

- Compliance with *PCI Local Bus Specification,* Revision 2.2
- Supports seven PCI bus masters plus the AMD-766 peripheral bus controller
- 32-bit interface, compatible with 3.3-V and 5-V PCI I/O
- Synchronous PCI bus operation up to 33 MHz
- PCI-initiator peer concurrency
- Automatic processor-to-PCI burst cycle detection
- Zero wait-state PCI initiator and target burst transfers
- PCI-to-DRAM data streaming up to 132 Mbytes/s
- Enhanced PCI command optimization, such as Memory Read Line (MRL), Memory Read Multiple (MRM), and Memory-Write-and-Invalidate (MWI)

1.4 AGP Features

The AGP features include the following:

- Bus Features
  - Compliance with *Accelerated Graphics Port Interface Specification*, Revision 2.0
  - Synchronous 66-MHz 1x, 2x, and 4x data-transfer modes
  - Multiplexed and demultiplexed transfers
  - Up to four pipelined grants
  - Support of Sideband Address (SBA) bus

- Request Queue Features
  - Separate read-request and write-request queues
  - Reordering of high-priority requests over low-priority requests in queue
  - Simultaneous issuing of requests from both the write queue and read queue
- GART (Graphics Address Remapping Table) Features
  - Conventional (two-level) GART scheme
  - Eight-entry, fully associative GART table cache
  - Three fully associative GART directory caches

    One 4-entry for PCI

    One 8-entry for the processor

    One 16-entry for AGP

1.5 Power Management

The power management features include the following:

- Compliance support for both Advanced Configuration and Power Interface (ACPI) and Microsoft® PC 99 power management
- The AMD-761 system controller supports the following power states:
  - Processor halt/stop grant/sleep states (ACPI C1, C2)
  - ACPI S1 (power on suspend) and S3 (suspend to RAM) sleep states
  - Clock throttling with the processor's STPCLK#/stop grant mechanism

Refer to Figure 1 on page 5 for a block diagram of the AMD-760 chipset.

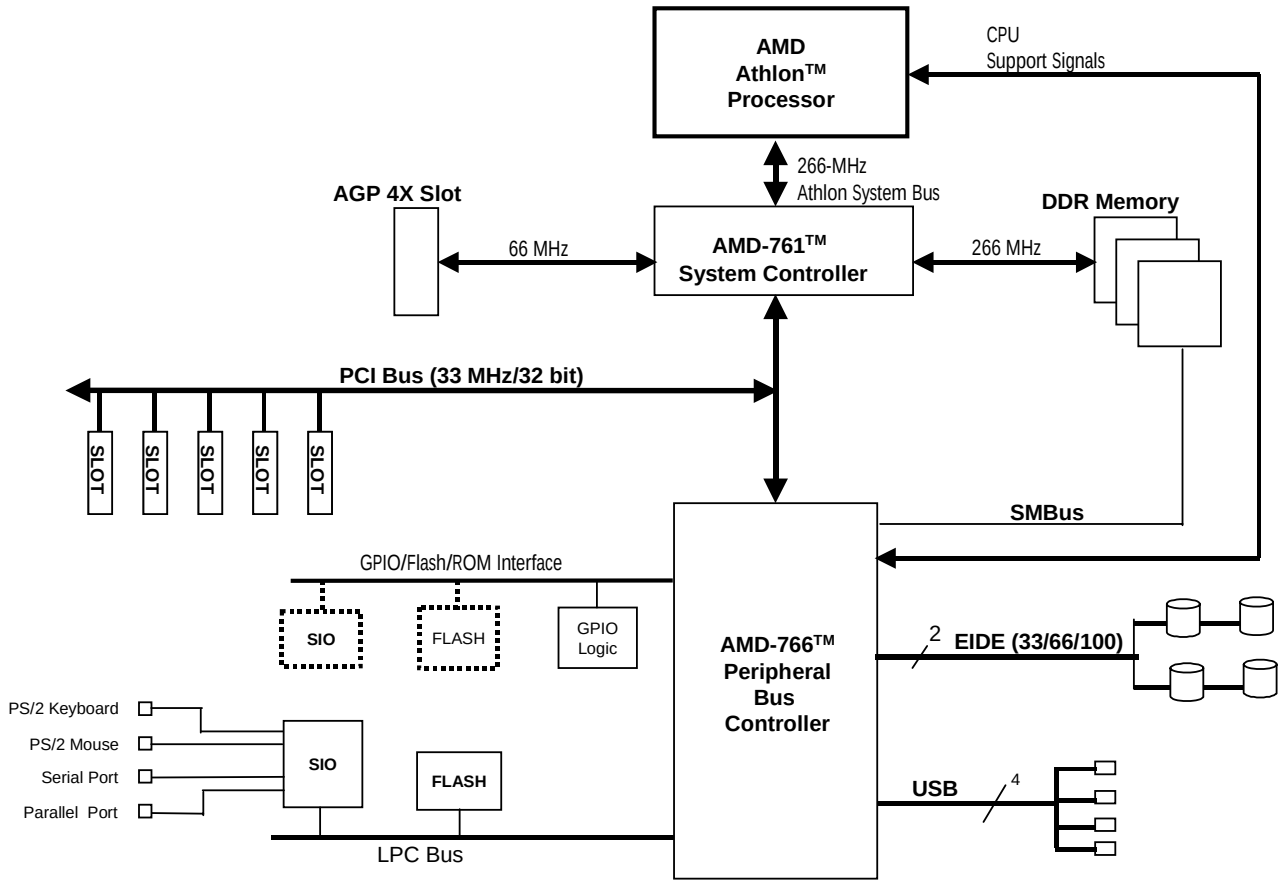


Figure 1. AMD-760™ Chipset System Block Diagram

2 Functional Operation

This chapter describes the functional operation of the AMD-761™ system controller.

2.1 Processor Interface

The AMD Athlon™ processor system bus is a high-performance, out-of-order, split-transaction bus, capable of transferring one processor command and one probe response, one chip-set response and one probe request, and one data packet simultaneously. Data and command packets are transferred as packets of two, four, or eight datums on each edge of the 100-MHz or 133-MHz clock.

2.1.1 Out of Order, Split Transaction

The split transaction bus separates the transfer of the command and the associated data into different transactions on different buses. Data may be returned in a different order than it was requested, subject to ordering rules.

A read transaction consists of a Read command sent from the processor to the memory system over the SADDOUT bus. When the memory system is ready to return data, a ReadData command is sent to the processor over the SADDIN bus to alert the processor that data is coming and identify the associated data request. The data is sent to the processor over the SDATA bus a programmable number of clocks later. Similarly, a write transaction is sent to the chipset over the SADDOUT bus, the chipset requests the associated write data over the SADDIN bus, and the data is transferred over the SDATA bus a programmable number of clocks later. Probes and probe responses are piggybacked with the other commands on the SADDIN and SADDOUT bus.

The split transaction scheme provides a high degree of parallelism between the various buses and facilitates pipeline flow or memory requests and responses.

2.1.2 Point-to-Point, Source Synchronized

All of the AMD Athlon processor system bus signals use a terminated, point-to-point topology—that is, there is one signal connection plus termination on each end of each wire. The terminated point-to-point topology allows the use of incident wave signalling, eliminating much of the time for transmission line reflections. This feature allows high-transfer speeds while maintaining high signal integrity. All data transfer is synchronized by a clock generated at the data source. The clock and data propagate over matched length paths, minimizing skew between clock and data, and the data is sampled at the destination using this forwarded clock.

Data is sampled into a FIFO at the receiver synchronous to the forwarded clock and read out of FIFO a programmable number of processor clocks later, reducing all metastability concerns. The initialization procedure establishes the location of a common ClockN on both ends of the wire to within the system wide, clock distribution skew. A data object, transmitted from one end of the wire on ClockM, is sampled into the FIFO at the other end of the wire by ClockM forwarded with the data. It is read from the FIFO by ClockM+X that is generated in the receivers clock domain, X clocks later. X is a programmed constant that accounts for the worst case propagation delay.

A detailed description of the AMD Athlon system bus, including operations, initialization, and timing can be found in the *AMD Athlon™ System Bus Specification*, order# 21902, and the *AMD Athlon™ System Bus Design Guide*, order# 22666.

2.1.3 Push-Pull Compensation

The AMD-761 system controller provides push-pull driver configuration. The push-pull driver scheme implements drivers with a user-defined output impedance. This feature allows the point-to-point signals to be source-terminated without any external devices, simplifying layout and reducing cost. In current semiconductor technology, it is not possible to implement a transistor with a tightly controlled impedance over realistic voltage, temperature, and process parameters. For this reason, a dynamic compensation scheme is implemented. For a push-pull transmission line example, see Figure 2 on page 9.

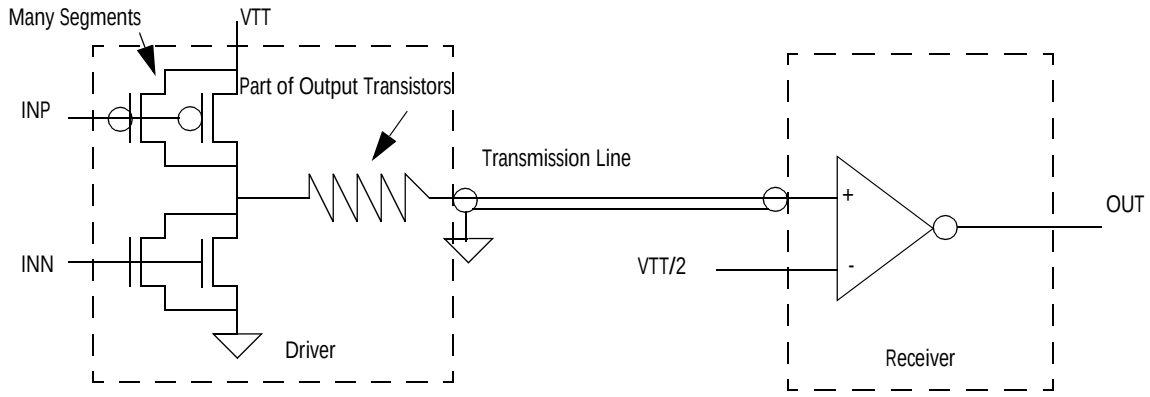


Figure 2. Push-Pull Transmission Line Example

The dynamic compensation scheme implements a dummy driver with characteristics exactly matching the normal driver. An external precision resistor is attached, and the voltage of the resulting voltage divider is compared to $V_{TT}/2$. The drive strength is then adjusted until a voltage near $V_{TT}/2$ is achieved. The output impedance then roughly matches the resistor value. Separate compensation is performed for the N and P transistors. The drive strength is changed in small steps when no data is being driven. Refer to Figure 3.

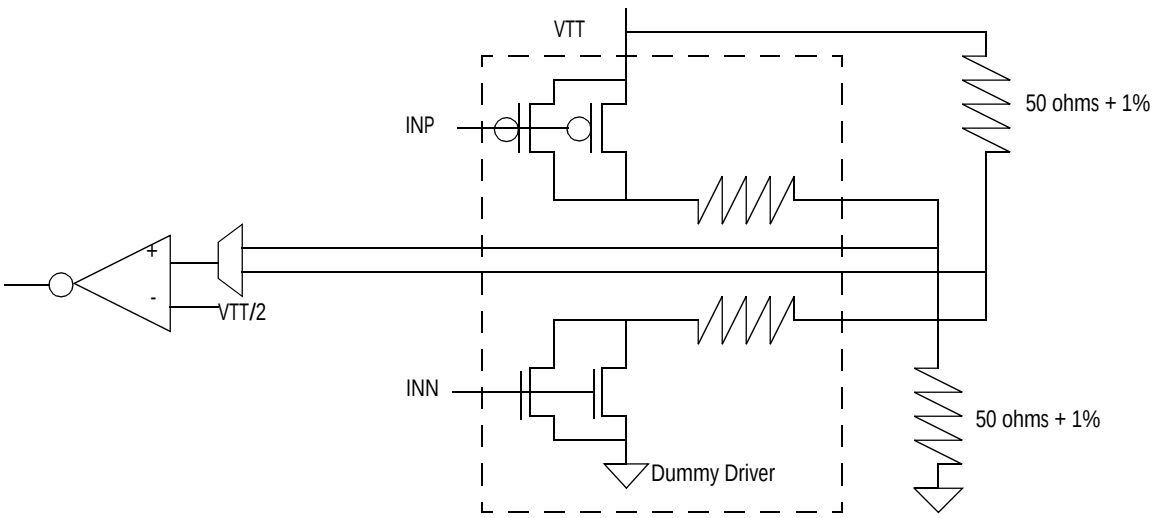


Figure 3. Dummy Load with External Compensation Resistors

2.2 Memory Interface

The AMD-761 memory controller arbitrates and optimizes incoming memory requests, handles ECC and Graphics Address Remapping Table (GART), and controls up to four double-data-rate (DDR) SDRAM DIMMs.

The AMD-761 system controller memory interface is designed to support both unbuffered and registered DDR DIMMs. Up to two unbuffered DIMMs or four registered DIMMs can be supported by the AMD-761 system controller. The AMD-761 system controller does not allow DIMM types to be mixed on the same motherboard. All DIMMs on the motherboard must be either unbuffered or registered.

The AMD-761 system controller supports 64-Mbit, 128-Mbit, 256-Mbit, and 512-Mbit DDR devices. Device widths of x4, x8, and x16 are supported (x4 supported only for registered DIMMs). Mixed banks are supported, meaning that a x8 DIMM can coexist with x4 and x16, etc.

DDR timing parameters are programmable via the AMD-761 system controller's memory controller configuration registers, allowing support of different DIMM configurations and loading. Refresh is also programmable, with support of various refresh rates as well as the ability to queue up to four outstanding refreshes. Clock pairs can also be selectively disabled to unpopulated DIMM slots via configuration register bits in the memory controller.

The memory controller supports up to four open pages in the active chip select. All pages in a chip select are closed when an access to another chip select is detected. Memory page operation can be further optimized by programming the number of idle cycles to a bank before the bank is automatically precharged.

Unbuffered DIMMs Support

Refer to Table 1 on page 11 for the total memory sizes for various unbuffered DIMM configurations. A total of 2 Gbytes is supported with unbuffered DIMMs.

Table 1. Total Memory Sizes With Unbuffered DIMMs

Devices Used On DIMM	1 DIMM (2 Rows) x64/x72	2 DIMMs (2 Rows Each) x64/x72
64 Mbit (2M x 8 x 4 banks)	128 Mbytes	256 Mbytes
64 Mbit (1M x 16 x 4 banks)	64 Mbytes	128 Mbytes
128 Mbit (4M x 8 x 4 banks)	256 Mbytes	512 Mbytes
128 Mbit (2M x 16 x 4 banks)	128 Mbytes	256 Mbytes
256 Mbit (8M x 8 x 4 banks)	512 Mbytes	1 Gbytes
256 Mbit (4M x 16 x 4 banks)	256 Mbytes	512 Mbytes
512 Mbit (16M x 8 x 4 banks)	1 Gbytes	2 Gbytes
512 Mbit (8M x 16 x 4 banks)	512 Mbytes	1 Gbytes

Figure 4 on page 12 shows the AMD-761 system controller connection to unbuffered DIMMS. Unbuffered DIMM support requires only four chip selects to support a maximum of two DIMMs. Only two unbuffered DIMMs are supported due to the heavy loading of the DDR signals by unbuffered DIMMs. The AMD-761 system controller provides six differential clock pairs, three for each unbuffered DIMM.

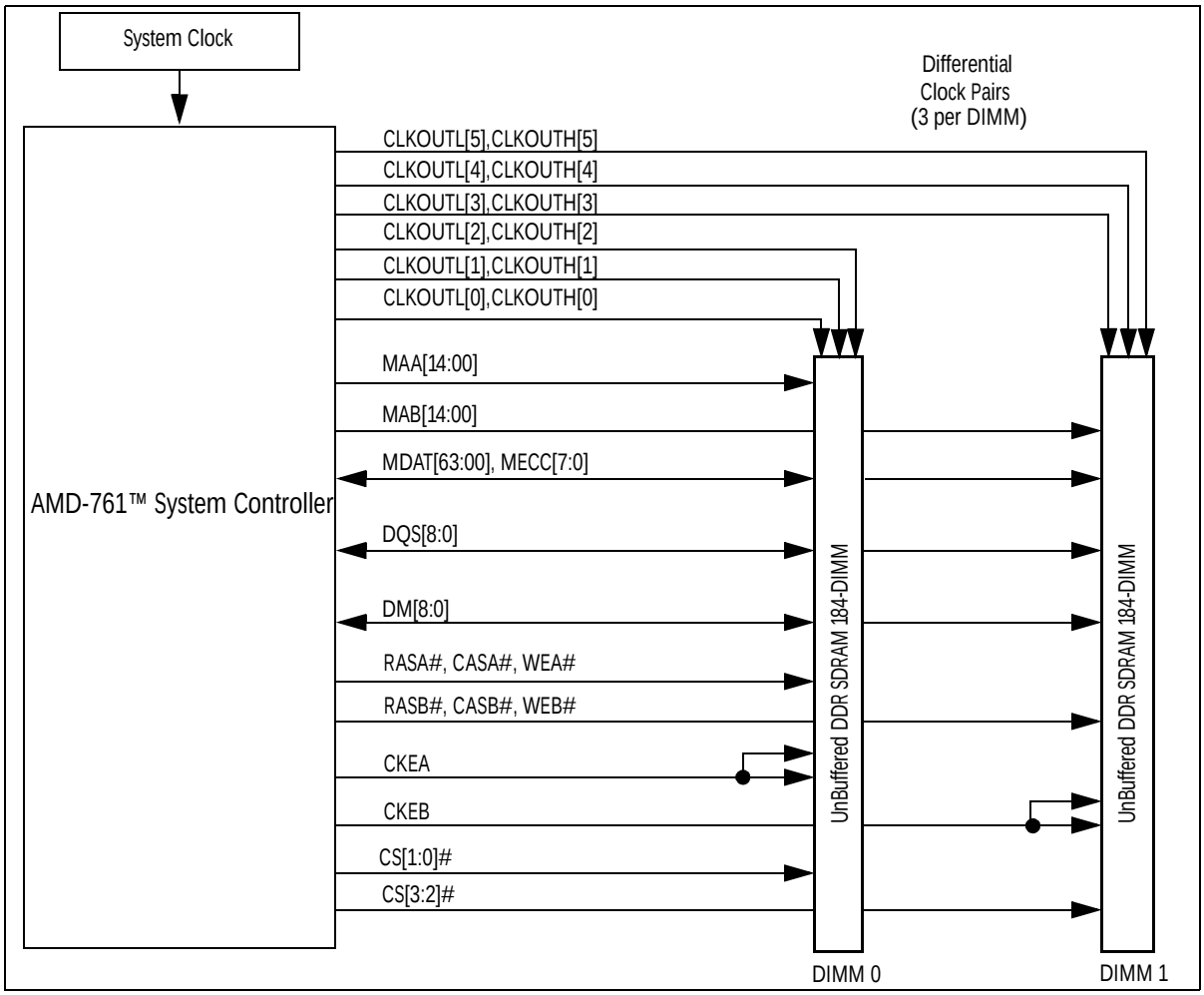


Figure 4. AMD-761™ System Controller Connection to Unbuffered DIMMs

Registered DIMMs Support

Support of four registered DIMMs is accomplished by the AMD-761 system controller's eight DDR chip-select pins (CS[7:0]#), which allow DIMMs with two chip selects, as illustrated in Figure 5 on page 13. In this example, each DIMM contains two physical DRAM banks, thus two chip selects are routed to the DIMM. The AMD-761 system controller provides one differential clock pair for each registered DIMM.

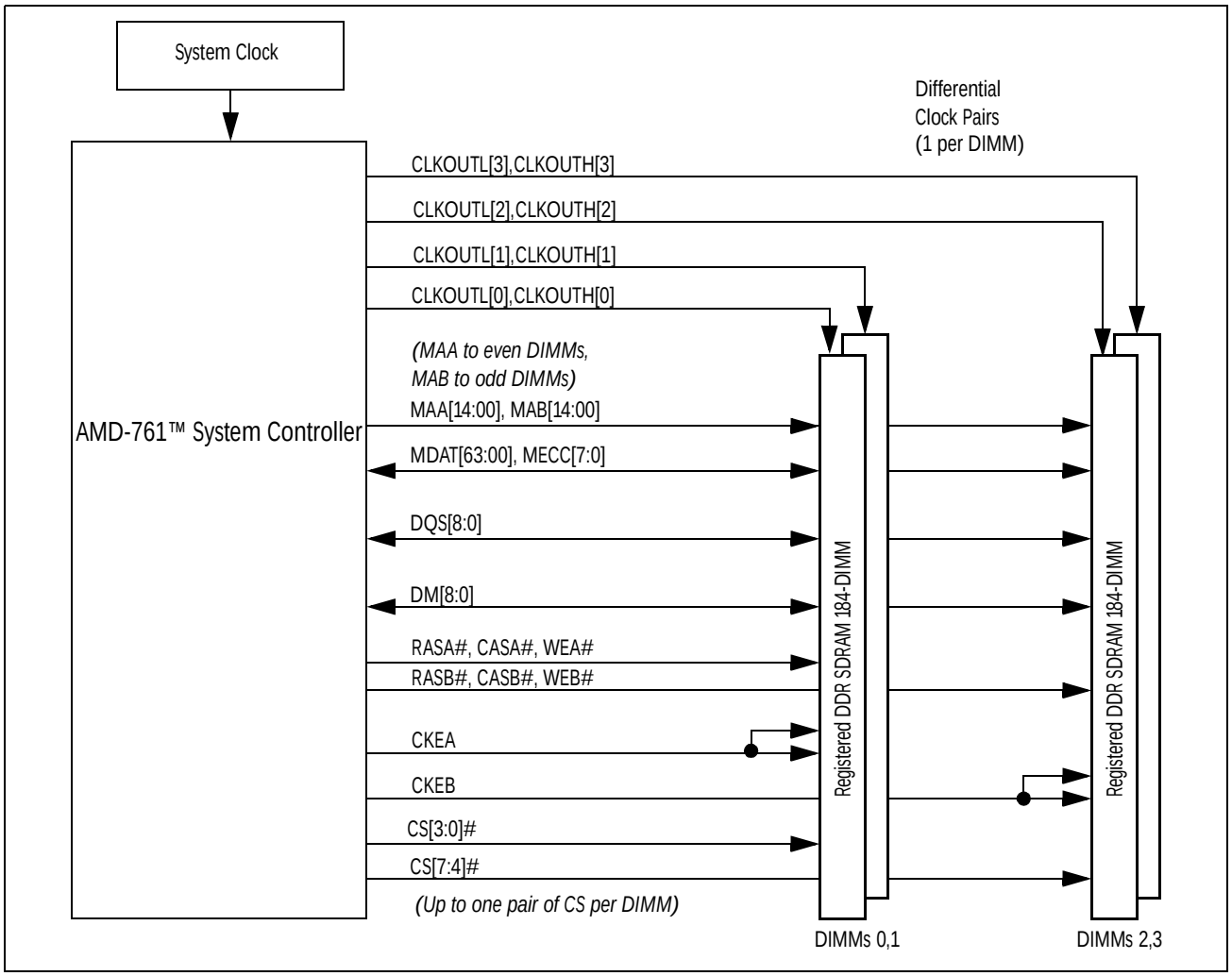


Figure 5. AMD-761™ System Controller Connection to Registered DIMMs

A total of 4 Gbytes is supported with registered DIMMs. Refer to Table 2 on page 14 for the total memory sizes for various registered DIMM configurations.

Table 2. Total Memory Sizes With Registered DIMMs

Devices used on DIMM	1 DIMM (2 rows) x64/x72	2 DIMMs (2 rows each) x64/x72	3 DIMMs (2 rows each) x64/x72	4 DIMMs (2 rows each) x64/x72
64 Mbit (4M x 4 x 4 banks)	256 Mbytes	512 Mbytes	768 Mbytes	1 Gbytes
64 Mbit (2M x 8 x 4 banks)	128 Mbytes	256 Mbytes	384 Mbytes	512 Mbytes
64 Mbit (1M x 16 x 4 banks)	64 Mbytes	128 Mbytes	192 Mbytes	256 Mbytes
128 Mbit (8M x 4 x 4 banks)	512 Mbytes	1 Gbytes	1.5 Gbytes	2 Gbytes
128 Mbit (4M x 8 x 4 banks)	256 Mbytes	512 Mbytes	768 Mbytes	1 Gbytes
128 Mbit (2M x 16 x 4 banks)	128 Mbytes	256 Mbytes	384 Mbytes	512 Mbytes
256 Mbit (16M x 4 x 4 banks)	1 Gbytes	2 Gbytes	3 Gbytes	4 Gbytes
256 Mbit (8M x 8 x 4 banks)	512 Mbytes	1 Gbytes	1.5 Gbytes	2 Gbytes
256 Mbit (4M x 16 x 4 banks)	256 Mbytes	512 Mbytes	768 Mbytes	1 Gbytes
512 Mbit (32M x 4 x 4 banks)	2 Gbytes	4 Gbytes	4 Gbytes	4 Gbytes
512 Mbit (16M x 8 x 4 banks)	1 Gbytes	2 Gbytes	3 Gbytes	4 Gbytes
512 Mbit (8M x 16 x 4 banks)	512 Mbytes	1 Gbytes	1.5 Gbytes	2 Gbytes
Note: *The maximum address space supported by the AMD-761 system controller is 4 Gbytes.*				

2.2.1 DRAM Refresh

The AMD-761 system controller keeps track of when each of CS[7:0] needs to be refreshed. Each CS is refreshed independently. Refresh is only performed on rows that are populated. A concurrent refresh cycle can be executed in parallel with other read and write requests, if there is no CS conflict and the command bus is free. Figure 6 on page 15 shows DRAM refresh timing.

Refresh rates are programmable by BIOS and can accommodate various rates at 100-MHz or 133-MHz system bus speeds.

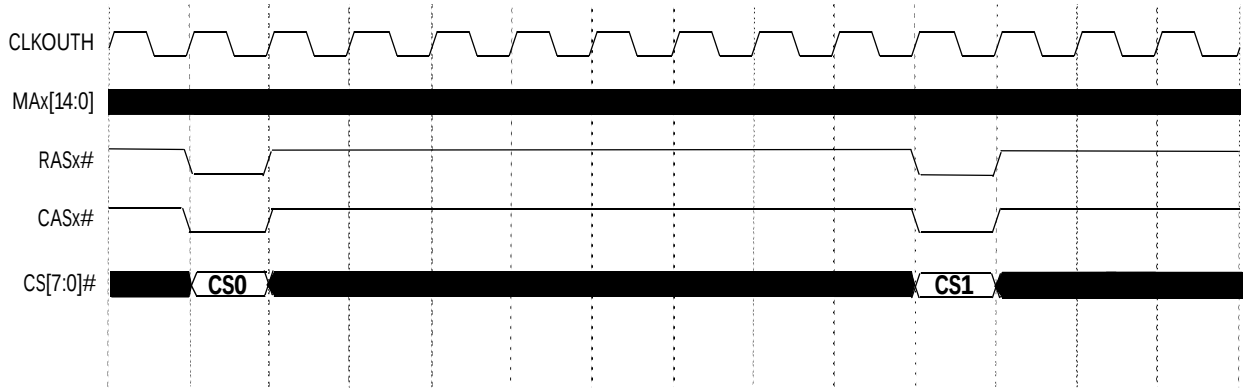


Figure 6. DRAM Refresh Timing

2.2.2 DDR Data Strobes

Unlike single data rate SDRAMs, Double Data Rate (DDR) does not latch data on the rising edge of the memory clock. Instead, DDR devices specify bidirectional data strobes (DQS pins) between the system memory controller and the DDR memories that are used to capture data. The data strobes are source-synchronous, which means that the DQS signals are driven by the device that is currently driving the data bus. The AMD-761 system controller provides one DQS pin per byte when using x8 and x16 DIMMs, or one per nibble when using x4 DIMMs. The data mask (DM) pins provide the additional DQS strobe function when accessing a x4 DIMM. The DM pins no longer provide a mask function when performing a write access to a x4 DIMM. Therefore, a read-modify-write cycle occurs for partial write accesses (partial implying an incomplete quadword of data). In the case of writes to memory, the AMD-761 system controller must drive DQS such that each edge is centered in the write-data valid window to allow the DDR DRAMs to capture the data on each edge of the strobe. For memory reads, the devices drive the DQS pins edge-aligned with the memory clock, and the AMD-761 system controller must center the DQS with the incoming data. Delaying the DQS accordingly for each byte or nibble is required. Because this timing is very tight, the AMD-761 system controller implements programmable delay lines (PDLs) to accomplish this centering of DQS with the data. A separate PDL is implemented for each DQS pin.

Because the propagation delay of an individual buffer internal to the AMD-761 system controller is a function of process, voltage, and temperature (PVT), a mechanism is required to compensate for these three variables. As mentioned previously, the delay value is known, but the number of buffers that provides this delay value is not known for a given PVT point. The calibration mechanism provides this piece of information. The mechanism used is a simple measurement of how many buffer delays are required to equal the system clock period. Because the system clock is generated by a PLL in the AMD-761 system controller that is already compensated for PVT, the system clock period is guaranteed to be independent of PVT. Therefore, the clock period can be assumed to be a constant and can be used to correlate the PDL values to units of time.

The calibration is automatically performed once after reset and once after self-refresh exit (before acknowledging self-refresh exit), and the resultant value is transferred to each PDL. Recalibration can be initiated via software. The AMD-761 system controller also has a mode that enables periodic autocalibration.

2.3 PCI Bus Controller

The AMD-761 system controller drives the 32-bit PCI bus synchronously with the PCI clock (PCICLK) supplied by the system clock generator. The AMD-761 system controller converts the 64-bit processor data to 32-bit PCI data and regenerates commands with minimal overhead. A processor-to-PCI posted write buffer enables the processor and PCI to operate concurrently. The AMD-761 system controller converts consecutive processor addresses to burst PCI cycles. A PCI-to-DRAM posted write buffer and a DRAM-to-PCI prefetch buffer enable concurrent PCI bus and processor-DRAM accesses during PCI-initiator transactions.

When the processor drives an I/O cycle to an address other than the AMD-761 system controller configuration register addresses, the AMD-761 system controller passes the I/O cycle to the PCI bus and responds to the CPU only after the PCI cycle completes. The AMD-761 system controller does not respond to I/O cycles driven by PCI initiators on the PCI bus. The AMD-761 system controller allows these cycles to complete

on the PCI bus. A memory write is the only transaction permitted from PCI to AGP.

The PCI block can be broken up into two sub-blocks—the PCI target module and the PCI master module. The PCI target module handles cycles initiated by an external master on the PCI bus. The AMD-761 system controller responds to cycles that are directed to main memory or writes that are sent to the other PCI interface (the AGP interface). This module contains write buffers (PCI-to-memory and PCI-to-PCI), read buffers from memory, and a target sequencer that keeps track of the bus while the AMD-761 system controller is a PCI target.

The PCI master module handles processor-to-PCI bus cycles. Within a processor stream, no reordering is done.

2.3.1 Memory Coherency

The AMD-761 system controller assures that all data accesses remain coherent:

- All PCI/AGP accesses not in the GART range generate processor probes assuring that reads receive only the latest version of the data and that writes update only the latest version of the data. Writes are always performed in order.
- The GART range is by definition not cacheable. As a result, all PCI/AGP accesses that are in the GART range are subject to non-cacheable ordering rules—that is, they do not generate probes to the processor, writes are performed in order, and reads receive the results of all earlier writes.
- Processor accesses to addresses mapped by the GART range can either use the GART for the final address translation or map the addresses through its page tables as a non-cacheable memory type.

2.3.2 PCI Arbitration

The AMD-761 system controller contains arbitration logic that allocates ownership of the PCI bus among itself, the AMD-766™ peripheral bus controller, and seven other PCI initiators.

Access priority rotates between the Southbridge and CPU/PCI bus masters (GNT[6:0]#) such that the following arbitration sequence could be seen in a busy system:

1. Southbridge
2. CPU
3. Southbridge
4. PCI master (one of GNT[6:0]#)
5. Repeat step 1

When there are no requests for the bus, ownership defaults to the processor through the AMD-761 system controller. This mode is controlled by the PCI Arbitration Control register (Dev 0:F0, 0x84, bit 0).

2.3.3 PCI Configuration

The AMD-761 system controller uses PCI configuration mechanism #1 to select all of the options available for interaction with the processor, DRAM, and the PCI bus. This mechanism is defined in the *PCI Local Bus Specification*, Revision 2.2. All configuration functions for the AMD-761 system controller are performed by using two I/O-mapped configuration registers—IO_CNTRL (I/O address 0CF8h) and IO_DATA (I/O address 0CFCh).

These two registers are used to access all the other internal configuration registers of the AMD-761 system controller. The AMD-761 system controller decodes accesses to these two I/O addresses and handles them internally. A read to a nonexistent configuration register returns a value of FFh. Accesses to all other I/O addresses are forwarded to the PCI bus as regular I/O cycles. Read and write cycles involving the AMD-761 system controller configuration registers are only distinguished by the address and command that is sent.

The AMD-761 system controller implements the following configuration spaces:

- Device 0:Function 0 (host bridge configuration registers)
- Device 0:Function 1 (DDR I/O and PDL configuration)
- Device 1:Function 0 (PCI-PCI bridge, AGP configuration)

The Device 0:Function 1 space is disabled by default, and must be enabled by writing to a specific bit in the PCI Control register (Dev 0:F0:0x4C). The normal reserved PCI header space (0x00-0x3F) in this function returns all 1s.

2.3.4 PCI Southbridge Signals

The AMD-761 system controller supports one pair of PCI request/grant signals, SBREQ# and SBGNT#, to connect to a Southbridge device such as an ISA/EISA bridge. These signals are generally used when a PCI device, an ISA master, or a DMA device requires ownership of the system main memory. The ISA bus device asserts SBREQ# to request the bus. The AMD-761 system controller grants the request after all of its write buffers have been flushed by asserting SBGNT#.

Note: *The AMD-761 system controller allows a Southbridge device to hold SBREQ# for an extended time in order to complete an ISA transfer and avoid a potential deadlock condition.*

2.3.5 PCI Parity/ECC Errors

The AMD-761 system controller indicates that an ECC error occurred on the memory bus by setting a bit in the status register and optionally asserting the PCI SERR# signal. This action results in the error being reported by the Southbridge.

The AMD-761 system controller does not check parity on the PCI bus. The status bit (Dev 0:04h, bit 31) is always 0.

2.3.6 PCI Accesses by an Initiator

A PCI initiator begins a memory read or write cycle by asserting FRAME# and placing the memory address on AD[31:00]. The AMD-761 system controller decodes the address. If the address is within the memory region as defined by PCI Top of Memory (Dev 0:F0:0x9C), the AMD-761 system controller accepts the cycle and responds as a PCI target by

asserting DEVSEL#. If the address is not within the defined memory region, the AMD-761™ system controller ignores the cycle and allows it to complete on the PCI.

Read requests from PCI masters to the memory subsystem are full cache lines only. After fetching the initial cache line, the AMD-761 system controller can optionally start prefetching the next cache line. Prefetching the next cache line is preferred, because the PCI master typically reads more than one line, but can waste DRAM bandwidth if this line is thrown away.

The length of a read request is always 8 quadwords (one cache line). During writes, the AMD-761 system controller attempts to accumulate an entire cache line. If the start address is not cache aligned, the AMD-761 system controller makes single write requests until it reaches a cache-aligned address. When aligned, it makes a request every 8 quadwords. If a partial cache line write is detected, no more data is accumulated, and a request is issued to the memory subsystem.

2.3.7 WSC# Pin Assertion

The Write Snoop Complete (WSC#) pin is used to indicate to the Southbridge that all probe activity for the last PCI to DRAM write has been completed and that an interrupt message can now be sent by the APIC. The AMD-761 system controller supports both bidirectional and unidirectional modes of operation for the WSC# pin as described below.

Note: *The unidirectional WSC# mode is available only in silicon revisions B4 and above. All other revisions support only the bidirectional WSC# mode.*

Bidirectional WSC#

The default mode for WSC# operation is bidirectional for the AMD-761 system controller. This is selected by writing a 0 to the WSC_DIR bit in the PCI Control register (Dev 0:F0:0x4C, bit 3). In this mode, the Southbridge first drives the WSC# pin low for a single PCICLK period when an APIC interrupt message must be sent to the processor. This action alerts the AMD-761 system controller that posted PCI-to-DRAM writes must be flushed to coherent memory. The AMD-761 system controller then asserts the WSC# pin for two PCICLK periods after the probe activity for the last PCI-to-DRAM write has

completed. This action instructs the Southbridge that it can now send an APIC message over the interrupt messaging bus.

The bidirectional WSC# mode is supported by the AMD-766™ peripheral bus controller.

Unidirectional WSC#

The unidirectional WSC# mode is selected by setting the WSC_DIR bit in the PCI Control register (Dev 0:F0:0x4C, bit 3). In this mode, the WSC# pin is always an output of the AMD-761 system controller and is driven Low when there are no pending probes due to PCI-to-DRAM writes. The WSC# pin is High when there are any outstanding probes due to PCI-to-DRAM writes.

Note: *The unidirectional WSC# mode is available only in silicon revisions B4 and above. All other revisions support only the bidirectional WSC# mode.*

2.4 Accelerated Graphics Port (AGP)

The Accelerated Graphics Port (AGP) is a point-to-point connection between a graphics adapter (AGP initiator) and the AMD-761 memory controller (AGP target), which enables the adapter to store and use graphics data in main memory. This connection relieves graphics traffic from the PCI bus and greatly accelerates video performance.

The AMD-761 system controller functions as an AGP target, providing all the signals, buffers, and logic required for compliance with the *Accelerated Graphics Port Interface Specification*, Revision 2.0.

While AGP relieves traffic on the PCI bus and frees up graphics adapter memory, the greatest impact on system performance comes from the many innovations AGP brings to data transfer operations. These improvements include the following:

- *Split Transactions*—Requests to read or write data are separate from the data transfers.
- *Pipelined Requests*—Requests can be issued contiguously and stored in the AMD-761 system controller request queue. Pipelining allows AGP to achieve high levels of concurrency with PCI and the processor.

- *Pipeline Grants*—Pipelined GNT# signals for up to four write transactions.
- *Prioritizing* (reordering)—Read and write requests can be assigned a high priority or a low priority to ensure that more urgent requests are serviced first.
- *Defined-Length Requests*—The amount of data requested is indicated in the AGP command, rather than the duration of an asserted signal, such as FRAME# in PCI.
- An 8-byte minimum data size for AGP 2x/4x transfers, which provides an efficient method for moving the large amount of data typical in a graphics request.
- A separate, optional Sideband Address (SBA) bus that enables concurrent transmissions of requests and data transfers.
- Optional 2x/4x modes that increase the AGP graphics adapter data transfer rate.
- Freedom from the coherency requirements of PCI, which eliminates the latency resulting from cache snooping.
- PCI 2.2 capability, which enables the AMD-761 system controller to pass programming information from the processor to the graphics adapter.
- A Graphics Address Remapping Table (GART).

The AGP request queue is split up into two queues—one for read requests and one for write requests. Because there is a reordering FIFO in the address module, the request queues do not have to be large. The read queue is big enough to hold all outstanding read requests, which avoids stalling writes that run on the bus while the reads occur to memory.

Requests from the SBA bus are multiplexed with PIPE# requests and written to the same queues. High-priority requests are inserted in front of low-priority requests so that the request to be serviced is at the top of the queue. This reordering is done dynamically as a new request is written into the queue.

Requests from each of the queues can be read out of both the queues at the same time. The reads start fetching data from memory and the write data is sent across the AGP bus at the same time.

The AGP ordering rules specify that writes are ordered ahead of reads. Reads are serviced only when all the preceding writes have been written to memory, which is only required for low-priority requests and does not affect high-priority read requests. When a low-priority request is the next one to be serviced from the read queue, the tag of that request is compared with all valid entries in the write queue. If any entry matches, then the read request is blocked. Only after the write requests are serviced will the read requests be allowed to proceed.

AGP Request Queue. In general, the AGP request queue services AGP requests in the order received, subject to their priority (write High, read High, write, read).

Ordering Rules. The request queue is subject to the following AGP ordering rules:

- High-priority write requests are processed in the order they are received.
- High-priority read requests are processed in the order they are received.
- Low-priority write requests are processed in the order they are received.
- Low-priority read requests are processed in the order they are received.
- Low-priority reads push low-priority writes, meaning that a write request is serviced before a subsequently received read request is serviced.
- Low-priority writes can pass low-priority reads, meaning that a write request can be serviced before a previously received read request.
- There are no ordering restrictions between AGP and PCI transactions on the AGP bus.
- PCI transactions on the AGP bus follow the PCI ordering rules described in the *PCI Local Bus Specification*, Revision 2.2.
- High-priority requests are re-ordered in front of low-priority requests.
- There is no ordering relationship between high-priority reads, high-priority writes, and any other transfer type, such as low-priority reads, low-priority writes, PCI reads, or PCI writes.

If a low-priority data transfer is in progress when a high-priority request is received, the data transfer completes before the high-priority request is serviced—that is, a request cannot be preempted. A high-priority request supersedes a low-priority request on a request boundary only.

2.5 System Clocking

The AMD-761 system controller requires the following system clocks:

- SYSCLK, used for clocking the AMD Athlon system bus and the DDR DRAM interface. This clock is typically either 100 MHz or 133 MHz. This clock is also used to create the DDR DRAM clock outputs (CLKOUT[5:0], CLKOUT[5:0]#).
- AGPCLK, 66 MHz, used for clocking the AGP and PCI internal logic.
- PCICLK, provides the 33-MHz PCI bus clock and is used to synchronize the PCI bus I/O signals to the 33-MHz PCI signal domain.

The AMD-761 system controller implements two internal PLLs to control clock skew on-chip for the SYSCLK and AGPCLK domains. These PLLs can be bypassed for motherboard testing. Refer to Chapter 3 for further details of PLL bypass testing.

2.6 Power Management

The AMD-761 system controller supports the advanced configuration power interface (ACPI) specification, On-Now, and PC 99 requirements through a handshake mechanism with the processor. The ACPI-defined registers required for processor and system power management are contained in the AMD-766 peripheral bus controller companion device. SMM memory remapping is handled by a model-specific register in the AMD Athlon processor. See the *AMD Athlon™ BIOS Developers Guide*, order# 21656, for more information about the SMM remapping operation. Figure 7 on page 25 shows how the processor and system controller communicate power-state transitions.

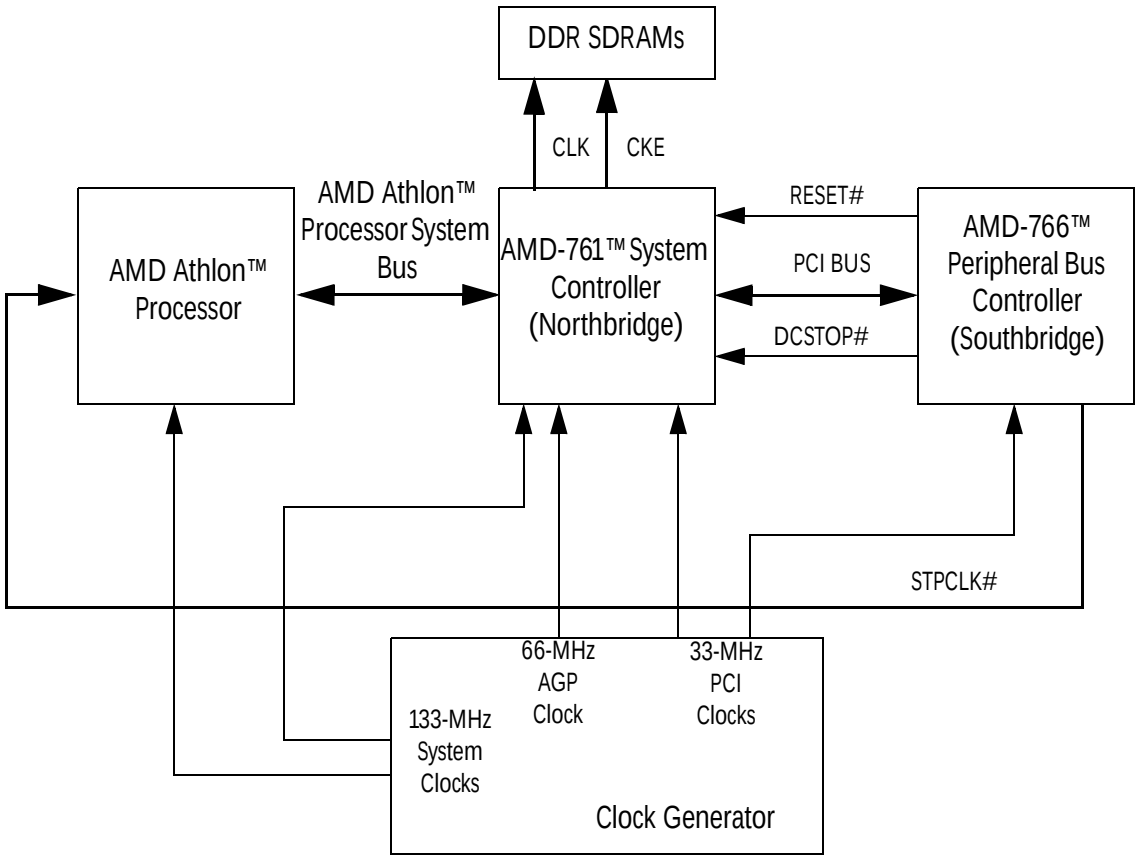


Figure 7. Power Management Signal Connections

The processor and the AMD-761 system controller communicate power-state transitions through the AMD Athlon system bus connect/disconnect protocol and special cycles (masked writes to a defined AMD Athlon system bus address with specific data encoding). In general, the processor initiates a request for a disconnect with a special cycle, and the AMD-761 system controller may or may not actually disconnect the processor with the connect/disconnect protocol. The AMD-761 system controller performs the requested connect/disconnect as part of the process of entering and exiting certain ACPI states. The following two special cycles are of interest:

- Halt—Generated by the AMD Athlon processor in response to executing a HALT instruction. The AMD-761 system controller sends a Halt special cycle on the PCI bus and optionally (through a configuration register bit) initiates an AMD Athlon system bus disconnect to the processor.

- Stop Grant—Generated by the AMD Athlon processor in response to assertion of STPCLK#. When the AMD-761 system controller receives a Stop Grant from the processor, it sends a Stop Grant special cycle on the PCI bus. The AMD-761 system controller initiates the following sequence of actions if the Stop Grant disconnect bit is set (Dev 0:F0:0x60):
  A. Disables PCI/AGP arbitration and waits for all queues to memory to be empty (including refresh requests).
  B. Completes the AMD Athlon system bus cycle. The AMD-761 system controller then initiates an AMD Athlon system bus disconnect to the processor, and causes the memory to enter self-refresh.
  C. The AMD-766 peripheral bus controller decodes the special cycle and enters the appropriate power state. The AMD-766 peripheral bus controller can then assert DCSTOP#.

Halt special cycles are generally considered part of an ACPI state definition (C1). STPCLK#, however, can be asserted at random times while the processor is in the full-running state (C0), to conserve power (clock throttling).

The AMD-761 system controller implements the following power states:

1. ACPI C0 full-on
2. ACPI C1 Halt
3. ACPI C2 Stop Grant (probed)
4. ACPI S1 power-on suspend
5. ACPI S3 suspend to RAM

These power states are described in further detail in subsequent paragraphs.

2.6.1 Full-On (C0)

In this state, the AMD-761 system controller is fully operational, all clock trees are running, all voltage planes are enabled, and the AMD-761 system controller provides normal refresh to DRAM.

2.6.2 Halt (C1)

If the AMD-761 system controller detects a Halt special cycle from the processor, the Halt state (C1) is entered and the Halt special cycle is driven on the PCI bus. If the Halt disconnect configuration bit is set (Dev 0:F0:0x60), the AMD-761 system controller disconnects the processor. PCI and AGP masters continue to run normally. If the AMD-761 system controller detects a PCI DMA master transaction that requires a probe of the processor's cache, the processor is connected, and the probe cycle(s) run on the AMD Athlon system bus. If the processor does not start any non-NOP AMD Athlon system bus cycles while the probe is in progress, the AMD-761 system controller disconnects the AMD Athlon system bus following the completion of the probe. If the processor starts sending non-NOP AMD Athlon system bus cycles while connected, the AMD-761 system controller transitions to the full-on state.

2.6.3 Stop Grant (C2)

If the AMD-761 system controller has detected a Stop Grant special cycle from the processor, the Stop Grant special cycle is driven on the PCI bus. If the Stop Grant disconnect bit is set (Dev 0:F0:0x60) when the Stop Grant special cycle is received, and there is no probe traffic, the AMD-761 system controller disconnects the processor and places system memory in self-refresh mode before passing the Stop Grant special cycle to the PCI bus. If the AMD-761 system controller detects a PCI DMA master transaction that needs a snoop, the processor is connected, DRAM is taken out of self-refresh mode, and the probe cycle(s) is initiated on the AMD Athlon system bus. If the processor does not start any non-NOP AMD Athlon system bus cycles while the probe is in progress, the AMD-761 system controller disconnects the AMD Athlon system bus following the completion of the probe. If the processor starts sending non-NOP AMD Athlon system bus cycles while connected, the AMD-761 system controller transitions to the full-on state.

2.6.4 Power-On Suspend (S1)

The S1 state achieves very low power by disconnecting the processor, entering self-refresh, and then gating off most of the internal high-speed clock trees in the AMD-761 system controller. Snooping is prevented by the peripheral device

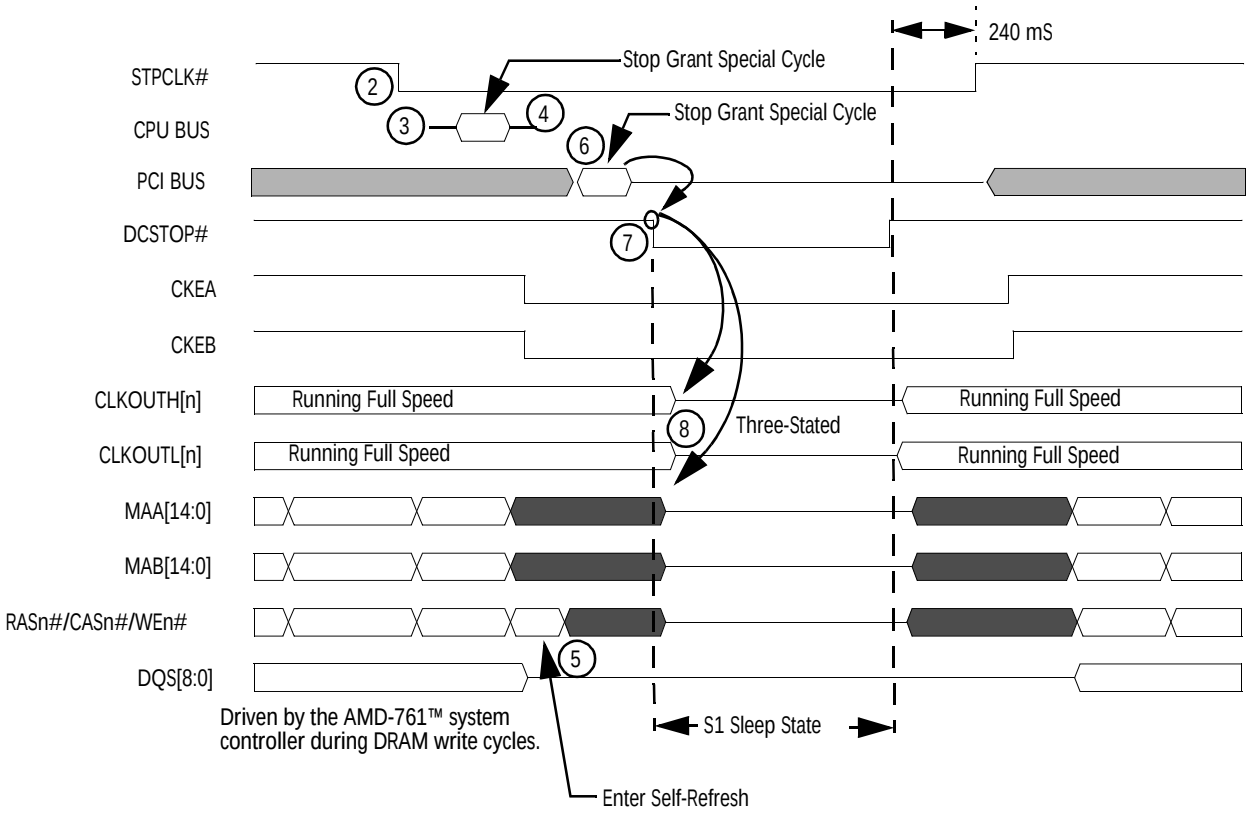
drivers prior to entering this state. The DDR DRAM clocks continue to be driven for registered DIMMs but are disabled (three-stated) for unbuffered DIMMs. Most internal clocks are gated off, allowing the AMD-761 system controller to achieve a low operating current.

The S1 state is entered in a similar manner to C2, starting with a STPCLK# assertion and the Stop Grant state. The AMD-766 peripheral bus controller Southbridge then asserts the DCSTOP# signal, which is used by the AMD-761 system controller to gate off internal clock trees for lower power. All power supplies remain on, and the clock synthesizer chip on the motherboard continues to drive all clocks. The sequence of operation for entering the S1 state is listed below. Figure 8 on page 29 shows a power-on suspend system timing diagram example.

S1 Sequence

1. The operating system communicates with all device drivers, causing them to disable their respective peripherals, thus preventing any new bus master activity (DMA) on the PCI and AGP buses. DMA activity already in progress in the AMD-761 system controller completes normally.
2. The Southbridge asserts STPCLK# to the AMD Athlon processor.
3. The processor flushes its buffers and generates a Stop Grant special bus cycle on the AMD Athlon system bus.
4. The AMD-761 system controller flushes all internal queues and initiates a disconnect cycle to the CPU by deasserting the CONNECT pin. The AMD Athlon responds by deasserting the PROCRDY signal.
5. After all queues are flushed, the AMD-761 system controller's power management logic requests the DRAM controller to place the DRAM in self-refresh mode. The DRAM controller initiates self-refresh, then acknowledges to the power management logic.
   - Self-refresh mode is initiated by generating an auto-refresh cycle and deasserting the CKE pins.
6. The AMD-761 system controller issues a Stop Grant special cycle on the PCI bus.
7. The Southbridge detects the Stop Grant special cycle on the PCI bus and asserts the DCSTOP# signal.

8. The AMD-761 system controller samples DCSTOP# active and gates off most of the internal clock trees. The DDR DRAM clocks and address/command outputs are three-stated. The CKE pins remain driven Low. The external clock sources and the AMD-761 system controller PLLs continue to run.
   - Note that the DDR DRAM clocks (CLKOUT[5:0], CLKOUT[5:0]#) continue to run when registered DIMMs are installed. This action is required because the reset signal to the registered DIMMs is connected to the AMD-761 system controller's RESET# pin. The RESET# pin is **not asserted in the S1 state, thus the clocks cannot be removed from the registered DIMMs**.



Note: *Circled numbers correspond to "S1 Sequence" on page 28.*

Figure 8. Power On Suspend System Timing Diagram Example

This state is exited when the DCSTOP# signal is deasserted by the AMD-766 peripheral bus controller Southbridge, followed by a deassertion of STPCLK#. This action causes the AMD-761 system controller to enable the clock trees and prepare to reconnect the processor. The processor asserts PROCRDY, which causes the AMD-761 system controller to exit self-refresh and reconnect the AMD Athlon system bus. The AMD-761 system controller retains the state of all configuration registers during the S1 state.

2.6.5 Suspend to RAM (S3)

The S3 state is similar to S1. However, power is removed from most of the motherboard except the AMD-761 system controller, DRAM, and a portion of the AMD-766 peripheral bus controller Southbridge. S3 is the lowest power sleep state, and allows very fast resume because system context is stored in memory instead of on disk.

The S3 state is entered similarly to S1 with a Stop Grant special cycle and DCSTOP#. After entering S3 state with DCSTOP# assertion, the AMD-766 peripheral bus controller asserts the RESET# signal, which causes the AMD-761 system controller to gate off its I/O rings to accommodate the voltages being removed from the AMD Athlon system bus, PCI bus, and AGP bus. The AMD-761 system controller core remains powered (2.5 Vdc) as does the DDR I/O interface and the DDR DIMMs, to allow the memory to remain in self-refresh mode with the CKE pins driven Low. The sequence of operation for entering the S3 state is listed below. Figure 9 on page 32 shows a suspend to RAM system timing diagram example.

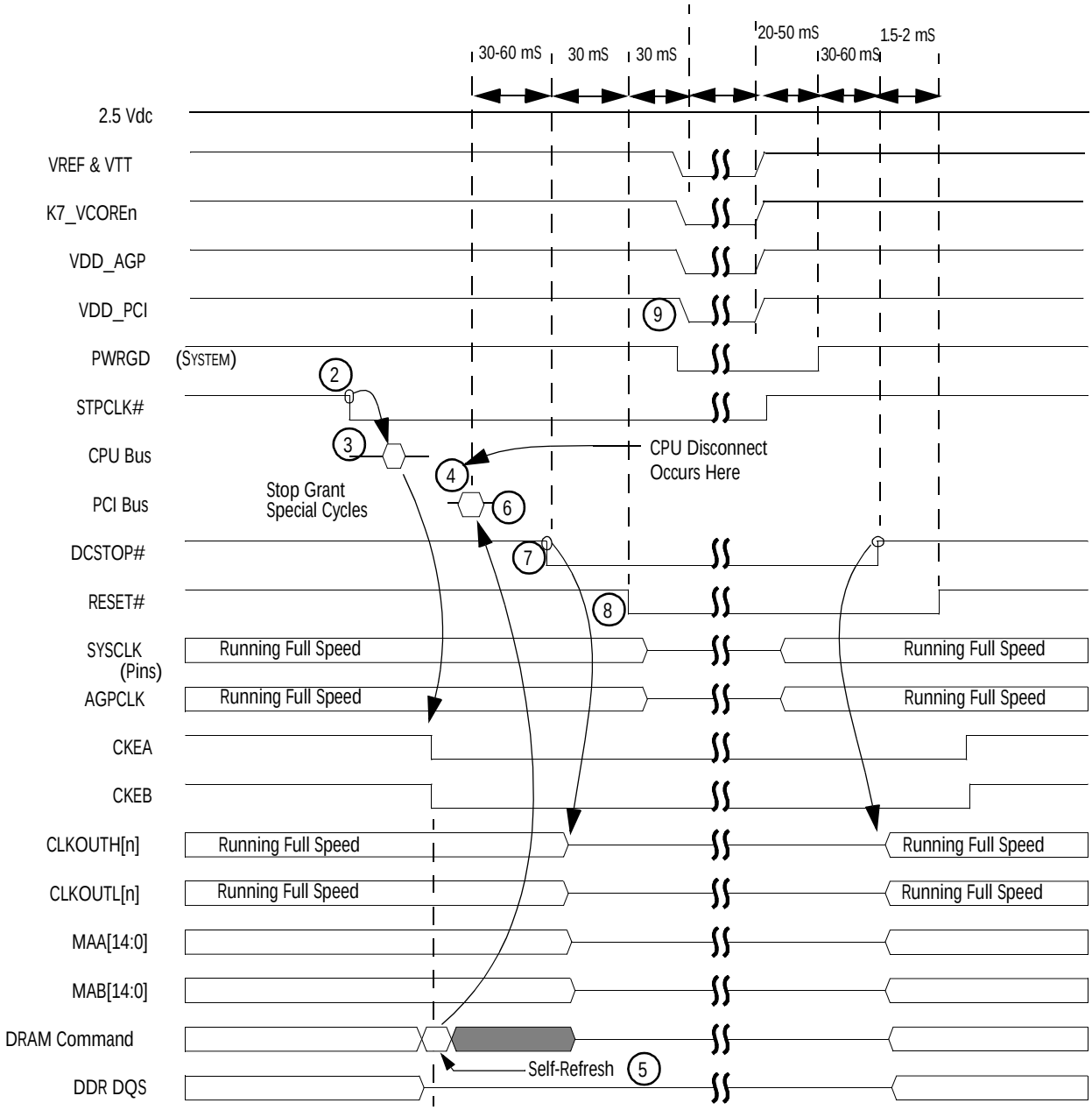
S3 Sequence

1. As with the S1 state, the device drivers are called to place all devices into the D3 device state, which prevents them from trying to master on the bus they reside (or access system memory).
2. The ACPI driver (or BIOS under APM) writes to the appropriate registers in the AMD-766 peripheral bus controller to initiate the hardware sequence into the S3 state. In response to this write, the AMD-766 peripheral bus controller asserts STPCLK# to the AMD Athlon processor. Once STPCLK# has been asserted, the power management

state machine in the AMD-766 peripheral bus controller waits for a Stop Grant special cycle on the PCI bus before completing the transition into the S3 state.

3. The CPU recognizes that STPCLK# has been asserted, flushes internal buffers, and generates a Stop Grant cycle on the AMD Athlon system bus.
4. The AMD-761 system controller flushes all internal queues including outstanding probes, then deasserts the CONNECT pin. The CPU responds by deasserting its PROCRDY pin.
5. When the disconnect is complete, the AMD-761 system controller executes a self-refresh command to the DDR SDRAM and waits for it to complete (this action is accomplished by issuing an auto-refresh command and driving the CKE signals Low to the DRAM).
6. The AMD-761 system controller issues a Stop Grant special cycle on the PCI bus.
7. The Southbridge asserts DCSTOP#. The AMD-761 system controller follows the normal DCSTOP# protocol as described in "S1 Sequence" on page 28, including gating most of the internal clocks off. The DDR clock pins are also three-stated at this time.
   - Note that if registered DIMMs are installed, the DDR output clocks (CLKOUT[5:0], CLKOUT[5:0]#) continue running for an additional six clock periods from the assertion of RESET#. This action is required because the DIMM reset signal on registered DIMMs is connected to the AMD-761 system controller RESET# pin, and the DIMM clocks must be running while the DIMM **reset is first asserted**.
8. The AMD-766 peripheral bus controller asserts PCIRST# (RESET# on the AMD-761 system controller). The AMD-761 system controller continues driving the CKE pins Low, and gates off the I/O pads to prevent driving 1s to the unpowered I/O ring and to inhibit floating inputs from the unpowered I/O rings to the powered core logic. The input clock pins (SYSCLK and AGPCLK) are also gated off because these input pins are floating when the motherboard's 3.3 Vdc is powered off. The two STR bits in the DRAM Mode/Status register (Dev 0:F0:0x58) are cleared to 0s. The state of all other memory controller configuration register bits is preserved.

9. The AMD-766 peripheral bus controller signals the power supply (deasserts PWRON#) to shut down all but the 5-Vdc and 2.5-Vdc voltages. The motherboard clock generator chip shuts down, therefore the input clocks (SYSCLK and AGPCLK) float.



Note: *Circled numbers correspond to "S3 Sequence" on page 30.*

Figure 9. Suspend to RAM System Timing Diagram Example

The S3 state is exited when the AMD-766 peripheral bus controller detects an enabled resume event. The AMD-766 powers up all of the voltage planes that are off during the S3 state by asserting PWRON#. After all of the voltage planes in the system are within specification, and all of the outputs of the system clock generator are running within specification, PWRGD is asserted to the AMD-766 peripheral bus controller. The AMD-766 then deasserts DCSTOP# followed by deassertion of PCIRST# (the RESET# pin on the AMD-761 system controller).

This state is exited when the DCSTOP# signal is driven High (power supplies back on) followed by deassertion of RESET#. The AMD-761 system controller retains the state of the memory controller configuration registers, which allows BIOS to access memory to retrieve and restore the system context. There are two configuration bits that BIOS uses to allow the AMD-761 system controller to differentiate between S3 and all other states following an active to inactive transition on the RESET# pin. Upon exiting the S3 sleep state, BIOS writes the appropriate value to these bits, which causes the AMD-761 system controller to exit self-refresh. The two register bits (STR_Control) are in the DRAM Mode/Status register (Dev 0:F0:0x58). Refer to the *AMD-761™ System Controller Software/BIOS Design Guide*, order# 24081, for detailed information on these bits.

3 Test

The AMD-761™ system controller supports test modes that may be used in some cases for motherboard manufacturing test and debug. The following test modes are available on the AMD-761 system controller:

- Three-state test
- NAND tree test
- PLL bypass test
- Clock output test

Three-state test and NAND tree test can be used to prevent the AMD-761 system controller from driving its pins and to verify connectivity of the AMD-761 system controller to the motherboard. The PLL bypass and clock output test modes are provided primarily for motherboard debug and can be used to verify system clocking and drive slower clocks into the system.

Test modes are invoked in the AMD-761 system controller by the assertion of the TEST# pin in conjunction with enabling specific pinstraps on the PCI bus AD[31:0] pins, as described in each section. These pins can be used as pinstraps for various functions by connecting either a pullup or pulldown resistor as required to enable or disable the function (a 10-kohm resistor should be used). The pinstraps are sampled at reset and latched, and the value of most pinstraps can be read in the Configuration Status register (Dev 0:F0:0x88).

Asserting the RESET# pin and de-asserting the TEST# pin causes the AMD-761 system controller to exit test modes.

3.1 Board (Three-State) Test Mode

Board test mode simply forces all AMD-761 system controller outputs to a high impedance to allow board-level test equipment to drive the nodes normally driven by AMD-761 system controller pins to test board connectivity. The outputs are three-stated after a maximum of six clocks are driven on the SYSCLK and AGPCLK pins. The minimum number of clocks is required due to some I/O cells that cannot be asynchronously forced into a three-state mode.

Board test mode is entered when the AD[25] pin is asserted High simultaneous with the TEST# pin during RESET# assertion. The test mode is then latched coming out of reset. The AD[09] pin should also be pulled up to force the internal PLLs to be bypassed.

Three-state mode can be exited by an assertion of the RESET# pin. This reset also disables the PLL bypass mode if it was entered.

3.1.1 Board Test Mode Clocking

When entering three-state test mode, the PLLs should also be bypassed as described above. This procedure forces the clocks driven on the SYSCLK and AGPCLK input pins to be routed directly to the appropriate clock domains. The SYSCLK and AGPCLK pins must then be clocked for six clocks as required to force some AMD-761 system controller I/O pads to the three-state mode.

3.2 NAND Tree Test Mode

NAND tree testing is used on the tester and can also be used during board testing to test connectivity of AMD-761 system controller inputs. In this test mode, each AMD-761 system controller input can be asserted one pin at a time, and for each pin assertion there should be a change in state on the output of the respective NAND tree. The AMD-761 system controller provides multiple NAND trees, which speeds up characterization of the device, and also reduces motherboard test time. The AMD-761 system controller NAND trees are divided by I/O type, thus there are the following trees:

- AMD Athlon system bus NAND tree

  This tree includes all signals on the AMD Athlon™ system bus. SYSCLK is not included in the NAND tree. The output of this tree is the GNT[0]# pin. The ordering for this NAND tree is shown in Table 3 on page 38.

- AGP/APC NAND tree

  This tree includes AGPCLK, AGP, and the PCI-type signals that are included in the AGP interface. The output of this tree is the GNT[1]# pin. The ordering for this NAND tree is shown in Table 4 on page 39.

- DDR DRAM NAND tree

  This tree includes all signals in the DDR interface. The output of this tree is the GNT[3]# pin. The ordering for this NAND tree is shown in Table 5 on page 40.

- PCI NAND tree

  This tree includes PCICLK and PCI bus signals, except the RESET# input. The output of this tree is the GNT[2]# pin. The ordering for this NAND tree is shown in Table 6 on page 42.

Table 3. AMD Athlon™ System Bus NAND Tree Ordering

Order	Input Pin Name	Ball	Order	Input Pin Name	Ball	Order	Input Pin Name	Ball
1	SADDOUT[09]#	N-3	39	SDATA[58]#	Y-2	77	SDATA[31]#	AE-4
2	SADDOUT[07]#	M-3	40	SDATA[57]#	Y-3	78	SDATA[19]#	AG-4
3	SADDOUT[14]#	L-1	41	SDATA[48]#	W-5	79	SDATAINCLK[1]#	AE-6
4	SADDOUT[12]#	N-2	42	SCHECK[7]#	W-3	80	SCHECK[2]#	AH-4
5	SADDOUT[06]#	P-3	43	SDATA[39]#	AA-1	81	SDATA[20]#	AJ-3
6	SADDOUT[13]#	M-1	44	SDATA[45]#	AC-1	82	SDATA[28]#	AE-7
7	SADDOUT[05]#	P-2	45	SDATA[36]#	Y-4	83	SDATA[29]#	AF-6
8	SADDOUTCLK#	N-1	46	SDATA[37]#	AA-3	84	SDATA[18]#	AH-5
9	SADDOUT[10]#	R-3	47	SDATA[47]#	AB-2	85	SDATA[24]#	AE-9
10	SADDOUT[08]#	P-1	48	SDATA[44]#	AC-2	86	SDATA[27]#	AE-8
11	SADDOUT[11]#	R-5	49	SDATA[46]#	Y-5	87	SDATA[17]#	AG-6
12	SADDOUT[02]#	R-1	50	SDATA[43]#	AE-1	88	SDATA[25]#	AF-8
13	SADDOUT[04]#	T-4	51	SDATA[38]#	AB-3	89	SDATA[16]#	AH-6
14	SADDOUT[03]#	T-1	52	SCHECK[4]#	AB-4	90	SDATA[26]#	AG-7
15	SDATA[55]#	T-5	53	SCHECK[5]#	AD-1	91	SDATA[01]#	AE-10
16	SCHECK[6]#	T-3	54	SDATAINCLK[2]#	AC-3	92	SDATA[07]#	AJ-5
17	SDATAOUTCLK[3]#	T-2	55	SDATA[35]#	AA-5	93	SDATA[15]#	AF-9
18	SDATA[63]#	U-3	56	SDATA[33]#	AC-4	94	SCHECK[0]#	AG-8
19	SDATA[54]#	U-4	57	SDATA[40]#	AF-1	95	SDATA[05]#	AJ-7
20	SDATA[53]#	U-1	58	SDATA[42]#	AE-2	96	SDATA[06]#	AJ-6
21	SDATA[49]#	U-2	59	SDATAOUTCLK[2]#	AD-3	97	SDATAINCLK[0]#	AG-9
22	SDATA[52]#	U-5	60	SDATA[34]#	AB-5	98	SDATA[4]#	AH-8
23	SDATA[62]#	W-1	61	SDATA[41]#	AE-3	99	SDATA[10]#	AE-12
24	SDATAINCLK[3]#	V-1	62	SDATA[32]#	AC-5	100	SCHECK[1]#	AE-11
25	SDATA[59]#	Y-1	63	SDATA[22]#	AG-3	101	SDATA[03]#	AH-9
26	SDATA[61]#	V-3	64	SDATA[30]#	AD-5	102	SDATA[12]#	AG-10
27	SDATA[50]#	V-5	65	SDATAOUTCLK[1]#	AF-2	103	SDATA[08]#	AF-11
28	SDATA[60]#	W-2	66	SDATA[23]#	AG-2	104	SDATA[02]#	AJ-8
29	SDATA[51]#	W-4	67	SCHECK[3]#	AF-5	105	SDATAOUTCLK[0]#	AF-12
30	SDATA[56]#	AB-1	68	SDATA[21]#	AH-3	106	SDATA[14]#	AG-11
31	SDATA[13]#	AJ-10	69	SADDIN[07]#	AE-13	107	CLKFWDRST	AF-15
32	SDATA[00]#	AJ-9	70	SADDIN[03]#	AJ-13	108	SADDIN[14]#	AJ-15
33	SDATA[11]#	AH-11	71	SDATAINVALID#	AF-14	109	SADDINCLK#	AH-15
34	SDATA[09]#	AJ-11	72	SADDIN[09]#	AJ-14	110	CONNECT	AE-15
35	SADDIN[11]#	AH-12	73	SADDIN[08]#	AE-14	111	PROCRDY	AJ-17
36	SADDIN[05]#	AG-12	74	SADDIN[04]#	AG-14	112	SADDIN[12]#	AJ-16
37	SADDIN[06]#	AG-13	75	SADDIN[10]#	AH-14			
38	SADDIN[02]#	AJ-12	76	SADDIN[13]#	AG-15			

Table 4: AMD-761™ System Controller AGP NAND Tree Ordering

Order	Input Pin Name	Ball	Order	Input Pin Name	Ball	Order	Input Pin Name	Ball
1	A_GNT#	AD-27	23	SBSTB#	AA-29	45	A_AD[14]	N-29
2	SBA[1]	AB-25	24	A_AD[24]	W-27	46	A_AD[10]	M-29
3	PIPE#	AE-29	25	A_AD[31]	Y-29	47	A_AD[12]	M-28
4	WBF#	AC-26	26	A_AD[18]	U-26	48	A_AD[15]	N-27
5	SBA[5]	AA-25	27	A_AD[27]	V-27	49	A_AD[07]	L-29
6	ST[1]	AD-28	28	A_AD[29]	W-29	50	A_TRDY#	P-25
7	A_REQ#	AD-29	29	SBA[6]	Y-28	51	A_AD[11]	M-26
8	ST[0]	AC-27	30	A_AD[25]	V-28	52	A_AD[08]	L-28
9	ST[2]	AC-28	31	ADSTB[1]	U-27	53	A_PAR	N-25
10	SBA[7]	AA-26	32	ADSTB[1]#	V-29	54	ADSTB[0]	M-27
11	A_AD[30]	Y-25	33	A_AD[16]	T-27	55	ADSTB[0]#	L-27
12	SBA[3]	AB-27	34	A_AD[23]	U-28	56	A_AD[05]	K-29
13	RBF#	AC-29	35	A_AD[21]	U-29	57	A_AD[03]	J-29
14	A_AD[28]	Y-26	36	A_AD[19]	T-29	58	A_AD[09]	L-25
15	CBE[3]#	V-25	37	A_IRDY#	R-29	59	A_AD[06]	K-27
16	SBA[2]	AA-27	38	A_FRAME#	R-26	60	A_CBE[0]#	L-26
17	SBA[0]	AB-29	39	A_CBE[2]#	R-28	61	A_AD[01]	J-28
18	A_AD[26]	W-25	40	A_AD[17]	R-27	62	A_AD[13]	M-25
19	A_AD[20]	U-25	41	A_CBE[1]#	P-29	63	A_AD[04]	K-25
20	A_AD[22]	V-26	42	A_DEVSEL#	P-27	64	A_AD[02]	J-26
21	SBA[4]	Y-27	43	A_SERR#	P-28	65	A_AD[00]	J-25
22	SBSTB	AA-28	44	A_STOP#	P-26	66	PCICLK	F-28

Table 5: AMD-761™ System Controller DDR NAND Tree Ordering

Order	Input Pin Name	Ball	Order	Input Pin Name	Ball	Order	Input Pin Name	Ball
1	MDAT[59]	E-29	35	MDAT[49]	A-24	69	DQS[4]	A-16
2	MDAT[63]	E-27	36	CS[0]#	D-22	70	MDAT[36]	A-15
3	DQS[7]	D-29	37	WEA#	E-20	71	MAB[00]	E-15
4	CLKOUT[5]	F-26	38	MDAT[48]	C-22	72	MDAT[37]	B-15
5	DCSTOP#	G-25	39	MDAT[52]	A-23	73	MDAT[33]	C-15
6	MDAT[58]	E-28	40	CS[2]#	D-21	74	MDAT[32]	A-14
7	MDAT[62]	C-29	41	WEB#	C-20	75	MECC[7]	C-14
8	CLKOUT[2]#	F-25	42	MDAT[47]	B-22	76	MECC[6]	A-13
9	MDAT[57]	C-27	43	MAB[13]	E-18	77	MECC[2]	B-13
10	DM[7]	C-28	44	MDAT[43]	A-22	78	DQS[8]	A-12
11	CLKOUT[2]	E-26	45	RASA#	E-19	79	MECC[1]	B-12
12	CS[6]#	D-25	46	MAA[14]	E-17	80	DM[8]	C-13
13	MDAT[56]	B-28	47	RASB#	D-19	81	MECC[5]	A-11
14	CLKOUT[5]#	D-27	48	MDAT[46]	C-21	82	MAA[00]	E-14
15	CS[5]#	E-24	49	MDAT[42]	B-21	83	MECC[3]	D-13
16	MDAT[60]	B-27	50	DQS[5]	A-21	84	CLKOUT[0]#	E-13
17	CS[1]#	E-23	51	MDAT[41]	C-19	85	MECC[0]	C-12
18	MDAT[61]	C-26	52	DM[5]	A-20	86	MECC[4]	A-10
19	MDAT[51]	A-27	53	MAA[13]	D-18	87	CLKOUT[3]	C-11
20	MDAT[55]	C-25	54	MDAT[44]	C-18	88	MDAT[31]	B-10
21	CS[7]#	E-25	55	MDAT[45]	B-19	89	MAA[01]	E-11
22	DM[6]	C-24	56	MDAT[40]	A-19	90	MDAT[27]	C-10
23	MDAT[50]	A-26	57	MDAT[35]	B-18	91	MDAT[30]	B-9
24	CASA#	E-22	58	MAA[10]	E-16	92	CLKOUT[0]	D-12
25	DQS[6]	B-25	59	MAB[14]	C-17	93	DM[3]	C-9
26	CS[4]#	D-24	60	DM[4]	B-16	94	DQS[3]	A-8
27	CASB#	E-21	61	MAB[10]	D-16	95	MAB[01]	D-10
28	MDAT[54]	A-25	62	MDAT[34]	C-16	96	CLKOUT[3]#	E-12
29	MDAT[53]	B-24	63	MDAT[39]	A-18	97	MDAT[26]	A-9
30	CS[3]#	C-23	64	MDAT[38]	A-17	98	MAB[02]	E-10
31	MAA[03]	C-8	65	MDAT[16]	B-3	99	MAA[11]	H-4
32	MAA[02]	D-9	66	MAA[05]	E-5	100	CKEA	K-5
33	MDAT[25]	A-7	67	MAB[08]	D-4	101	MDAT[02]	H-3
34	MDAT[29]	B-7	68	MAB[07]	F-5	102	MDAT[07]	G-1

Table 5: AMD-761™ System Controller DDR NAND Tree Ordering (Continued)

Order	Input Pin Name	Ball	Order	Input Pin Name	Ball	Order	Input Pin Name	Ball
103	MAB[03]	E-9	120	MAB[09]	G-5	137	MAA[12]	K-4
104	MDAT[28]	C-7	121	MDAT[11]	B-2	138	CKEB	J-3
105	MDAT[24]	A-6	122	MDAT[15]	D-3	139	MDAT[06]	H-2
106	MAA[04]	D-7	123	MDAT[10]	C-1	140	CLKOUT[1]#	M-5
107	MDAT[22]	A-5	124	DQS[1]	E-3	141	DQS[0]	H-1
108	MAB[04]	E-8	125	MAA[08]	E-4	142	CLKOUT[4]#	L-5
109	MDAT[23]	C-6	126	MDAT[14]	D-2	143	CLKOUT[1]	N-5
110	MDAT[19]	B-6	127	MAA[07]	F-3	144	CLKOUT[4]	L-4
111	MDAT[18]	A-4	128	DM[1]	D-1	145	MDAT[01]	K-3
112	MAB[06]	D-6	129	MAB[11]	H-5	146	DM[0]	J-1
113	DM[2]	B-4	130	MDAT[13]	E-2	147	MDAT[04]	L-3
114	MAA[06]	E-7	131	MAA[09]	G-4	148	MDAT[00]	K-1
115	DQS[2]	C-5	132	MAB[12]	J-5	149	MDAT[05]	K-2
116	MDAT[21]	A-3	133	MDAT[09]	E-1			
117	MAB[05]	E-6	134	MDAT[12]	F-1			
118	MDAT[17]	C-4	135	MDAT[08]	G-3			
119	MDAT[20]	C-3	136	MDAT[03]	G-2			

Table 6: AMD-761™ PCI NAND Tree Ordering

Order	Input Pin Name	Ball	Order	Input Pin Name	Ball	Order	Input Pin Name	Ball
1	AD[31]	AG-16	22	CBE[1]#	AF-22	43	AD[05]	AF-25
2	REQ[6]#	AH-17	23	DEVSEL#	AF-21	44	AD[13]	AG-27
3	GNT[5]#	AJ-18	24	AD[28]	AJ-23	45	AD[03]	AE-25
4	REQ[5]#	AH-18	25	AD[26]	AH-23	46	AD[01]	AF-26
5	GNT[6]#	AG-17	26	SERR#	AE-21	47	AD[11]	AH-28
6	REQ[4]#	AJ-19	27	AD[24]	AG-23	48	AD[00]	AE-26
7	AD[29]	AE-16	28	AD[19]	AJ-24	49	SBGNT#	AD-25
8	AD[27]	AF-17	29	AD[12]	AF-23	50	AD[09]	AG-28
9	REQ[3]#	AH-19	30	AD[18]	AJ-25	51	WSC#	AC-25
10	AD[25]	AE-17	31	AD[14]	AE-22	52	AD[06]	AF-27
11	GNT[4]#	AG-18	32	AD[22]	AH-24	53	CBE[0]#	AG-29
12	CBE[3]#	AF-18	33	AD[20]	AG-24	54	SBREQ#	AE-27
13	AD[17]	AE-19	34	AD[16]	AH-25	55	AD[04]	AF-28
14	REQ[2]#	AH-20	35	TRDY#	AJ-26	56	AD[02]	AF-29
15	REQ[1]#	AH-21	36	AD[08]	AF-24			
16	AD[21]	AF-19	37	STOP#	AH-26			
17	REQ[0]#	AG-21	38	AD[10]	AE-23			
18	CBE[2]#	AF-20	39	FRAME#	AG-25			
19	AD[23]	AE-18	40	PAR	AJ-27			
20	AD[30]	AH-22	41	AD[07]	AE-24			
21	IRDY#	AE-20	42	AD[15]	AH-27			

3.3 PLL Bypass Test Mode

PLL bypass test mode provides a method to clock the Northbridge core logic directly from an external source without the need for the internal PLLs of the AMD-761 system controller. This test mode is sometimes useful for motherboard debug and is required in the three-state and NAND tree test modes.

PLL bypass mode is entered by asserting the TEST# pin Low and pulling the AD[09] pin High. There are two clocking options for PLL bypass mode as listed in Table 7. Because the AMD-761 system controller internal logic normally uses clocks that are 2x the SYSCLK input and 2x/4x the AGPCLK input, the PLL bypass mode requires that either 2x or 4x clocks be driven in this mode, but they can be driven at a much lower frequency for test purposes (see Table 7). Note that when operating in this mode, the minimum clock frequency most likely will be dictated by the surrounding logic, such as the DDR interface.

Table 7. Clocking Options in PLL Bypass Test Mode

Mode	C/BE[1]#	SYSCLK	AGPCLK	Comments
Normal	0	2x	2x	PLLs bypassed, drives a 2x clock to internal divider, and resulting 1x clock to internal logic.
AGP-4x Testing	1	2x	4x	Same as above, except allows 4x clock to accommodate 4x AGP testing.

The PLL reset function can be invoked by asserting a Low on the PCI IRDY# pin This procedure provides a synchronous reset for the clocking, but probably is not required when using this test mode for motherboard debug.

Note: *AD[29] must be pulled Low when entering PLL bypass test mode to enable the PLL reset function capability.*

3.4 Clock Output Test Mode

The clock output test mode provides external visibility of the two PLLs used to generate the clocks for the processor/memory and AGP clock domains. In this test mode, the PLLs are running, and the output clocks are driven to GNT[6:5]# pins. System designers that intend to make use of this test feature should provide 0-ohm resistors on these pins to isolate the PCI peripherals when observing the clocks.

This test mode is entered by the Low assertion of the TEST# pin while pulling the PCI bus PAR pin Low. Additional pinstraps are then used to select the various clock outputs as illustrated in Table 8.

Table 8. Clock Output Test Mode Options

AD[07:05]	SYSCLK PLL Output GNT[5]# Pin	AD[14:12]	AGPCLK PLL Output GNT[6]# Pin
000	1x SYSCLK clock after internal divide by two	000	1x AGPCLK clock after internal divide by two
001	SYSCLK input	001	AGPCLK input
010	Reserved, undefined	010	Reserved, undefined
011	Reserved, undefined	011	Reserved, undefined
100	1x SYSCLK output from SYSCLK PLL	100	1x SYSCLK output from SYSCLK PLL
101	Reserved, undefined	101	Reserved, undefined
110	Reserved, undefined	110	Reserved, undefined
111	Reserved, undefined	111	Reserved, undefined

4 Electrical Data

This section provides electrical data for the AMD-761™ system controller.

4.1 Absolute Ratings

The AMD-761 system controller is not designed to operate beyond the parameters shown in Table 9.

Note: *The absolute ratings in Table 9 and associated conditions must be adhered to in order to avoid damage to the AMD-761™ system controller and motherboard. Systems using the AMD-761 system controller must be designed to ensure that the power supply and system logic board guarantee that these parameters are not violated. VIOLATION OF THE ABSOLUTE RATINGS WILL VOID THE PRODUCT WARRANTY.*

Table 9. Absolute Ratings*

Parameter	Minimum	Maximum	Comments
VDD_CORE, A_VDD, K7_VCORE	–0.5 V	3.6 V	Core, PLL, DDR I/O, and AMD Athlon™ System Bus I/O supplies
VDD_AGP, VDD_PCI	–0.5 V	4.6 V	AGP and PCI I/O supplies
REF_5V	–0.5 VI	5.25 V	
V_{PIN} DDR	–0.5 V	4.6 V	Voltage on any pin.
V_{PIN} AMD Athlon™ System Bus	–0.5 V	3.6 V	Voltage on any pin.
V_{PIN} PCI	–0.5 V	5.25 V	Voltage on any pin.
V_{PIN} AGP	–0.5 V	4.6 V	Voltage on any pin.
V_{PIN} Miscellaneous	–0.5 V	4.6 V	Voltage on any pin.
T_{CASE} (Under Bias)		85 °C	
$T_{STORAGE}$	-65 °C	150 °C	

*This table contains preliminary information, which is subject to change.

4.2 Operating Ranges

The AMD-761 system controller is designed to provide functional operation if the voltage and temperature parameters are within the limits defined in Table 10.

Table 10. Operating Ranges*

Parameter	Minimum	Typical	Maximum	Comments
REF_5V	4.75	5.0	5.25	For PCI 5-V tolerance
VDD_CORE, A_VDD	2.375 V	2.5 V	2.625 V	Also includes DDR I/Os
K7_VCORE	1.50 V	1.6 V	1.70 V	AMD Athlon™ system bus I/O VDD
VDD_AGP	1.425 V	1.5 V	1.575 V	1x/2x/4x modes
VDD_AGP	3.135 V	3.3 V	3.465 V	1x/2x modes only
VDD_PCI	3.135 V	3.3 V	3.465 V	3.3-V signalling environment only
T_{CASE}			85°C	

*This table contains preliminary information, which is subject to change. The voltage applied to V_{DD} should-never exceed the voltage applied to REF_5V.

4.3 DC Characteristics

Table 11 shows DC characteristics (IDD). Table 12 shows the DC characteristics for the DDR Interface. Table 13 on page 48 shows DC characteristics for the PCI I/Os. Table 14 on page 48 shows DC characteristics for AGP I/Os in 1x mode. Table 15 on page 49 shows DC characteristics for AGP I/Os in 2x and 4x modes.

Table 11. DC Characteristics (IDD)*

Symbol	Parameter Description	Preliminary Data		Comments
		Min	Max	
I_{DD1}	VDD_CORE (2.5 V) Dynamic	1.25 A	1.5 A	
I_{DD2}	VDD_PCI (3.3 V) Dynamic	40 mA	70 mA	
I_{DD3}	VDD_AGP (1.5 V/3.3 V) Dynamic	10 mA	20 mA	
I_{DD4}	A_VDD (2.5 V) Dynamic	5 mA	10 mA	
I_{DD5}	K7_VCORE (Dynamic	125 mA	250 mA	

*This table contains preliminary information, which is subject to change.

Table 12. DC Characteristics for DDR Interface*

Symbol	Parameter Description	Preliminary Data		Comments
		Min	Max	
V_{IL}	Input Low Voltage	–300 mV	V_{REF} – 180 mV	Data, DQS pins
V_{IH}	Input High Voltage	V_{REF} + 180 mV	VDD_CORE + 300 mV	Data, DQS pins
V_{OL}	Output Low Voltage		0.15 * VDD_CORE	(15.2 mA/-15.2 mA) JEDEC Test conditions
V_{OH}	Output High Voltage	0.85 * VDD_CORE		
V_{REF}	DC Input Reference Voltage	1.15 V	1.35 V	
I_{LI}	Input Leakage Current	–10 µA	10 µA	$0 < V_{IN} <$ VDD_CORE
I_{LO}	Three-state Leakage Current	–10 µA	10 µA	
C_{IN}	Input Capacitance	4 pF	12 pF	

*This table contains preliminary information, which is subject to change.

Table 13. DC Characteristics for PCI I/Os*

Symbol	Parameter Description	Condition	Min	Max	Units	Notes
V_{IH}	Input High Voltage		0.5 V_{CC}	V_{CC} + 0.5	V	
V_{IL}	Input Low Voltage		–0.5	0.3 V_{CC}	V	
I_{IL}	Input Leakage Current	$0 < V_{IN} < V_{CC}$		±10	µA	1
V_{OH}	Output High Voltage	I_{OUT} = –500 µA	0.9 V_{CC}		V	
V_{OL}	Output Low Voltage	I_{OUT} = 1500 µA		0.1 V_{CC}	V	
C_{IN}	Input Pin Capacitance			10	pF	2

Notes:

** This table contains preliminary information, which is subject to change.*

1. Input leakage currents include hi-Z output leakage for all bi-directional buffers with three-state outputs.

2. Absolute maximum pin capacitance for a PCI input is 10 pF (except for CLK) with an exception granted to motherboard-only devices up to 16 pF in order to accommodate PGA packaging. Generally, this means that components for expansion boards need to use alternatives to ceramic PGA packaging—that is, PQFP, SGA, etc.

Table 14. AGP 1x Mode DC Specifications*

DC Specifications for AGP 1x Signalling at 3.3 Volts						
Symbol	**Parameter Description**	**Condition**	**Min**	**Max**	**Units**	**Notes**
V_{IH}	Input High Voltage		0.5 V_{DDQ}	V_{DDQ} + 0.5	V	
V_{IL}	Input Low Voltage		–0.5	0.3 V_{DDQ}	V	
I_{IL}	Input Leakage Current	$0 < V_{IN} < V_{DDQ}$		±10	µA	
V_{OH}	Output High Voltage	I_{OUT} = –500 µA	0.9 V_{DDQ}		V	
V_{OL}	Output Low Voltage	I_{OUT} = 1500 µA		0.1 V_{DDQ}	V	
C_{IN}	Input Pin Capacitance			8	pF	1
DC Specifications for AGP 1x Signalling at 1.5 Volts						
Symbol	**Parameter Description**	**Condition**	**Min**	**Max**	**Units**	**Notes**
V_{IH}	Input High Voltage		0.6 V_{DDQ}	V_{DDQ} + 0.5	V	
V_{IL}	Input Low Voltage		–0.5	0.4 V_{DDQ}	V	
I_{IL}	Input Leakage Current	$0 < V_{IN} < V_{DDQ}$		±10	µA	
V_{OH}	Output High Voltage	I_{OUT} = –200 µA	0.85 V_{DDQ}		V	
V_{OL}	Output Low Voltage	I_{OUT} = 1000 µA		0.15 V_{DDQ}	V	
C_{IN}	Input Pin Capacitance			8	pF	1

Notes:

** This table contains preliminary information, which is subject to change.*

1. Absolute maximum pin capacitance for an AGP-compliant component input is 8 pF (except for CLK) with an exception granted to motherboard-only devices, which could be up to 16 pF in order to accommodate PGA packaging. Generally, this means that components for expansion boards need to use alternatives to ceramic PGA packaging—that is, PQFP, BGA, etc.

Table 15 lists incremental parameters required for supporting AGP 2X with 3.3-V signalling and AGP 4X.

Table 15. AGP 2x and 4x Mode DC Specifications*

DC Specifications for 2x Mode Only at 3.3-Volt Signalling						
Symbol	**Parameter Description**	**Condition**	**Min**	**Max**	**Units**	**Notes**
V_{REF}	Input Reference Voltage		0.39 V_{DDQ}	0.41 V_{DDQ}	V	1, 2
I_{REF}	V_{REF} Pin Input Current	$0 < V_{IN} < V_{DDQ}$		±10	µA	2
C_{IN}	Input Pin Capacitance			8	pF	3
ΔC_{IN}	Strobe to Data Pin Capacitance Delta		–1	2	pF	3, 4
DC Specifications for 2x or 4x Mode at 1.5-Volt Signalling						
Symbol	**Parameter Description**	**Condition**	**Min**	**Max**	**Units**	**Notes**
V_{REF}	Input Reference Voltage		0.48 V_{DDQ}	0.52 V_{DDQ}	V	1, 2
I_{REF}	V_{REF} Pin Input Current	$0 < V_{IN} < V_{DDQ}$		±5	µA	2
C_{IN}	Input Pin Capacitance			8	pF	3
ΔC_{IN}	Strobe to Data Pin Capacitance Delta	2x Mode 4x Mode	–1 –1	2 1	pF	3, 4

Notes:

** This table contains preliminary information, which is subject to change.*

1. AGP allows differential input receivers to achieve the tighter timing tolerances needed for 133 Mbytes/s. Nominal value of V_{REF} is 0.4 V_{DDQ} for 3.3-V signalling and 0.5-V_{DDQ} for 1.5-V signalling. V_{REF} can be designed with 2% resistors to achieve the specified minimum and maximum values. The value of V_{REF} is intended to specify the center point of the V_{IL}/V_{IH} range. For the 3.3-V signalling case, at nominal V_{DDQ} (3.3 V), V_{REF} is 1.32 V ± 2.5%. A single input interface buffer can be designed to meet the V_{IL}/V_{IH} levels of both the AGP and PCI specifications. As in other AGP specifications, note that the V_{DDQ} references the I/O ring supply voltage and not the component supply.

2. Although a differential input buffer is not a required implementation, it is recommended especially at higher data transfer rates where there is less timing margin. All designs regardless of implementation style must meet all other specifications. Component designs requiring a reference are required to adhere to the V_{REF} and I_{REF} specifications and to facilitate a common reference circuit. (A common reference circuit is not applicable to add-in card designs, because V_{REF} is not supplied via the connector.)

3. Capacitance specifications refer only to pin capacitance on the AGP-compliant components used on the AGP interface.

4. Delta C_{IN} is required to restrict timing variations resulting from differences in input pin capacitance between the strobe and associated data pins. This delta only applies between signal groups and their associated strobes: AD_STB1, AD_STB1#=>AD[31::16], and C/BE[3::2]; AD_STB0, AD_STB0#=>AD[15::00], and C/BE[1::0]#; SB_STB, SB_STB#=>SBA[7::0]. (Complementary strobes apply to 4x mode only.)

4.4 Power Dissipation

Table 16 shows typical and maximum power dissipation of the AMD-761 system controller during normal and reduced power states. The measurements are taken with the V_{DD} shown.

Table 16. Typical and Maximum Power Dissipation*

Supply	Normal Operation		Low-Power States		
	Typical	Maximum	ACPI S1 State Unbuffered DIMMs	ACPI S1 State Registered DIMMs	ACPI S3 State
VDD_CORE					
100 MHz	3 W	3.75 W	100 mW	125 mW	50 mW
133 MHz	4 W	5 W	133 mW	165 mW	65 mW

*This table contains preliminary information, which is subject to change.

4.5 Switching Characteristics and Requirements

The AMD-761 system controller signal switching characteristics and requirements are presented in Tables 17 through 28. All signal timings are based on the following conditions:

- The target signals are input or output signals that are switching from logical 0 to 1, or from logical 1 to 0.
- Measurements are taken from the time the reference signal (AGPCLK, PCICLK, CLKOUT, SYSCLK, or RESET#) passes through 1.5 V to the time the target signal passes through 1.5 V.
- Parameters are within the range of those listed in "Operating Ranges" on page 46.

4.5.1 Clock Switching Requirements

Table 17 on page 52 contains the switching characteristics of the SYSCLK input to the AMD-761 system controller for 100-MHz processor bus operation. These timings are all measured with respect to the voltage levels indicated by Table 10 on 52. Clock skew requirements are shown in Figure 12 on page 53. Table 18 on page 52 contains the switching characteristics of the AGPCLK input for 66-MHz PCI bus operation. Table 19 on page 53 contains the switching characteristics of the PCICLK input for 33-MHz PCI bus operation. These timings are all measured with respect to the voltage levels indicated by Figure 11 on page 53.

The clock period stability specifies the variance (jitter) allowed between successive periods of the clock inputs measured at appropriate reference voltage. This parameter must be considered as one of the elements of clock skew between the AMD-761 system controller and the system logic.

Table 17. SYSCLK Switching Requirements*

Symbol	Parameter Description	Preliminary Data		Figure	Comments
		Min	Max		
$1/t_{CKIo}$	Frequency		133 MHz	10	
t_3/t_{CKIo} x 100	SYSCLK Duty Cycle	45%	55%	10	1.15-V reference
t_4	SYSCLK Falling Edge Slew Rate	TBD	1.0 V/ns	10	
t_5	SYSCLK Rising Edge Slew Rate	TBD	1.0 V/ns	10	
	SYSCLK Period Stability **100 MHz** **133 MHz**		 ± 200 ps ± 150 ps		1.15-V reference

*This table contains preliminary information, which is subject to change.

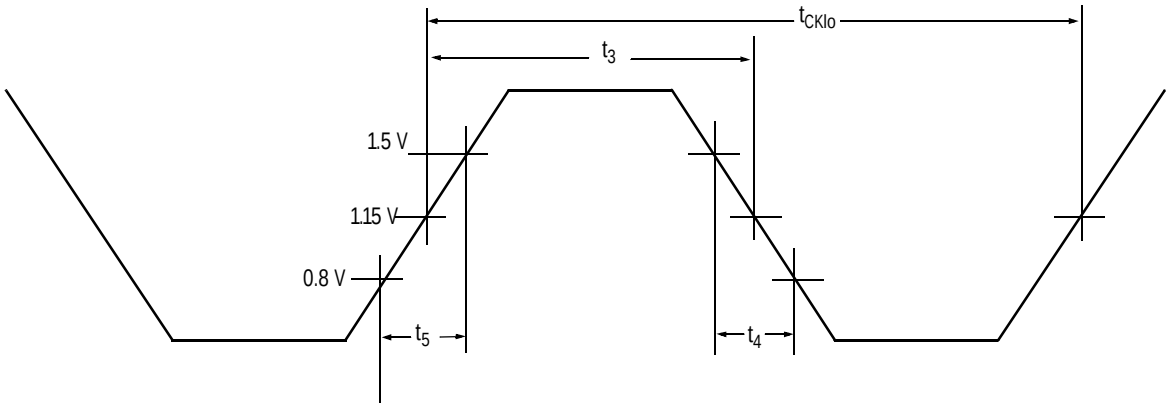


Figure 10. SYSCLK Waveform

Table 18. AGPCLK Switching Requirements for 66-MHz Bus Operation*

Symbol	Parameter Description	Preliminary Data		Figure	Comments
		Min	Max		
$1/t_{CKhi}$	Frequency		66 MHz	11	
t_{CKIo}	AGPCLK High Time	6.0 ns		11	
t_3	AGPCLK Low Time	6.0 ns		11	
	AGPCLK Fall Time	0.15 ns	2 ns		
	AGPCLK Rise Time	0.15 ns	2 ns		
t_{SKEW}	SYSCLK to AGPCLK Skew	–500 ps	500 ps	12	Rising to rising edges
	AGPCLK Period Stability		± 300 ps		1.5-V reference

*This table contains preliminary information, which is subject to change.

Table 19. PCICLK Switching Requirements for 33-MHz PCI Bus*

Symbol	Parameter Description	Preliminary Data		Figure	Comments
		Min	Max		
t_{CKhi}	PCICLK Cycle	30 ns	∞	11	
t_{CKlo}	PCICLK High Time	11.0 ns		11	
t_3	PCICLK Low Time	11.0 ns		11	
	PCICLK Fall Time	1 V/ns	2 V/ns		
	PCICLK Rise Time	1 V/ns	2 V/ns		
	PCICLK Period Stability		± 300 ps		1.5-V reference

*This table contains preliminary information, which is subject to change.

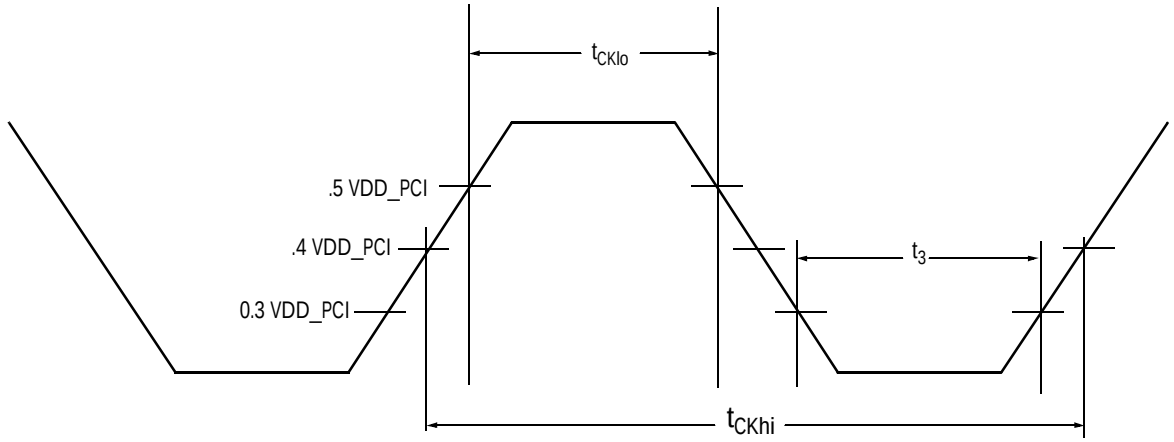


Figure 11. AGPCLK and PCICLK Waveform

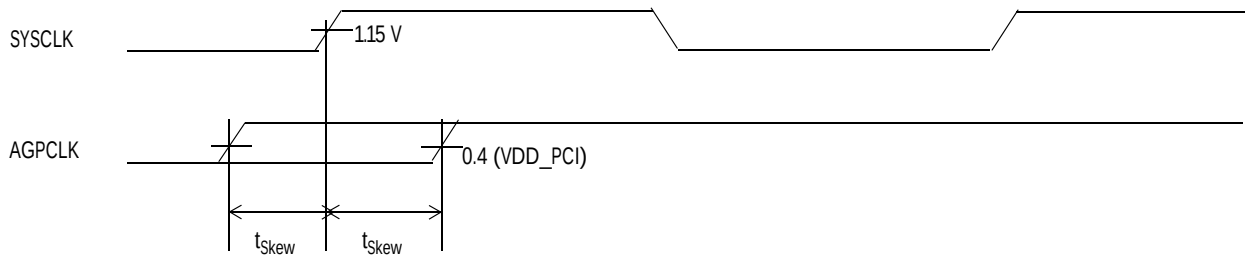


Figure 12. Clock Skew Requirements

4.5.2 DDR Interface Timing

Table 20 on page 54 and Table 21 on page 54 show the DDR SDRAM interface timings. Figure 13 on page 54 shows DDR clock specifications. The controller's DDR DRAM interface complies to JEDEC specifications for 100/133-MHz device timing.

Table 20. DDR Clock Switching Characteristics for 100-MHz DDR Operation*

Symbol	Parameter Description	Preliminary Data		Figure	Comments
		Min	Max		
	Frequency		100 MHz		
t_{CKhi}	CLKOUTH/L[5:0] High Time	4.75 ns		13	
t_{CKlo}	CLKOUTH/L[5:0] Low Time	4.75 ns		13	
	CLKOUTH/L[5:0] Fall Time	0.86 ns	1.30 ns		Drive strength: P = 3, N = 2; P_{SLEW} = 5, N_{SLEW} = 5
	CLKOUTH/L[5:0] Rise Time	0.86 ns	1.30 ns		
	CLKOUTH/L[5:0] Period Stability		± 2%		
	CLKOUTH/L[5:0] Skew	0	0.12 ns		Relative to all other CLKOUTH/L pairs

*This table contains preliminary information, which is subject to change.

Table 21. DDR Clock Switching Characteristics for 133-MHz DDR Operation*

Symbol	Parameter Description	Preliminary Data		Figure	Comments
		Min	Max		
	Frequency		133 MHz		
t_{CKhi}	CLKOUTH/L[5:0] High Time	3.625 ns		13	
t_{CKlo}	CLKOUTH/L[5:0] Low Time	3.625 ns		13	
	CLKOUTH/L[5:0] Fall Time	0.86 ns	1.30 ns		Drive strength: P = 3, N = 2; P_{SLEW} = 5, N_{SLEW} = 5
	CLKOUTH/L[5:0] Rise Time	0.86 ns	1.30 ns		
	CLKOUTH/L[5:0] Period Stability		± 2%		
	CLKOUTH/L[5:0] Skew	0	0.12 ns		Relative to all other CLKOUTH/L pairs

*This table contains preliminary information, which is subject to change.

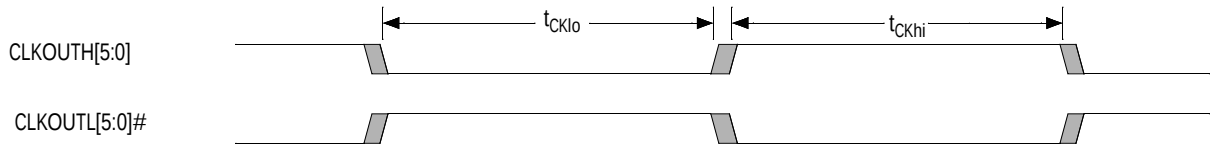


Figure 13. DDR Clock Specifications

Table 22 and Table 23 on page 56 show the AMD-761 system controller preliminary timing information.

Table 22. AMD-761 System Controller Preliminary DDR Timing Information (100 MHz)*

Symbol	Parameter Description	Min	Max	Unit	Figure
V_{IL} (AC)	AC Input Low Voltage		VREF – 0.35	V	
V_{IH} (AC)	AC Input High Voltage	VREF + 0.35		V	
t_{ADsu}	ADDR/CMD Setup to CK (Delay Disabled)[1]	6.20		ns	Figure 15 on page 58
t_{ADsu}	ADDR/CMD Setup to CK (Delay Enabled)[1]	5.90		ns	
t_{ADhld}	ADDR/CMD Hold from CK (Delay Disabled)[1]	2.00		ns	
t_{ADhld}	ADDR/CMD Hold from CK (Delay Enabled)[1]	2.30		ns	
t_{DQsu}	DQ/DM Setup to DQS[2]	1.70		ns	
t_{DQhld}	DQ/DM Hold from DQS[2]	1.50		ns	
t_{WPREsu}	Write Preamble Setup	1.30		ns	
$t_{WPREhld}$	Write Preamble Hold	5.30		ns	
t_{WpostA}	Write Postamble	4.70	5.50	ns	
t_{DSsu}	DQS Falling Edge to Next CK Rising Edge	3.50		ns	
t_{DQSdly}	Write Command to First DQS Latching Transition	9.90	11.30	ns	
t_{DQSQrd}	DQ Setup to DQS, Memory Reads (PDL = 0)[3]	0.40		ns	Figure 17 on page 60
t_{DQSQrd}	DQ Setup to DQS, Memory Reads (PDL = default)[3]		1.50	ns	
t_{QHrd}	DQ Hold from DQS, Memory Reads (PDL = 0)[4]		2.22	ns	
t_{QHrd}	DQ Hold from DQS, Memory Reads (PDL = default)[4]		2.30	ns	
t_{DQS2ck}	DQS to CK, Memory Controller Reads[5]	1.00	3.90	ns	

Notes:

* *This table contains preliminary information, which is subject to change. Timing reference load (applied to all chip-level outputs) used for all information contained herein is a 30-pF capacitance.*

1. *Additional ADDR/CMD HOLD is provided by setting configuration bits Dev0:F0:0x54 [30:29].*
2. *The specified values apply for both x4 and non-x4 DQ/DM versus DQS write timing, thus includes timing when DM signals act as DQS signals during x4 DIMM write accesses.*
3. *Minimum refers to DQS lagging DQ and maximum refers to DQS leading DQ. If the PDL is programmed to zero delay, the minimum specification requires that DQS lag DQ by the amount shown so as to meet setup requirements. If the PDL is programmed to the default delay, the maximum specification requires that DQS lead DQ by no more than the amount shown.*
4. *If the PDL is programmed to zero delay, the maximum specification requires that DQS not lag DQ greater than the amount specified. If the PDL is programmed to the default delay, the maximum specification requires that DQS not lag DQ greater than the amount specified. A violation of this maximum results in the DQS missing the capture of data at the back end of the DQ data valid window.*
5. *This timing is the minimum and maximum round trip loop timing. The minimum refers to the earliest that DQS can be returned relative to any CLKOUT signal, and the maximum refers to the latest that DQS can be returned relative to CLKOUT with the default specified PDL setting.*

Table 23: AMD-761 System Controller Preliminary DDR Timing Information(133 MHz)*

Symbol	Parameter Description	Min	Max	Unit	Figure
V_{IL} (AC)	AC Input Low Voltage		VREF – 0.35	V	
V_{IH} (AC)	AC Input High Voltage	VREF + 0.35		V	
t_{ADsu}	ADDR/CMD Setup to CK (Delay Disabled)[1]	4.30		ns	Figure 15 on page 58
t_{ADsu}	ADDR/CMD Setup to CK (Delay Enabled)[1]	4.00		ns	
t_{ADhld}	ADDR/CMD Hold from CK (Delay Disabled)[1]	1.70		ns	
t_{ADhld}	ADDR/CMD Hold from CK (Delay Enabled)[1]	2.00		ns	
t_{DQsu}	DQ/DM Setup to DQS[2]	1.20		ns	
t_{DQhld}	DQ/DM Hold from DQS[2]	1.00		ns	
t_{WPREsu}	Write Preamble Setup	0.80		ns	
$t_{WPREhld}$	Write Preamble Hold	3.90		ns	
t_{WpostA}	Write Postamble	3.50	5.00	ns	
t_{DSsu}	DQS Falling Edge to Next CK Rising Edge	2.20		ns	
t_{DQSdly}	Write Command to First DQS Latching Transition	7.50	8.80	ns	
t_{DQSQrd}	DQ Setup to DQS, Memory Reads (PDL = 0)[3]	0.40		ns	Figure 17 on page 60
t_{DQSQrd}	DQ Setup to DQS, Memory Reads (PDL = default)[3]		1.00	ns	
t_{QHrd}	DQ Hold from DQS, Memory Reads (PDL = 0)[4]		3.10	ns	
t_{QHrd}	DQ Hold from DQS, Memory Reads (PDL = default)[4]		1.60	ns	
t_{DQS2ck}	DQS to CK, Memory Controller Reads[5]	1.00	3.90	ns	

Notes:

* *This table contains preliminary information, which is subject to change. Timing reference load (applied to all chip-level outputs) used for all information contained herein is a 30-pF capacitance. A CL of 2.5 is used unless otherwise indicated.*

1. *Additional ADDR/CMD HOLD is provided by setting configuration bits Dev0:F0:0x54 [30:29].*
2. *The specified values apply for both x4 and non-x4 DQ/DM versus DQS write timing, thus includes timing when DM signals act as DQS signals during x4 DIMM write accesses.*
3. *Minimum refers to DQS lagging DQ and maximum refers to DQS leading DQ. If the PDL is programmed to zero delay, the minimum specification requires that DQS lag DQ by the amount shown so as to meet setup requirements. If the PDL is programmed to the default delay, the maximum specification requires that DQS lead DQ by no more than the amount shown.*
4. *If the PDL is programmed to zero delay, the maximum specification requires that DQS not lag DQ greater than the amount specified. If the PDL is programmed to the default delay, the maximum specification requires that DQS not lag DQ greater than the amount specified. A violation of this maximum results in the DQS missing the capture of data at the back end of the DQ data valid window.*
5. *This timing is the minimum and maximum round trip loop timing. The minimum refers to the earliest that DQS can be returned relative to any CLKOUT signal and the maximum refers to the latest that DQS can be returned relative to CLKOUT with the default specified PDL setting.*

DDR Write Timing

Figure 14 on page 57 shows a DDR interface output block diagram. Figure 15 on page 58 shows basic AC timing for DDR write cycles.

Note: *All information shown under DDR Write Timing is preliminary.*

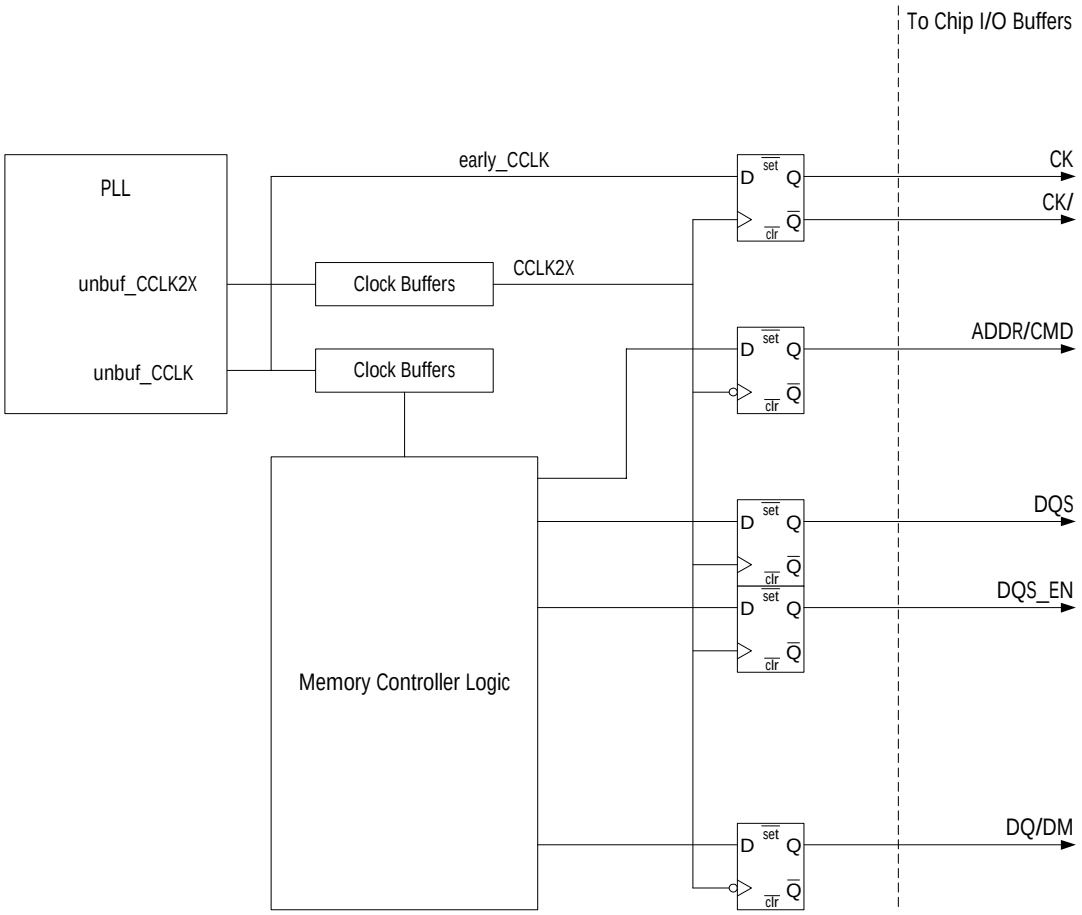
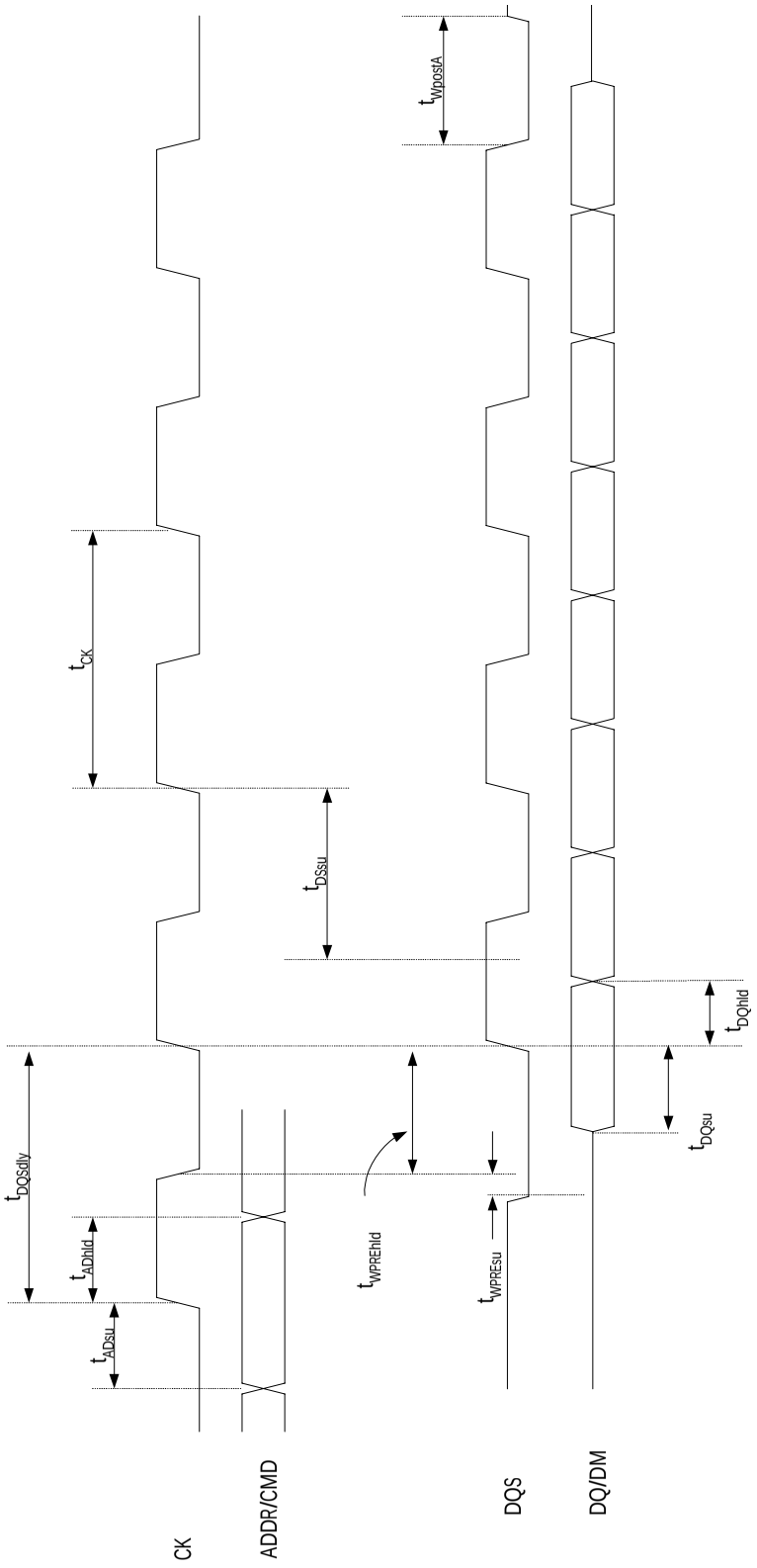


Figure 14. AMD-761™ System Controller DDR Interface Outputs Conceptual Block Diagram



Note: Timing parameter symbols defined at controller interface, not at memory device interface.

Figure 15. Address/Command and Memory Write Cycle Timing

DDR Read Timing

Figure 16 shows a block diagram of the AMD-761 system controller DDR interface inputs, and Figure 17 on page 60 shows memory read cycle timing.

Note: *All information shown under DDR Read Timing is preliminary.*

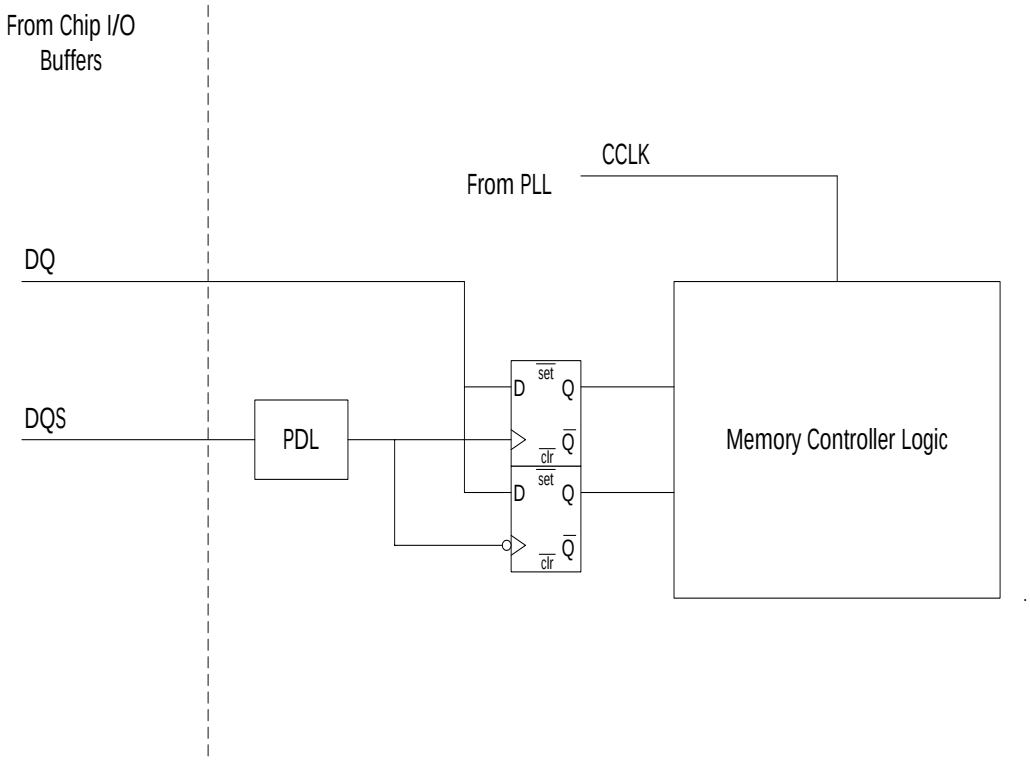
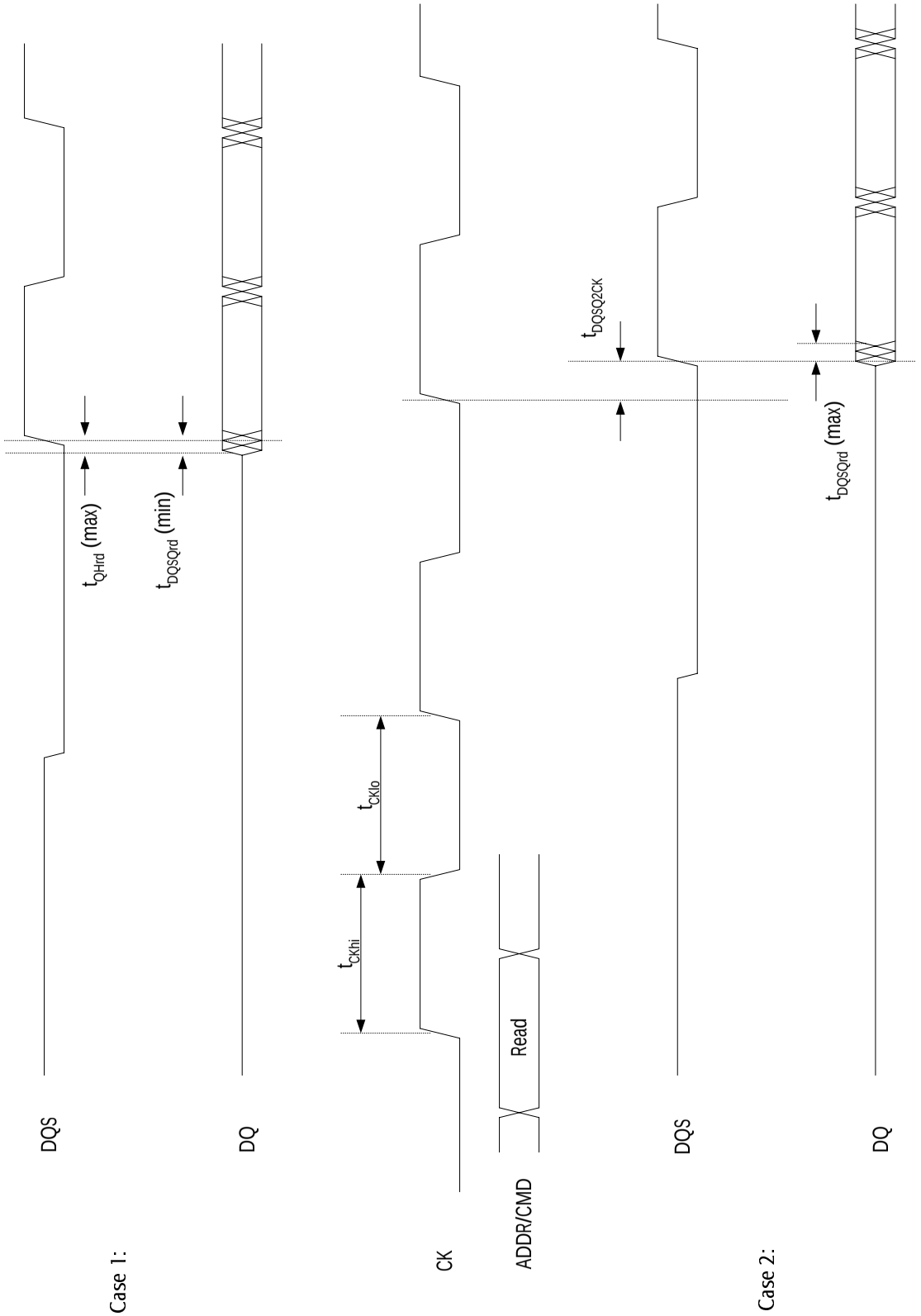


Figure 16. AMD-761™ System Controller DDR Interface Inputs Conceptual Block Diagram



Note: Timing parameter symbols defined at controller interface, not at memory device interface (CAS latency = 2 shown unregistered).

Figure 17. Memory Read Cycle Timing

4.5.3 AGP/PCI Signals

Valid Delay, Float, Setup, and Hold Timings

The valid delay and float timings for output signals during functional operation are relative to the rising edge of the given clock. The maximum valid delay timings are provided to allow a system designer to determine if setup times can be met. Likewise, the minimum valid delay timings are used to analyze hold times.

The setup and hold time requirements for the AMD-761 system controller input signals presented here must be met by any device that interfaces with it to assure the proper operation of the AMD-761 system controller.

Figure 18 shows the relationship between the rising clock edge and setup, hold, and valid data timings.

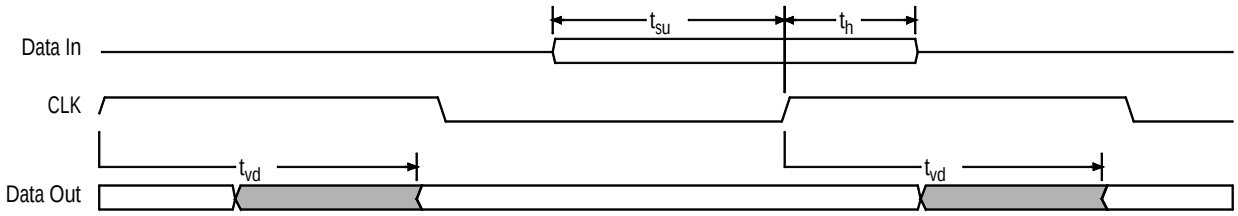


Figure 18. Setup, Hold, and Valid Delay Timings

AGP Interface Timing

The 4x AGP interface of the AMD-761 system controller can operate in three modes—1x, 2x, and 4x, and complies to the AGP specification parameters.

The timings for the 1x mode, shown in Table 24 on page 62, are relative to AGPCLK. The timings for the 2x mode, shown in Table 25 on page 63, are relative to the respective strobe.

The timings for the 4x mode, shown in Table 26 on page 64, apply only to the inner loop 4x clock mode signals (AD, C/BE#, and SBA).

Figure 19 on page 64 shows an AGP 2x strobe/data turnaround timing diagram. Figure 20 on page 65 and Figure 21 on page 65 show AGP 2x and 4x timing diagrams, respectively. Figure 22 on page 66 shows an AGP 4x strobe/data turnaround timing diagram.

Table 24. AGP 1x Mode Timings*

Symbol	Parameter Description	Preliminary Data		Figure	Notes
		Min	Max		
Input Signal Requirements					
t_{su}	A_AD[31:0] Setup Time	5.5 ns		18	1
	Setup time for A_FRAME#A_STOP# A_TRDY#A_DEVSEL# A_IRDY#A_C/BE[3:0]# A_REQ# ADSTB[1:0] SBA[7:0] SBSTB RBF#WBF# A_PAR PIPE#	6 ns		18	1
t_h	A_AD[31:0] Hold Time	0 ns		18	1
	Hold time for A_FRAME#A_STOP# A_TRDY#A_DEVSEL# A_IRDY#A_C/BE[3:0]# A_REQ# ADSTB[1:0] SBA[7:0] SBSTB RBF#WBF# A_PAR A_SERR# PIPE#	0 ns		18	1
Output Signal Characteristics					
t_{vd}	A_AD[31:0] Valid Delay	1 ns	6.0 ns	18	1
	A_C/BE[3:0]# Valid Delay	1 ns	5.5 ns	18	1
	Valid Delay for A_FRAME#A_STOP# A_TRDY#A_DEVSEL# A_IRDY#A_GNT# ST[2:0]	1 ns	5.5 ns	18	1
t_{fd}	Float Delay (Active to Float)	1 ns	14 ns		
t_{on}	Turn-on Delay (Float to Active)	1 ns	6 ns		

Note:

** This table contains preliminary information, which is subject to change.*

1. These signals are specified with a 10-pF load.

Table 25. AGP 2x Mode Timings*

Symbol	Parameter Description	Preliminary Data		Figure	Notes
		Min	Max		
Input Signal Requirements					
t_{RSsu}	Receive Strobe Setup Time to AGPCLK	6 ns			
t_{RSH}	Receive Strobe Hold Time from AGPCLK	1 ns			
t_{Dsu}	Data Setup Time Relative to Strobe	1 ns		20	1
t_{Dh}	Data Hold Time Relative to Strobe	1 ns		20	1
Output Signal Characteristics					
t_{TSf}	AGPCLK to Transmit Strobe Falling	2 ns	12 ns	20	
t_{TSr}	AGPCLK to Transmit Strobe Rising		20 ns	20	
t_{DVa}	Data Valid Delay after Strobe	1.9 ns		20	1
t_{DVb}	Data Valid before Strobe	1.7 ns		20	1
t_{fd}	Float Delay (Active to Float)	1 ns	12 ns	19	
t_{OFFS}	Strobe Rising Edge to Strobe Float Delay	6 ns	10 ns	19	
t_{oNd}	Turn-on Delay (Float to Active)	–1 ns	9 ns	19	

Note:

** This table contains preliminary information, which is subject to change.*

1. These signals are specified with a 10-pF load.

Table 26. AGP 4x Mode Timings*

Symbol	Parameter Description	Preliminary Data		Figure	Notes
		Min	Max		
Transmitter Output Signals					
t_{TSf}	CLK to First Transmit Strobe Transition	1.9 ns	8 ns	21	
t_{TSr}	CLK to Fourth Transmit Strobe Transition		20 ns	21	
t_{Dvb}	Data Valid Before Strobe	–0.95 ns		21	
t_{Dva}	Data Valid After Strobe	1.15 ns		21	
t_{ONd}	Float to Active Delay	–1 ns	7 ns	22	
t_{OFFd}	Active to Float Delay	1 ns	14 ns	22	
t_{ONS}	Strobe Active to First Strobe Edge Setup	4 ns	9 ns	22	
t_{OFFS}	Last Strobe Edge to Strobe Float Delay	4 ns	9 ns	22	
Receiver Input Signals					
t_{RSsu}	Receive Strobe Setup Time to CLK	6 ns			1
t_{RSh}	Receive Strobe Hold Time from CLK	0.5 ns			1
t_{Dsu}	Data to Strobe Setup Time	0.40 ns		21	
t_{Dhld}	Strobe to Data Hold Time	0.70 ns		21	

Note:
** This table contains preliminary information, which is subject to change.*
1. These specifications refer to the setup and hold times for the strobe set started in the previous cycle.

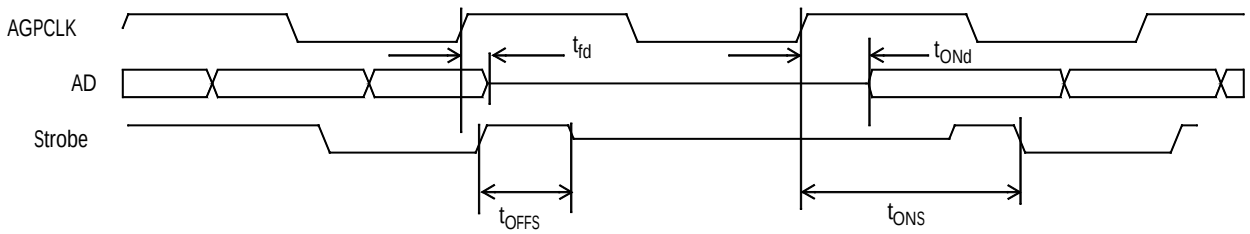


Figure 19. AGP 2x Strobe/Data Turnaround Timings

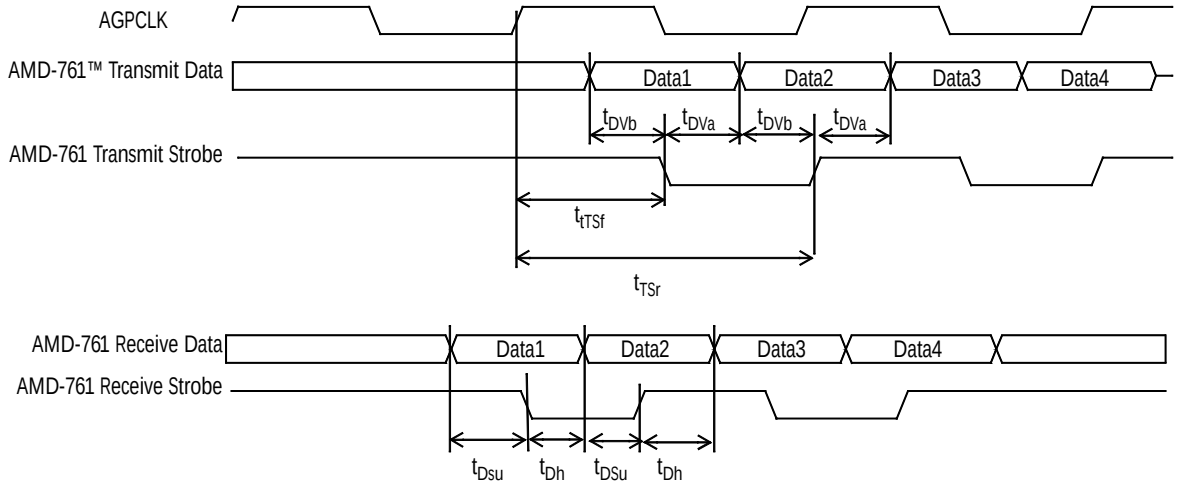


Figure 20. AGP 2x Timing Diagram

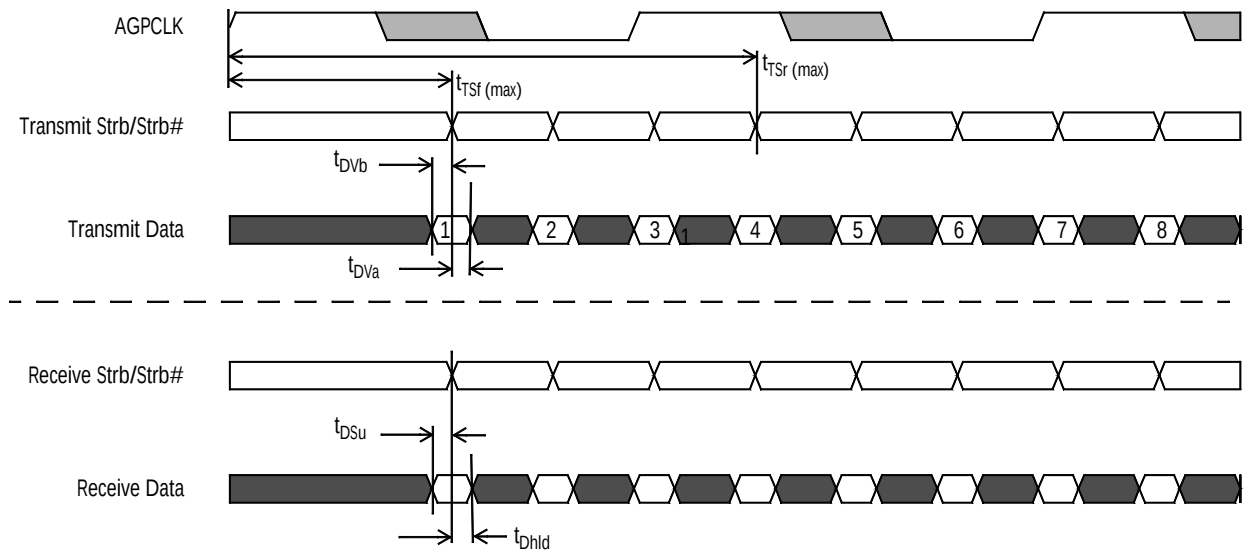


Figure 21. AGP 4x Timing Diagram

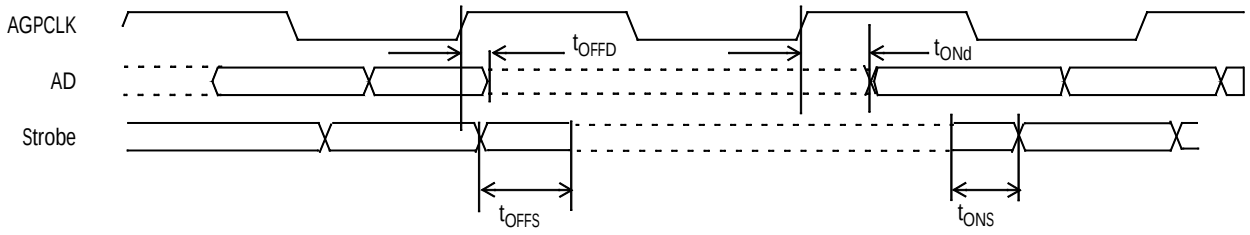


Figure 22. AGP 4x Strobe/Data Turnaround Timing

PCI Interface Timings Table 27 on page 67 shows the PCI interface timings. All of the timings are relative to PCLK.

Table 27. PCI Interface Timings*

Symbol	Parameter Description	Preliminary Data		Figure	Notes
		Min	Max		
t_{su}	AD[31:0] Setup Time	7 ns		18	
	SBREQ#, REQ[6:0]# Setup Time	12 ns		18	
	Setup Time for FRAME# STOP# TRDY# DEVSEL# IRDY# C/BE[3:0]# RESET# WSC# PAR	7 ns		18	
t_h	AD[31:0] Hold Time	0 ns		18	
	Hold Time for FRAME# STOP# TRDY# DEVSEL# IRDY# C/BE[3:0]# SBREQ# REQ[3:0]# WSC# PAR	0 ns		18	
t_{vd}	AD[31:0] Valid Delay (address phase)	2 ns	11 ns	18	1
	AD[31:0] Valid Delay (data phase)	2 ns	11 ns	18	1
	Valid Delay for FRAME# STOP# TRDY# DEVSEL# IRDY# C/BE[3:0]# GNT[3:0]# WSC# PAR	2 ns	11 ns	18	1
	SBGNT# Valid Delay	2 ns	12 ns	18	
t_{fd}	Float Delay for FRAME# STOP# TRDY# DEVSEL# IRDY# C/BE[3:0]# WSC#		28 ns		1
t_{pw}	RESET# Pulse Width	2 clks		18	

Note:

** This table contains preliminary information, which is subject to change.*

1. Measurements are taken with no load for t_{min}, and 50 pF for t_{max}.

4.5.4 AMD Athlon™ Processor System Bus Timings

Table 28 on page 68 shows the AMD Athlon system bus timings.

Table 28. AMD Athlon™ Processor System Bus/AMD-761™ System Controller AC Specification*

Group	Symbol	Parameter Description	Minimum	Nominal	Maximum	Units	Notes
Clock Forward Group Signals	$T_{NB-SKEW-SAMEEDGE}$	Output skew with respect to the same clock edge	–	–	400	ps	1
	$T_{NB-SKEW-DIFFEDGE}$	Output skew with respect to a different clock edge	–	–	1025	ps	1
	T_{NB-SU}	Input Data Setup Time	500	–	–	ps	1, 2
	T_{NB-HD}	Input Data Hold Time	800	–	–	ps	1, 2
	T_{RISE}	Signal or Clock Rise Time	1	–	3	V/ns	
	T_{FALL}	Signal or Clock Fall Time	1	–	3	V/ns	
	C_{DATA}	Data Pin Capacitance	4	–	12	pF	
	C_{INCLK}	Input Clock Capacitance	4	–	12	pF	
Sync Signals *3	$T_{NB-SYSCLK-TO-PAD}$	SYSCLK to Synchronous Signal Output at Pad (CONNECT, CLKFWDRST)	2400	–	4800	ps	4, 5
	$T_{NB-SETUP-TO-SYSCLK}$	Input Setup Time for Synchronous Signal to SYSCLK (PROCRDY)	1500	–	–	ps	4, 5
	$T_{NB-HOLD-FROM-SYSCLK}$	Input Hold Time for Synchronous Signal to SYSCLK (PROCRDY)	1200	–	–	ps	4, 5

Notes:

** This table contains preliminary information, which is subject to change.*

1. *$T_{NB-SKEW-SAMEEDGE}$ is the maximum skew within a clock-forwarded group between any two signals or between any signal and its forward clock, as measured at the package, with respect to the same clock edge.*
   $T_{NB-SKEW-DIFFEDGE}$ is the maximum skew within a clock-forwarded group between any two signals or between any signal and its forward clock, as measured at the package, with respect to different clock edges.
2. *Input SU and HLD times are with respect to the appropriate clock forward group input clock.*
3. *The synchronous signals include PROCREADY, CONNECT, and CLKFWDRST.*
4. *This value is measured with respect to the rising edge of SYSCLKIN.*
5. *Test load = 25 pF.*

5 Package Specifications

Figure 23 shows the package specifications for the AMD-761™ system controller. Tables 29, 30, and 31, starting on page 70, contain information about the symbols shown in the figures.

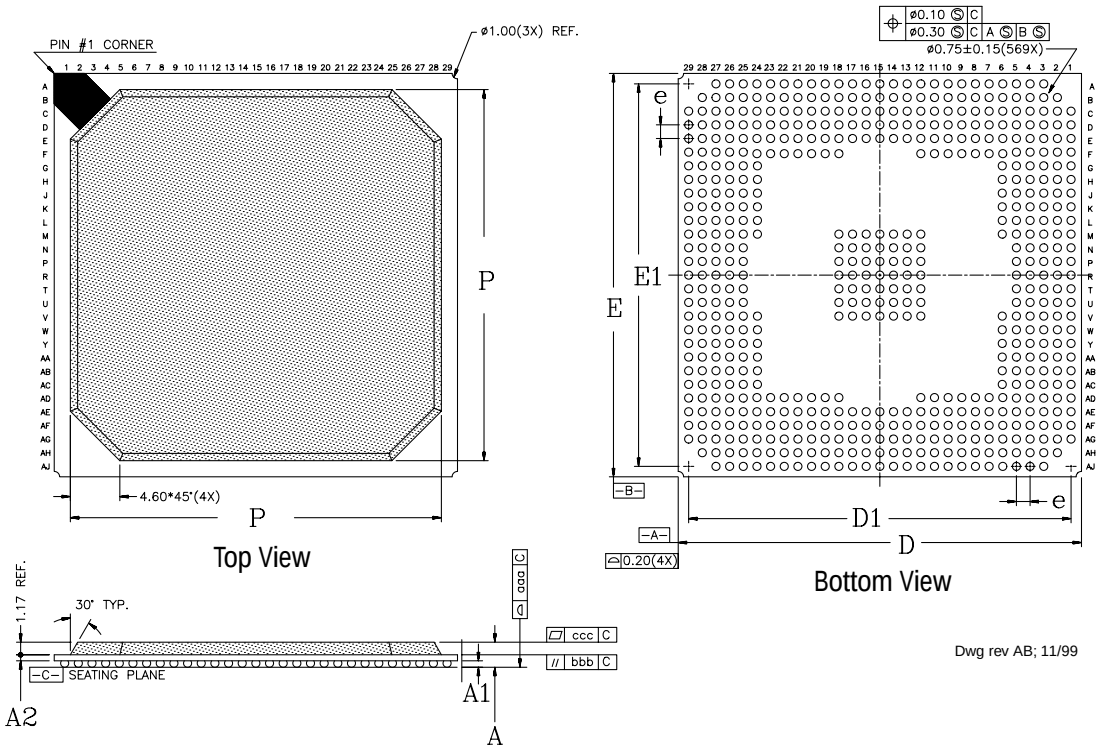


Figure 23. 569-Ball Plastic Ball Grid Array (PBGA) Package

Table 29. Symbol Notes (unless specified otherwise)

Symbol	Description
1	Dimensions and tolerances conform to ASME Y14.5M–1994.
2	All dimensions are in millimeters.
3	Dimension 'b' is measured at the maximum solder ball diameter on a plane parallel to Datum C.
4	Datum C and the seating plane are defined by the spherical crowns of the solder balls.
5	A1 corner I.D. is marked by ink.
6	Number of peripheral rows or columns.
7	Height from encapsulation to seating plane.
8	"S" is measured with respect to datums A and B and defines the position of the solder balls nearest the package centerlines. When there is an odd number of solder balls in the outer row, "S" = .000. When there is an even number of solder balls in the outer row, the value "S" = e/2.
9	Conforms to JEP–95, MO–151, Issue B, Variation BAT–1.
10	Clearance from encapsulation edge to solder ball closest point to be 0.5 mm minimum.

Table 30. 569-Pin PBGA 37.50-mm by 37.50-mm Package Specifications

Symbol	Minimum	Nominal	Maximum	Description
A	2.20	2.33	2.46	Overall thickness
A1	0.50	0.60	0.70	Ball height
A2	0.51	0.56	0.61	Body thickness
A3 7	0.20	0.30	0.45	Seating plane clearance
D	37.50 BSC.			Body size
D1	35.56 BSC.			Ball footprint
E	37.50 BSC.			Body size
E1	35.56 BSC.			Ball footprint
M	29 x 29			Ball matrix size
N	569			Total ball count
MR 6	6			Number of rows deep
b	0.60	0.75	0.90	Ball diameter
e	1.27 BSC.			Ball pitch
P	34.50 REF.			Encapsulation area
S	0.635 BSC.			Solder ball placement
S	0.635 BSC.			Solder ball placement

Table 31. Geometric Tolerances

Symbol	Tolerance	Description
aaa	0.15	Coplanarity
bbb	0.15	Parallelism
ccc	0.15	Flatness

6 Pin Designations

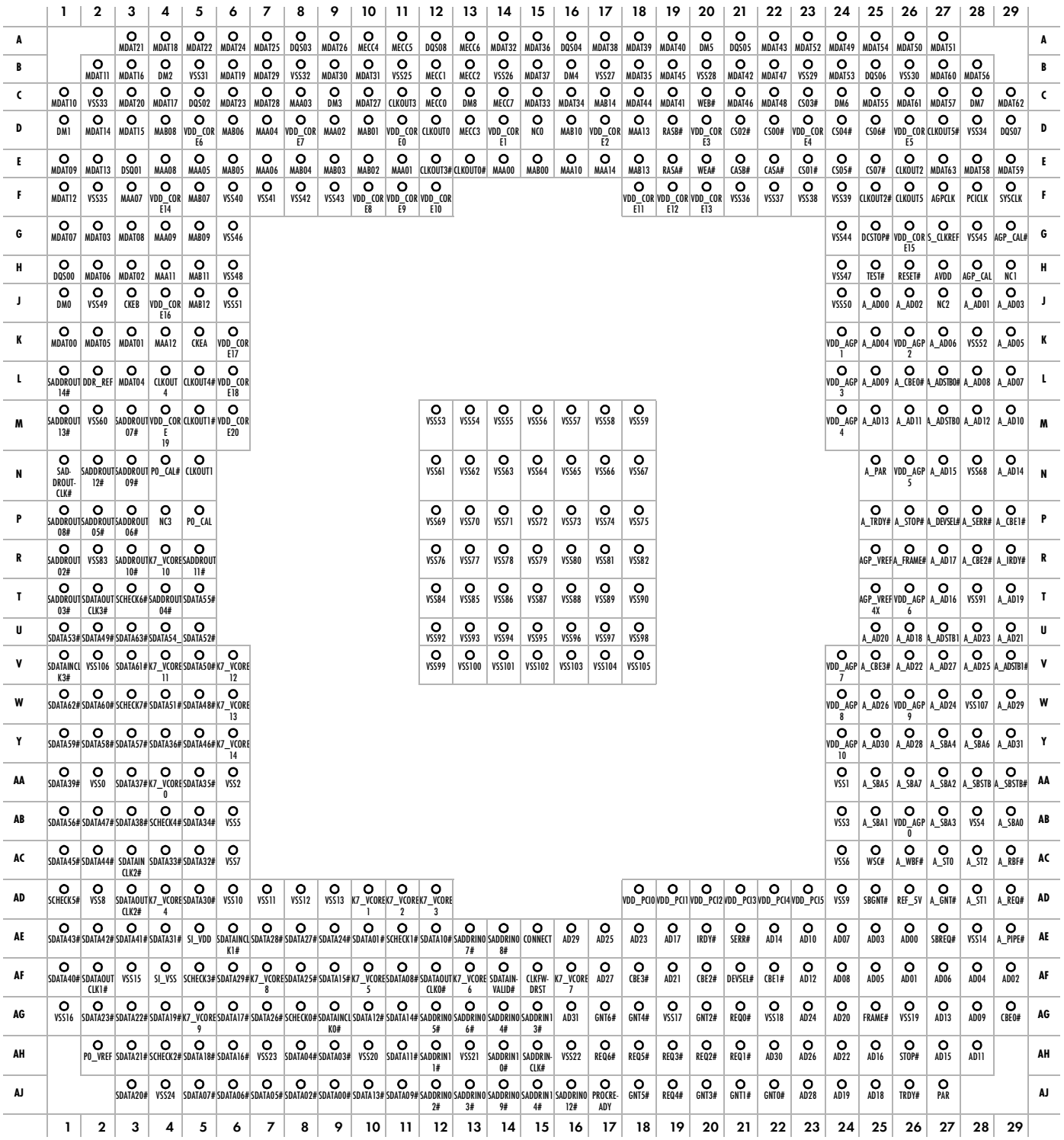


Table 32. AMD-761™ System Controller Pin Functional Grouping (1 of 3)

DDR DRAM								AGP		APCI	
Name	No.	Name	No.	Name	No.	Name	No.	Name	No.	Name	No.
MAA[14]	E-17	CS[0]#	D-22	MDAT[47]	B-22	MDAT[01]	K-3	ADSTB[1]	U-27	A_AD[31]	Y-29
MAA[13]	D-18	RASB#	D-19	MDAT[46]	C-21	MDAT[00]	K-1	ADSTB[1]#	V-29	A_AD[30]	Y-25
MAA[12]	K-4	RASA#	E-19	MDAT[45]	B-19	MECC[7]	C-14	ADSTB[0]	M-27	A_AD[29]	W-29
MAA[11]	H-4	CASB#	E-21	MDAT[44]	C-18	MECC[6]	A-13	ADSTB[0]#	L-27	A_AD[28]	Y-26
MAA[10]	E-16	CASA#	E-22	MDAT[43]	A-22	MECC[5]	A-11	SBSTB	AA-28	A_AD[27]	V-27
MAA[09]	G-4	WEB#	C-20	MDAT[42]	B-21	MECC[4]	A-10	SBSTB#	AA-29	A_AD[26]	W-25
MAA[08]	E-4	WEA#	E-20	MDAT[41]	C-19	MECC[3]	D-13	WBF#	AC-26	A_AD[25]	V-28
MAA[07]	F-3	CKEB	J-3	MDAT[40]	A-19	MECC[2]	B-13	PIPE#	AE-29	A_AD[24]	W-27
MAA[06]	E-7	CKEA	K-5	MDAT[39]	A-18	MECC[1]	B-12	RBF#	AC-29	A_AD[23]	U-28
MAA[05]	E-5	DQS[8]	A-12	MDAT[38]	A-17	MECC[0]	C-12	SBA[0]	AB-29	A_AD[22]	V-26
MAA[04]	D-7	DQS[7]	D-29	MDAT[37]	B-15			SBA[1]	AB-25	A_AD[21]	U-29
MAA[03]	C-8	DQS[6]	B-25	MDAT[36]	A-15			SBA[2]	AA-27	A_AD[20]	U-25
MAA[02]	D-9	DQS[5]	A-21	MDAT[35]	B-18			SBA[3]	AB-27	A_AD[19]	T-29
MAA[01]	E-11	DQS[4]	A-16	MDAT[34]	C-16			SBA[4]	Y-27	A_AD[18]	U-26
MAA[00]	E-14	DQS[3]	A-8	MDAT[33]	C-15			SBA[5]	AA-25	A_AD[17]	R-27
MAB[14]	C-17	DQS[2]	C-5	MDAT[32]	A-14			SBA[6]	Y-28	A_AD[16]	T-27
MAB[13]	E-18	DQS[1]	E-3	MDAT[31]	B-10			SBA[7]	AA-26	A_AD[15]	N-27
MAB[12]	J-5	DQS[0]	H-1	MDAT[30]	B-9			ST[0]	AC-27	A_AD[14]	N-29
MAB[11]	H-5	CLKOUT[5]	F-26	MDAT[29]	B-7			ST[1]	AD-28	A_AD[13]	M-25
MAB[10]	D-16	CLKOUT[5]#	D-27	MDAT[28]	C-7			ST[2]	AC-28	A_AD[12]	M-28
MAB[09]	G-5	CLKOUT[4]	L-4	MDAT[27]	C-10			AGPCLK	F-27	A_AD[11]	M-26
MAB[08]	D-4	CLKOUT[4]#	L-5	MDAT[26]	A-9					A_AD[10]	M-29
MAB[07]	F-5	CLKOUT[3]	C-11	MDAT[25]	A-7					A_AD[09]	L-25
MAB[06]	D-6	CLKOUT[3]#	E-12	MDAT[24]	A-6					A_AD[08]	L-28
MAB[05]	E-6	CLKOUT[2]	E-26	MDAT[23]	C-6					A_AD[07]	L-29
MAB[04]	E-8	CLKOUT[2]#	F-25	MDAT[22]	A-5					A_AD[06]	K-27
MAB[03]	E-9	CLKOUT[1]	N-5	MDAT[21]	A-3					A_AD[05]	K-29
MAB[02]	E-10	CLKOUT[1]#	M-5	MDAT[20]	C-3					A_AD[04]	K-25
MAB[01]	D-10	CLKOUT[0]	D-12	MDAT[19]	B-6					A_AD[03]	J-29
MAB[00]	E-15	CLKOUT[0]#	E-13	MDAT[18]	A-4					A_AD[02]	J-26
DM[8]	C-13	MDAT[63]	E-27	MDAT[17]	C-4					A_AD[01]	J-28
DM[7]	C-28	MDAT[62]	C-29	MDAT[16]	B-3					A_AD[00]	J-25
DM[6]	C-24	MDAT[61]	C-26	MDAT[15]	D-3					A_CBE[3]#	V-25
DM[5]	A-20	MDAT[60]	B-27	MDAT[14]	D-2					A_CBE[2]#	R-28
DM[4]	B-16	MDAT[59]	E-29	MDAT[13]	E-2					A_CBE[1]#	P-29
DM[3]	C-9	MDAT[58]	E-28	MDAT[12]	F-1					A_CBE[0]#	L-26
DM[2]	B-4	MDAT[57]	C-27	MDAT[11]	B-2					A_DEVSEL#	P-27
DM[1]	D-1	MDAT[56]	B-28	MDAT[10]	C-1					A_FRAME#	R-26
DM[0]	J-1	MDAT[55]	C-25	MDAT[09]	E-1					A_GNT#	AD-27
CS[7]#	E-25	MDAT[54]	A-25	MDAT[08]	G-3					A_IRDY#	R-29
CS[6]#	D-25	MDAT[53]	B-24	MDAT[07]	G-1					A_PAR	N-25
CS[5]#	E-24	MDAT[52]	A-23	MDAT[06]	H-2					A_REQ#	AD-29
CS[4]#	D-24	MDAT[51]	A-27	MDAT[05]	K-2					A_SERR#	P-28
CS[3]#	C-23	MDAT[50]	A-26	MDAT[04]	L-3					A_STOP#	P-26
CS[2]#	D-21	MDAT[49]	A-24	MDAT[03]	G-2					A_TRDY#	P-25
CS[1]#	E-23	MDAT[48]	C-22	MDAT[02]	H-3						

Table 33. AMD-761™ System Controller Pin Functional Grouping (2 of 3)

PCI Bus				AMD Athlon System Bus					
Name	**No.**	**Name**	**No.**	**Name**	**No.**	**Name**	**No.**	**Name**	**No.**
AD[31]	AG-16	REQ[1]#	AH-21	CLKFWDRST	AF-15	SDATA[06]#	AJ-6	SDATA[52]#	U-5
AD[30]	AH-22	REQ[2]#	AH-20	CONNECT	AE-15	SDATA[07]#	AJ-5	SDATA[53]#	U-1
AD[29]	AE-16	REQ[3]#	AH-19	PROCRDY	AJ-17	SDATA[08]#	AF-11	SDATA[54]#	U-4
AD[28]	AJ-23	REQ[4]#	AJ-19	SYSCLK	F-29	SDATA[09]#	AJ-11	SDATA[55]#	T-5
AD[27]	AF-17	REQ[5]#	AH-18	SADDIN[02]#	AJ-12	SDATA[10]#	AE-12	SDATA[56]#	AB-1
AD[26]	AH-23	REQ[6]#	AH-17	SADDIN[03]#	AJ-13	SDATA[11]#	AH-11	SDATA[57]#	Y-3
AD[25]	AE-17	GNT[0]#	AJ-22	SADDIN[04]#	AG-14	SDATA[12]#	AG-10	SDATA[58]#	Y-2
AD[24]	AG-23	GNT[1]#	AJ-21	SADDIN[05]#	AG-12	SDATA[13]#	AJ-10	SDATA[59]#	Y-1
AD[23]	AE-18	GNT[2]#	AG-20	SADDIN[06]#	AG-13	SDATA[14]#	AG-11	SDATA[60]#	W-2
AD[22]	AH-24	GNT[3]#	AJ-20	SADDIN[07]#	AE-13	SDATA[15]#	AF-9	SDATA[61]#	V-3
AD[21]	AF-19	GNT[4]#	AG-18	SADDIN[08]#	AE-14	SDATA[16]#	AH-6	SDATA[62]#	W-1
AD[20]	AG-24	GNT[5]#	AJ-18	SADDIN[09]#	AJ-14	SDATA[17]#	AG-6	SDATA[63]#	U-3
AD[19]	AJ-24	GNT[6]#	AG-17	SADDIN[10]#	AH-14	SDATA[18]#	AH-5	SDATAINCLK[0]#	AG-9
AD[18]	AJ-25	SBREQ#	AE-27	SADDIN[11]#	AH-12	SDATA[19]#	AG-4	SDATAINCLK[1]#	AE-6
AD[17]	AE-19	SBGNT#	AD-25	SADDIN[12]#	AJ-16	SDATA[20]#	AJ-3	SDATAINCLK[2]#	AC-3
AD[16]	AH-25	RESET#	H-26	SADDIN[13]#	AG-15	SDATA[21]#	AH-3	SDATAINCLK[3]#	V-1
AD[15]	AH-27			SADDIN[14]#	AJ-15	SDATA[22]#	AG-3	SDATAINVALID#	AF-14
AD[14]	AE-22			SADDINCLK#	AH-15	SDATA[23]#	AG-2	SDATAOUTCLK[0]#	AF-12
AD[13]	AG-27			SADDOUT[02]#	R-1	SDATA[24]#	AE-9	SDATAOUTCLK[1]#	AF-2
AD[12]	AF-23			SADDOUT[03]#	T-1	SDATA[25]#	AF-8	SDATAOUTCLK[2]#	AD-3
AD[11]	AH-28			SADDOUT[04]#	T-4	SDATA[26]#	AG-7	SDATAOUTCLK[3]#	T-2
AD[10]	AE-23			SADDOUT[05]#	P-2	SDATA[27]#	AE-8		
AD[09]	AG-28			SADDOUT[06]#	P-3	SDATA[28]#	AE-7		
AD[08]	AF-24			SADDOUT[07]#	M-3	SDATA[29]#	AF-6		
AD[07]	AE-24			SADDOUT[08]#	P-1	SDATA[30]#	AD-5		
AD[06]	AF-27			SADDOUT[09]#	N-3	SDATA[31]#	AE-4		
AD[05]	AF-25			SADDOUT[10]#	R-3	SDATA[32]#	AC-5		
AD[04]	AF-28			SADDOUT[11]#	R-5	SDATA[33]#	AC-4		
AD[03]	AE-25			SADDOUT[12]#	N-2	SDATA[34]#	AB-5		
AD[02]	AF-29			SADDOUT[13]#	M-1	SDATA[35]#	AA-5		
AD[01]	AF-26			SADDOUT[14]#	L-1	SDATA[36]#	Y-4		
AD[00]	AE-26			SADDOUTCLK#	N-1	SDATA[37]#	AA-3		
CBE[3]#	AF-18			SCHECK[0]#	AG-8	SDATA[38]#	AB-3		
CBE[2]#	AF-20			SCHECK[1]#	AE-11	SDATA[39]#	AA-1		
CBE[1]#	AF-22			SCHECK[2]#	AH-4	SDATA[40]#	AF-1		
CBE[0]#	AG-29			SCHECK[3]#	AF-5	SDATA[41]#	AE-3		
PCICLK	F-28			SCHECK[4]#	AB-4	SDATA[42]#	AE-2		
DEVSEL#	AF-21			SCHECK[5]#	AD-1	SDATA[43]#	AE-1		
FRAME#	AG-25			SCHECK[6]#	T-3	SDATA[44]#	AC-2		
WSC#	AC-25			SCHECK[7]#	W-3	SDATA[45]#	AC-1		
IRDY#	AE-20			SDATA[00]#	AJ-9	SDATA[46]#	Y-5		
PAR	AJ-27			SDATA[01]#	AE-10	SDATA[47]#	AB-2		
SERR#	AE-21			SDATA[02]#	AJ-8	SDATA[48]#	W-5		
STOP#	AH-26			SDATA[03]#	AH-9	SDATA[49]#	U-2		
TRDY#	AJ-26			SDATA[04]#	AH-8	SDATA[50]#	V-5		
REQ[0]#	AG-21			SDATA[05]#	AJ-7	SDATA[51]#	W-4		

Table 34. AMD-761™ System Controller Pin Functional Grouping (3 of 3)

Miscellaneous		VDD		VSS					
Name	No.	Name	No.	Name	No	Name	No.	Name	No.
S_CLKREF	G-27	VDD_CORE	D-5	VSS	B-5	VSS	P-14	VSS	AD-6
DCSTOP#	G-25	VDD_CORE	D-8	VSS	B-8	VSS	P-15	VSS	AD-7
K7_VCORE0	R-4	VDD_CORE	D-11	VSS	B-11	VSS	P-16	VSS	AD-8
K7_VCORE1	V-4	VDD_CORE	D-14	VSS	B-14	VSS	P-17	VSS	AD-9
K7_VCORE2	V-6	VDD_CORE	D-17	VSS	B-17	VSS	P-18	VSS	AD-24
K7_VCORE3	W-6	VDD_CORE	D-20	VSS	B-20	VSS	R-2	VSS	AE-28
K7_VCORE4	Y-6	VDD_CORE	D-23	VSS	B-23	VSS	R-12	VSS	AF-3
K7_VCORE5	AA-4	VDD_CORE	D-26	VSS	B-26	VSS	R-13	VSS	AG-1
K7_VCORE6	AD-4	VDD_CORE	F-4	VSS	C-2	VSS	R-14	VSS	AG-19
K7_VCORE7	AD-10	VDD_CORE	F-10	VSS	D-28	VSS	R-15	VSS	AG-22
K7_VCORE8	AD-11	VDD_CORE	F-11	VSS	F-2	VSS	R-16	VSS	AG-26
K7_VCORE9	AD-12	VDD_CORE	F-12	VSS	F-6	VSS	R-17	VSS	AH-7
K7_VCORE10	AF-7	VDD_CORE	F-18	VSS	F-7	VSS	R-18	VSS	AH-10
K7_VCORE11	AF-10	VDD_CORE	F-19	VSS	F-8	VSS	T-12	VSS	AH-13
K7_VCORE12	AF-13	VDD_CORE	F-20	VSS	F-9	VSS	T-13	VSS	AH-16
K7_VCORE13	AF-16	VDD_CORE	G-26	VSS	F-21	VSS	T-14	VSS	AJ-4
K7_VCORE14	AG-5	VDD_CORE	J-4	VSS	F-22	VSS	T-15		
P0_VREF	AH-2	VDD_CORE	K-6	VSS	F-23	VSS	T-16		
P0_CAL	P-5	VDD_CORE	L-6	VSS	F-24	VSS	T-17		
P0_CAL#	N-4	VDD_CORE	M-4	VSS	G-6	VSS	T-18		
SI_VSS	AF-4	VDD_CORE	M-6	VSS	G-24	VSS	T-28		
SI_VDD	AE-5	VDD_AGP	K-24	VSS	G-28	VSS	U-12		
AGP_VREF	R-25	VDD_AGP	K-26	VSS	H-6	VSS	U-13		
AGP_VREF4X	T-25	VDD_AGP	L-24	VSS	H-24	VSS	U-14		
AGP_CAL	H-28	VDD_AGP	M-24	VSS	J-2	VSS	U-15		
AGP_CAL#	G-29	VDD_AGP	N-26	VSS	J-6	VSS	U-16		
REF_5V	AD-26	VDD_AGP	T-26	VSS	J-24	VSS	U-17		
DDR_REF	L-2	VDD_AGP	V-24	VSS	K-28	VSS	U-18		
TEST#	H-25	VDD_AGP	W-24	VSS	M-2	VSS	V-2		
SPARE1	D-15	VDD_AGP	W-26	VSS	M-12	VSS	V-12		
SPARE2	P-4	VDD_AGP	Y-24	VSS	M-13	VSS	V-13		
SPARE3	H-29	VDD_AGP	AB-26	VSS	M-14	VSS	V-14		
SPARE4	J-27	VDD_PCI	AD-18	VSS	M-15	VSS	V-15		
		VDD_PCI	AD-19	VSS	M-16	VSS	V-16		
		VDD_PCI	AD-20	VSS	M-17	VSS	V-17		
		VDD_PCI	AD-21	VSS	M-18	VSS	V-18		
		VDD_PCI	AD-22	VSS	N-12	VSS	W-28		
		VDD_PCI	AD-23	VSS	N-13	VSS	AA-2		
		A_VDD	H-27	VSS	N-14	VSS	AA-6		
				VSS	N-15	VSS	AA-24		
				VSS	N-16	VSS	AB-6		
				VSS	N-17	VSS	AB-24		
				VSS	N-18	VSS	AB-28		
				VSS	N-28	VSS	AC-6		
				VSS	P-12	VSS	AC-24		
				VSS	P-13	VSS	AD-2		

7 Signal Descriptions

Table 35 describes the terms used in the signal description table. The signals are organized within the following functional groups:

- Processor interface signals (page 78)
- PCI interface signals (page 80)
- DRAM interface signals (page 82)
- AGP/PCI signals (page 85)
- AGP-only signals (page 86)
- Initialization pinstrapping (page 88)
- Miscellaneous signals (page 87)
- Pin multiplexing options (page 92)

Table 35. Signal Descriptions Table Definitions

Signal Types	
B	Bidirectional
I	Input
O	Output
STS	Sustained three-state
TS	Three-state

Table 36 on page 78 contains a description of the AMD-761™ system controller signals.

Table 36. Signal Descriptions

Signal	Type	Description
Processor Interface Signals		
CLKFWDRST	O	**AMD Athlon™ System Bus Clock Forward Reset** CLKFWDRST resets the source-synchronous clock circuitry for the processor. Forwarded clocks are driven continuously beginning three clocks after CLKFWDRST is negated. This signal is negated by RESET#. It changes on the rising edge of SYSCLK.
CONNECT	O	**AMD Athlon System Bus Connect** CONNECT is an output from the AMD-761™ system controller and is used for power management and source-synchronous clock initialization at reset. This signal is negated by RESET#. It changes on the rising edge of SYSCLK.
PROCRDY	I	**AMD Athlon System Bus Processor Ready** PROCRDY is an input to the AMD-761 system controller and is used for power management and source-synchronous clock initialization at reset. This signal is sampled on the rising edge of SYSCLK.
SADDIN[14:2]#	O	**AMD Athlon System Bus Address/Command** The SADDIN[14:2]# is a unidirectional system command bus to the processor. It is used to transfer probe and data movement commands into the processor. SADDIN[14:2]# are skew-aligned with the source-synchronous clock, SADDINCLK#. The AMD-761 system controller drives the SADDIN[14:2]# channel on each edge of SADDINCLK#.
SADDINCLK#	O	**AMD Athlon System Bus System Address In Clock** SADDINCLK# is the single-ended source-synchronous clock for the SADDIN[14:2]# bus, driven by the AMD-761 system controller. Each clock edge is used to transfer probe and data movement commands to the processor. This signal is driven inactive (negated) when the CLKFWDRST signal is asserted (true). When CLKFWDRST is negated, SADDINCLK# runs continuously after a three clock delay.
SADDOUT[14:2]#	I	**AMD Athlon System Bus System Address Out** The SADDOUT[14:2]# is a unidirectional system address interface from the processor to the AMD-761 system controller. The SADDOUT[14:2]# channel is used to transfer processor requests and probe responses to the system. This channel is skew-aligned with the source-synchronous clock, SADDOUTCLK#. The SADDOUT[14:2]# channel is sampled by the AMD-761 system controller on each edge of SADDOUTCLK#. The AMD-761 system controller samples commands driven by the processor on the SADDOUT[14:2]# channel and forwards them to the PCI bus, AGP bus, or DRAM, depending on the address range and AMD-761 configuration.
SADDOUTCLK#	I	**AMD Athlon System Bus System Address Out Clock** SADDOUTCLK# is a single-ended source synchronous clock for the SADDOUT[14:2]# channel driven by the processor. Each edge is used to transfer commands. This signal is driven inactive (negated) when the CLKFWDRST signal is asserted (true). When CLKFWDRST is negated, SADDOUTCLK# runs continuously after a three-clock delay.

Table 36. Signal Descriptions (Continued)

Signal	Type	Description
SCHECK[7:0]#	B	**AMD Athlon™ System Bus Data Bus Check Byte** SCHECK[7:0]# transfer ECC check bits for data transferred on the SDATA[63:0]# bus. *As Outputs:* The AMD-761 system controller drives SCHECK[7:0]# with each valid data quadword. SCHECK[7:0]# are skew-aligned with the source-synchronous clocks, SDATAINCLK[3:0]#. *As Inputs:* The AMD-761 system controller samples SCHECK[7:0]# and transfers the data to the memory. The SCHECK[7:0]# is sampled by the AMD-761 system controller on each edge of SDATAOUTCLK[3:0]#. SCHECK[7:0]# are floated by RESET#. Check bits for write data are driven by the processor and check bits for read data are driven by the system controller. The AMD-761 system controller drives the previous data value between transfers to prevent floating inputs.
SDATA[63:0]#	B	**AMD Athlon System Bus Processor Data Channel** The SDATA[63:0]# transfer data between the processor and system. *As Outputs:* The AMD-761 system controller drives SDATA[63:0]# with each valid data quadword. SDATA[63:0]# are skew-aligned with the source-synchronous clocks, SDATAINCLK[3:0]#. *As Inputs:* The AMD-761 system controller samples SDATA[63:0]# and transfers the data to the memory. The SDATA[63:0]# is sampled by the AMD-761 system controller on each edge of SDATAOUTCLK[3:0]#. SDATA[63:0]# is floated out of RESET#. Write data is driven by the processor and read data is driven by the system controller. The AMD-761 system controller drives the previous data value between transfers to prevent floating inputs.
SDATAINCLK[3:0]#	O	**AMD Athlon System Bus System Data In Clock** SDATAINCLK[3:0]# is the single-ended source-synchronous clock driven by the AMD-761 system controller to transfer data on SDATA[63:0]# and check bits on SCHECK[7:0]#. Sixteen bits of data and two check bits are skew-aligned with each clock. Data is transferred on each clock edge. These signals are driven inactive (negated) when the CLKFWDRST signal is asserted (true). When CLKFWDRST is negated, SDATAINCLK[3:0]# run continuously after three clock delays.
SDATAINVAL#	O	**AMD Athlon System Bus System Data In Valid** SDATAINVAL# is driven by the AMD-761 system controller and controls the flow of data into the processor. SDATAINVAL# can be used to introduce an arbitrary number of cycles between quadword pairs (128 bits). SDATAINVAL# is skew-aligned with the source-synchronous clock, SADDINCLK#.
SDATAOUTCLK[3:0]#	I	**AMD Athlon System Bus System Address Out Clock** SDATAOUTCLK[3:0]# is the single-ended source-synchronous clock driven by the processor and is used to transfer data and check bits on the SDATA[63:0]# and SCHECK[7:0]#. Sixteen bits of data and two check bits are skew-aligned with each clock. Data is transferred on each clock edge. These signals are driven inactive (negated) when the CLKFWDRST signal is asserted (true). When CLKFWDRST is negated, SDATAOUTCLK[3:0]# run continuously after three clock delays.

Table 36. Signal Descriptions (Continued)

Signal	Type	Description
SYSCLK	I	**AMD Athlon™ System Bus System Clock** SYSCLK is a single-ended input clock signal provided by the system clock generator to the phase locked loop (PLL) of the AMD-761 system controller. Frequencies of 66.67 MHz, 100.00 MHz, or 133.33 MHz are supported.
		PCI Interface Signals
AD[31:00]	B *TS*	**PCI Address/Data Bus** This is the multiplexed address/data bus, sampled on the rising edge of PCICLK. The address is valid on AD[31:00] during the first clock when FRAME# is asserted. Write data is valid on AD[31:00] when IRDY# is asserted and read data is valid when TRDY# is asserted. Data transfers occur on AD[31:00] when both IRDY# and TRDY# are asserted. These pins are also used for initialization pinstrapping to configure various startup parameters of the AMD-761 system controller. The initialization pinstraps are configured with a weak pullup or pulldown and sampled by the AMD-761 system controller during system reset. Refer to Section 7.1 on page 88 for further details.
C/BE[3:0]#	B *TS*	**PCI Command/Byte Enables** During the address phase, these pins define the PCI command. During the data phase these pins are used as byte enables. These pins are also used for initialization pinstrapping to configure various startup parameters of the AMD-761 system controller. The initialization pinstraps are configured with a weak pullup or pulldown and sampled by the AMD-761 system controller during system reset. Refer to Section 7.1 on page 88 for further details. C/BE[1:0]# are also optionally used for connecting an external serial initialization packet (SIP) ROM for processor initialization. This feature is typically used only for test and debug modes.
DEVSEL#	B *STS*	**PCI Device Select** The AMD-761 system controller asserts this pin when an external bus master drives a valid address within the AMD-761 system controller's memory region, as defined by the PCI Top of Memory register (Dev 0:F0:0x9C). The AMD-761 system controller responds only to memory cycles. This pin is sampled by the AMD-761 system controller when the CPU accesses a PCI target.
FRAME#	B *STS*	**PCI Cycle Frame** The FRAME# pin is asserted by the AMD-761 system controller to indicate the beginning of a bus transaction. FRAME# is sampled by the AMD-761 PCI target controller when an external bus master is performing a transaction on the PCI bus.
GNT[6:0]#	O *TS*	**PCI Bus Grant** As the PCI bus arbiter, the AMD-761 system controller asserts one of these device-specific bus grant signals off the rising clock edge to indicate to an initiator that it has been granted control of the PCI bus the next time the bus is idle. GNT[6:0]# signals are never floated. They are negated off the rising edge of the PCICLK input, indicating that no device has been granted the bus. One of the GNT[6:0]# signals is asserted off the rising edge of the clock, indicating the particular channel that is granted use of the bus. These pins are also optionally used in test modes as described in Table 38 on page 92, and in Chapter 3.

Table 36. Signal Descriptions (Continued)

Signal	Type	Description
IRDY#	B *STS*	**PCI Initiator Ready** The AMD-761™ system controller asserts this signal during PCI transactions to indicate that write data is valid or it is ready to receive read data. It is sampled by the AMD-761 system controller during memory transactions by external bus masters to DRAM. This pin is also optionally used in test modes as described in Table 38 on page 92, and in Chapter 3.
PAR	B *TS*	**PCI Bus Parity** PAR is used to generate and check for even parity across the AD[31:0] and C/BE[3:0]# pins. The AMD-761 system controller generates but does not check parity. This pin is also optionally used in test modes as described in Table 38 on page 92, and in Chapter 3.
PCICLK	I	**PCI Clock** PCICLK is a 33.33-MHz clock provided by the system clock generator. It is used by the AMD-761 system controller logic in the PCI clock domain.
SBGNT#	O *TS*	**PCI Grant to Peripheral Bus Controller** SBGNT# grants control of the PCI bus to the PCI-ISA/IDE bridge functions implemented in the AMD-766™ peripheral bus controller. SBGNT# is driven off the rising edge of PCICLK. RESET# forces SBGNT# inactive. SBGNT# is asserted in response to a SBREQ#. SBGNT# and GNT[6:0]# all grant control of the bus to an external device. Only one is asserted at any time.
SBREQ#	I	**PCI Request from Peripheral Bus Controller** The AMD-761 system controller samples SBREQ# to determine if the AMD-766 peripheral bus controller needs PCI bus access. This signal is sampled by the rising edge of every PCICLK. If asserted, the arbiter issues a SBGNT# when the bus is available.
REQ[6:0]#	I	**PCI Bus Request** As the PCI bus arbiter, the AMD-761 system controller samples these device-specific bus request signals to determine if another agent requires control of the PCI bus. These signals are sampled by the rising edge of every PCICLK. If active, the arbiter issues the corresponding GNT[6:0]# when the bus is available.
RESET#	I	**System Reset** Asserting RESET# resets the AMD-761 system controller and sets all register bits to their default values (except memory controller registers as required for ACPI S3 support). Bidirectional signals are three-stated and outputs are driven inactive. RESET# is driven by the PCIRST# output of the AMD-766 peripheral bus controller. See “Pin States at Reset” on page 92. This signal may be asynchronous to SYSCLK and PCICLK. It is synchronized internally, therefore it must be active for a minimum of four PCICLK periods.
SERR#	O *OD*	**PCI System Error** SERR# is used by the AMD-761 system controller to transfer GART errors, ECC errors, or AGP A_SERR# pin assertion errors to error reporting logic on the AMD-766 peripheral bus controller.

Table 36. Signal Descriptions (Continued)

Signal	Type	Description
STOP#	B *STS*	**PCI Stop** As a target, the STOP# signal is asserted by the AMD-761™ system controller PCI target logic to initiate a target disconnect, ending the current transfer. As a master, the AMD-761 system controller ends the current transfer when it samples the STOP# signal asserted.
TRDY#	B *STS*	**PCI Target Ready** TRDY# is asserted by the AMD-761 system controller during accesses of DRAM by an external bus master when read data is valid or when the target logic is ready to receive write data. This signal is sampled by the AMD-761 PCI master logic when the AMD-761 system controller is accessing an external PCI target. This pin is also optionally used in test modes as described in Table 38 on page 92, and in Chapter 3.
WSC#	B *TS*	**PCI Write Snoop Complete** WSC# is asserted to indicate that all snoop activity on the processor bus on behalf of the last PCI-to-DRAM write transaction has completed. It indicates that an APIC interrupt message can be sent by the Southbridge. This signal is required only in configurations where an I/O APIC is installed. The WSC# pin is driven and sampled by the AMD-761 system controller on the rising edge of PCICLK. The AMD-761 system controller supports a bidirectional WSC# configuration by default for connection to Southbridges that drive a request on the WSC# pin as well as receive an acknowledge on the WSC# pin. On silicon revisions B4 and above, the AMD-761 system controller also supports a unidirectional WSC# mode for Southbridges that do not drive the WSC# pin. Refer to Chapter 2 on page 7 for details of WSC# operation.
DDR DRAM Interface Signals ***Note:*** *DDR outputs are SSTL-2 compatible.*		
CS[7:0]#	O	**DDR DIMM Chip Selects** CS[7:0]# function as chip-select signals for the DDR DRAMs. These signals are negated by RESET#. The memory controller asserts or negates these signals relative to CLKOUT at the appropriate time in the memory access sequence. CS[7:0]# are driven a quarter of a cycle off from the CLKOUT rising edge to provide additional HOLD time. See Chapter 2, “Functional Operation” starting on page 7 for more information.
DM[8:0]	B	**DDR Data Masks/Data Strobes (for x4 DIMMs only)** DM[8:0] provides data masks for each byte during DDR writes to x8 and x16 DIMMs only. For x4 DIMMs, these pins are used to provide the additional DQS pins required in x4 DIMM configurations. DM signals are not provided by x4 DIMMs. In the absence of the DM function, partial writes result in full-line read-modify-write cycles with all bytes being written active on the DIMM. These control signals are three-stated by RESET# and remain three-stated until driven by the AMD-761 system controller during writes or by the DDR DRAM during reads. During DDR writes to x8 and x16 DIMMs, the memory controller asserts or negates these signals relative to the DQS[8:0] clock signals (described below). For x4 DIMMs, these pins function as additional DQS strobe signals. See Chapter 2, “Functional Operation” starting on page 7 for more information.

Table 36. Signal Descriptions (Continued)

Signal	Type	Description
DQS[8:0]	B	**DDR Data Strobes** DQS[8:0] are bidirectional data strobes between the memory devices and the memory controller that are used to capture data. The data strobes (DQS signals) are source-synchronous, which means that the DQS signals are driven by the device that is driving the data. The source-synchronous strobe scheme is also referred to as the clock-forwarded scheme. The AMD-761 system controller provides one DQS signal per byte of data for x8 and x16 DIMMs or one DQS signal per nibble of x4 DIMMs. During a x4 DIMM access, the DM pins provide the additional DQS strobe signals, which function the same as the DQS strobe signals. An access to a x4 DIMM requires 18 data strobes (including ECC), which are the DQS[8:0] and DM[8:0] pins combined. The AMD-761 system controller implements a DQS scheme on the DDR interface that is similar to the clock-forwarded scheme used on the AMD Athlon system bus interface.
MAA[14:0] and MAB[14:0]	O	**DDR Memory Address** The multiplexed row and column address bits MAA[14:0] and MAB[14:0] connect to the system DDR SDRAMs. Two sets of memory addresses are provided to reduce signal loading for motherboard designs with more than one DIMM slot. In an effort to reduce switching noise on the DDR interface, the MAB bus is an inverted copy of the MAA bus, with the exception of the MA[10] bit that remains un-inverted on the MAB bus. The MAB bus is **not** inverted from the MAA bus during the DDR device initialization phase. The memory controller asserts or de-asserts these signals relative to CLKOUT at the appropriate time in the memory access sequence. MAA[14:0] and MAB[14:0] are driven a quarter of a cycle off from the CLKOUT rising edge to provide additional HOLD time. See Chapter 2, “Functional Operation” starting on page 7 for more information.
CKEA and CKEB	O	**DDR Clock Enables** CKEA and CKEB are clock enable signals for the DDR DRAMs and are used for power saving modes. They operate in parallel to drive greater loads than a single signal can support. These control signals are driven inactive (negated) by RESET# or when the DDR devices are placed in self refresh mode. The memory controller asserts or de-asserts these signals relative to CLKOUT at the appropriate time in the memory access sequence. CKEA and CKEB are driven a quarter of a cycle off from the CLKOUT rising edge to provide additional HOLD time. See Chapter 2, “Functional Operation” starting on page 7 for more information.
MDAT[63:0]	B	**DDR Memory Data** MDAT[63:0] connect to the DRAM data I/O. They are driven by the DDR DRAM during reads and are driven by the AMD-761 system controller during writes. During writes, the AMD-761 system controller provides the clock-forwarded DQS[8:0] strobes centered within the write data. The DQS strobes are used to capture the write data at the DDR DRAMs. (The DM pins provide additional strobes when accessing a x4 DIMM.) During reads, the DDR DRAMs source the DQS strobes **aligned** with MDAT and are used within the AMD-761 system controller to capture read data. (The DM pins are used to receive the DQS signals from the DDR DRAMs when accessing a x4 DIMM.) MDAT[63:0] are floated when neither the AMD-761 system controller nor the memory are driving the bus.

Table 36. Signal Descriptions (Continued)

Signal	Type	Description
MECC[7:0]	B	**DDR ECC** MECC[7:0] carry error correction codes for the eight bytes of data on MDAT[63:0]. These signals are inputs to the AMD-761 system controller during DRAM read cycles and outputs during DRAM write cycles. During writes, the AMD-761 system controller provides the clock-forwarded DQS[8:0] strobes centered within the write data. The DQS strobes are used to capture the ECC write data at the DDR DRAMs. (The DM pins provide additional strobes when accessing a x4 DIMM.) During reads, the DDR DRAMs source the DQS strobes **aligned** with MECC and are used within the AMD-761 system controller to capture the ECC read data. (The DM pins are used to receive the DQS signals from the DDR DRAMs when accessing a x4 DIMM.) MECC[7:0] are floated when neither the AMD-761 system controller nor the memory are driving the bus.
CASA# and CASB#	O	**DDR Column Address Strobes** CASA# and CASB# are column address strobe signals for the DDR DRAMs. They operate in parallel to drive greater loads than a single signal can support. The CASx signal is 1 bit of the 3-bit DDR DRAM command bus. These control signals are driven inactive (negated) by RESET#. The memory controller asserts or de-asserts these signals relative to CLKOUT at the appropriate time in the memory access sequence. CASA and CASB are driven a quarter of a cycle off from the CLKOUT rising edge to provide additional HOLD time. See Chapter 2, “Functional Operation” starting on page 7 for more information.
CLKOUT[5:0] and CLKOUT[5:0]#	O	**DDR Clock Outputs** CLKOUT[5:0] and CLKOUT[5:0]# are differential clock pairs to the DDR DIMMs. The clock pairs can be individually disabled for unpopulated DIMM sockets.
RASA# and RASB#	O	**DDR Row Address Strobes** RASA# and RASB# are row address strobe signals for the DDR DRAM. They operate in parallel to drive greater loads than a single signal can support. The RASx signal is 1 bit of the 3-bit DDR DRAM command bus. These control signals are driven inactive (negated) by RESET#. The memory controller asserts or de-asserts these signals relative to CLKOUT at the appropriate time in the memory access sequence. RASA and RASB are driven a quarter of a cycle off from the CLKOUT rising edge to provide additional HOLD time. See Chapter 2, “Functional Operation” starting on page 7 for more information.
WEA# and WEB#	O	**DDR Memory Write Enables** WEA# and WEB# are write enable signals for the DDR DRAM. They operate in parallel to drive greater loads than a single signal can support. The WEx signal is 1 bit of the 3-bit DDR DRAM command bus. These control signals are driven inactive (negated) by RESET#. The memory controller asserts or de-asserts these signals relative to CLKOUT at the appropriate time in the memory access sequence. WEA and WEB are driven a quarter of a cycle off from the CLKOUT rising edge to provide additional HOLD time. See Chapter 2, “Functional Operation” starting on page 7 for more information.

Table 36. Signal Descriptions (Continued)

Signal	Type	Description
AGP/PCI Signals		
A_AD[31:00]	B *TS*	**AGP/APCI Address/Data Bus** These pins are the multiplexed address/data bus, sampled on the rising edge of AGPCLK. The address is valid on A_AD[31:00] during the first clock when FRAME# is asserted. Write data is valid on A_AD[31:00] when A_IRDY# is asserted and read data is valid when A_TRDY# is asserted. Data transfers occur on A_AD[31:00] when both A_IRDY# and A_TRDY# are asserted.
A_C/BE[3:0]#	B *TS*	**AGP/APCI Command/Byte Enables** During the address phase, these pins define the PCI command. During the data phase these pins are used as byte enables.
AGPCLK	I	**AGP/APCI Clock** AGPCLK receives a 66-MHz clock from the system clock generator. AGPCLK is used by the AMD-761™ system controller logic in the AGP clock domain.
A_DEVSEL#	B *STS*	**APCI Device Select** The AMD-761 system controller asserts this pin when an external bus master drives a valid address within the memory region of the AMD-761 system controller. The AMD-761 system controller responds only to memory cycles. This pin is sampled by the AMD-761 system controller when the CPU accesses a PCI target. A_DEVSEL# is not used during AGP transfers.
A_FRAME#	B *STS*	**APCI Cycle Frame** The A_FRAME# pin is asserted by the AMD-761 system controller to indicate the beginning of a bus transaction. A_FRAME# is sampled by the AMD-761 APCI target controller when an external bus master is performing a transaction on the PCI bus. A_FRAME# is not used during AGP transfers.
A_GNT#	O *TS*	**AGP/APCI Bus Grant** As the AGP bus arbiter, the AMD-761 system controller asserts A_GNT# in response to A_REQ# from the initiator (graphics controller) to indicate to the initiator that it has been granted control of the bus. At the same time, the system controller provides status information on status signals ST[2:0] to indicate to the initiator whether it is to supply data or receive data in response to a previously queued request. A_GNT# is asserted in response to an A_REQ#. A reset forces A_GNT# to be negated.
A_IRDY#	B *STS*	**AGP/APCI Initiator Ready** The AMD-761 system controller asserts this signal during APCI transactions to indicate that write data is valid or it is ready to receive read data. It is sampled by the AMD-761 system controller during transactions by the AGP master.
A_PAR	B *TS*	**APCI Bus Parity** PAR is used to generate and check for even parity across the AAD[31:00] and A_C/BE[3:0]# pins. The AMD-761 system controller generates but does not check parity. A_PAR# is not used during AGP transfers.
A_REQ#	I	**AGP/APCI Bus Request** As the bus arbiter, the AMD-761 system controller monitors A_REQ# to determine if the graphics controller requests access to the AGP bus. If A_REQ# is sampled asserted, the arbiter asserts A_GNT# as soon as the bus is available.

Table 36. Signal Descriptions (Continued)

Signal	Type	Description
A_SERR#	I	**APCI System Error** A_SERR# is not used during AGP transfers. An assertion on the A_SERR# pin during APCI transfers can be forwarded to the PCI SERR# pin when enabled in AMD-761 configuration registers.
A_STOP#	B *STS*	**APCI Bus Stop** The A_STOP# signal is asserted by the AMD-761™ system controller APCI target logic to initiate a disconnect by the AGP master. As a master, the AMD-761 system controller stops the current transfer when it samples the A_STOP# signal asserted. A_STOP# is not used during AGP transfers.
A_TRDY#	B *STS*	**AGP/APCI Target Ready** The A_TRDY# signal is asserted by the AMD-761 system controller during accesses by an external bus master when read data is valid or when the target logic is ready to receive write data. This signal is sampled by the AMD-761 AGP master logic when the AMD-761 system controller is accessing an external APCI target.
AGP-Only Signals		
ADSTB[1:0]	B *STS*	**AGP AD Bus Strobe** These signals are driven by the agent that is providing the data, and are used to generate a timing strobe for 2X AGP transfers. ADSTB[0] is used for A_AD[15:00], and ADSTB[1] is used for A_AD[31:16].
ADSTB[1:0]#	B *STS*	**AGP AD Bus Strobe (4X Timing)** These signals are driven by the agent that is providing the data, and are used to generate a timing strobe for 4X AGP transfers. ADSTB[0]# is used for A_AD[15:00], and ADSTB[1]# is used for A_AD[31:16].
PIPE#	I *STS*	**APG Pipelined Request** This signal is asserted by the current master to indicate that a full-width request should be enqueued by the AMD-761 AGP target controller. The AMD-761 system controller enqueues a new request each edge of AGPCLK while the PIPE# signal is asserted.
RBF#	I	**AGP Read Buffer Full** This signal indicates that the AGP master's input buffer is full, and that it cannot accept more read data. When this signal is asserted by the AGP master, the AMD-761 system controller does not attempt to return previously requested low-priority read data.
WBF#	I	**AGP Write Buffer Full** This signal indicates that the AGP master cannot accept more fast writes from the AMD-761 system controller. When this signal is asserted by the AGP master, the AMD-761 system controller does not attempt to initiate fast writes.
SBA[7:0]	I	**AGP Sideband Address Bus** These pins provide an additional bus that can be used to pass commands (address and data) from the AGP master to the AMD-761 system controller. The sideband bus is driven by an external AGP master.
SBSTB/SBSTB#	I *STS*	**AGP Sideband Strobes** These strobes are driven by the AGP master to provide timing for the sideband address bus (SBA[7:0] pins). The SBSTB# pin provides the complement of SBSTB and is used only for AGP 4X timing mode.

Table 36. Signal Descriptions (Continued)

Signal	Type	Description
ST[2:0]	O	**AGP Status** This bus is used to provide status from the AMD-761™ system controller to the AGP master. These signals are valid only when the A_GNT# signal is asserted (Low), and must be ignored by the AGP master at all other times. The status bits are encoded as follows: 000 = Indicates that previously requested low-priority read or flush data is being returned to the master. 001 = Indicates that previously requested high-priority read data is being returned to the master. 010 = Indicates that the master provides low-priority write data for a previous enqueued write command. 011 = Indicates that the master provides high-priority write data for a previous enqueued write command. 100 = Reserved 101 = Reserved 110 = Reserved 111 = Indicates that the master has been given permission to start a bus transaction. The master can enqueue AGP requests by asserting PIPE# or start a PCI transaction by asserting FRAME#. ST[2:0] are always an output from the core logic and an input to the master.
Miscellaneous Signals		
TEST#	I	**Test Mode Enable** The TEST# pin is used by AMD for internal chip testing. It is also used to enter NAND tree and three-state test modes for motherboard manufacturing test, as described in Chapter 3.
DCSTOP#	I	**DRAM Controller Stop** This pin is used to support ACPI S1 and S3 power management modes. It is asserted by the AMD-766 peripheral bus controller to enter the S1 power state, and asserted in conjunction with RESET# to enter the S3 state. Refer to "Power Management" on page 24 for details of AMD-761 system controller power management modes.
VSS/VDD, I/O Pad and Voltage Reference, and Compensation Pins		
VSS		VSS
VDD_CORE		AMD-761 VDD pins, 2.5 Vdc.
VDD_PCI		VDD for PCI I/O cells, 3.3 Vdc.
VDD_AGP		This pin functions as VDD for AGP I/O cells, and can be 1.5 Vdc or 3.3 Vdc as determined by TYPEDET# pin on the motherboard. The motherboard drives this input to 1.5 Vdc when the TYPEDT# pin is asserted Low by an AGP card, or 3.3 Vdc when the TYPEDET# pin is High.
AVDD		Separately filtered 2.5 Vdc for analog PLL circuitry.
AGP_CAL and AGP_CAL#		Compensation pads for matching impedance of motherboard AGP traces.
P0_CAL and P0_CAL#		Compensation pads for matching impedance of motherboard AMD Athlon system bus traces.
AGP_VREF		Voltage reference for 3.3 Vdc AGP I/O cells.

Table 36. Signal Descriptions (Continued)

Signal	Type	Description
AGP_VREF4X		Voltage reference for 1.5 Vdc AGP I/O cells.
REF_5V		Voltage reference to support 5 Vdc PCI signalling.
P0_VREF		AMD Athlon system bus I/O voltage reference.
DDR_REF		DDR I/O voltage reference.
S_CLKREF		System clock reference voltage.
CPU_VCORE		Voltage for push-pull I/O pads.
SI_VSS and SI_VDD		Connected to the AMD-761™ system controller VSS and VDD_CORE planes. These are intended only for signal integrity testing and should be connected to the motherboard VSS and VDD_CORE planes, respectively.

7.1 Initialization Pinstrapping

The AMD-761 system controller requires various strapping options to define the SIP stream returned to the AMD Athlon™ processor after reset, as well as to define specific AMD-761 system controller operating parameters. The pinstraps are set by 10K pullup or pulldown resistors attached externally to PCI bus pins, and they are sampled during reset. Unless otherwise defined, strapping options are enabled when pulled High, disabled when pulled Low. BIOS can read the value latched on most of these pinstraps in the Configuration Status register (Dev 0:F0:0x88). Table 37 on page 89 contains a description of the pinstrapping signals.

Table 37. Initialization Pinstrapping

Signal	Type	Description
Initialization Pinstrapping		
AD[31:30]	I	**ClkSpeed** These pinstraps are used to define the clock speed of the AMD Athlon™ system bus, and are encoded as follows: 00: 100 MHz 01: 66 MHz 10: Reserved 11: 133 MHz
AD[29]	I	**PLL Reset** This pin must be driven low when using the PLL bypass test mode. This pin is also optionally used in test modes as described in Chapter 3. A pullup resistor is required on this pinstrap for normal operation.
AD[28]	I	**SysClkThresh** This pin functions as the AMD Athlon system bus threshold range select for the system clock input receiver. When Low, the system clock input senses thresholds between 0.6 V and 1.0 V. When High, the inputs sense thresholds between 1.0 V and 1.4 V.
AD[27:26]	I	**Reserved**
AD[25]	I	**Three-State-Enable (For Test Only)** When pulled High, this pin enables board test mode when TEST# is asserted. Refer to Chapter 3 for details of this test mode bit.
AD[24]	I	**Inclk_Delay_Enable** When this pin is pulled High, forwarded clocks originating in the AMD-761™ system controller are delayed 1/4 SysClk period to place their edge in the nominal center of the associated data. Certain SIP parameters are also adjusted. When pulled Low, the forwarded clock edges are concurrent with the associated data transitions.
AD[23]	I	**NAND_TreeEnable (For Test Only)** When this pin is pulled High, NAND tree test mode is enabled when TEST# is asserted. Refer to Chapter 3 for details of this test mode bit.
AD[22:21]	I	**CPU_ClkHist** This field selects the amount of hysteresis applied to the SysDataOutClk[3:0]# and SysAddrOutClk# inputs for noise immunity. This field is encoded as follows: 00: No hysteresis 01: Low hysteresis (preferred setting) 10: Medium hysteresis 11: Maximum hysteresis
AD[20]	I	**TypeDet#** This pin functions as the AGP card type detect, used by the AGP I/O cells for impedance compensation. The latched value of the TYPEDET# pin can also be read in the Configuration Status register (Dev 0:F0:0x88). 0: AGP card with 1.5-V referencing installed 1: AGP card with 3.3-V referencing installed

Table 37. Initialization Pinstrapping (Continued)

Signal	Type	Description
AD[19:16]	I	**Reserved**
AD[15]	I	**General-Purpose Status** This bit can be used for any general-purpose communication to BIOS for motherboard-specific features. It is recommended that this bit be pulled down if not used. The value of this pinstrap can be read in the Configuration Status register (Dev 0:F0:0x88).
AD[14:12]	I	**AGPClock_Mux[2:0] (For Test Only)** This bit field selects input to APLL clock mux for PLL test mode. Refer to Chapter 3 for details of these bits.
AD[11:10]	I	**Length** This bit field selects the CPU 0 physical AMD Athlon™ system bus length: 00: Short, non-slot A 01: Single Slot A or close 10: Far dual slot A 11: Farthest possible slot A See the *AMD Athlon™ System Bus Design Guide*, Rev. B, PID #22666, for details of the bus length assumptions used in the bus timing calculations.
AD[9]	I	**Bypass_PLLs (For Test Only)** If this pin is pulled High, PLL bypass mode is enabled when TEST# is asserted. Refer to Chapter 3 for details of PLL bypass mode.
AD[8]	I	**OutClk_Delay_Enable** When this pin is pulled High, forwarded clocks originating in the AMD Athlon are delayed to the nominal center of the associated data. This control is provided by adjusting SIP parameters. When pulled Low, the AMD Athlon forwarded clock edges are concurrent with the associated data transitions. For details refer to the SIP mapping description in the *AMD Athlon™ System Bus Specification*, order# 21902.
AD[7:5]	I	**SysClock_Mux[2:0] (For Test Only)** This bit field selects input to SPLL clock mux for PLL test mode. Refer to Chapter 3 for details of these bits.
AD[4]	I	**CPU_Thresh** This pin functions as the AMD Athlon system bus threshold range select for AMD Athlon system bus I/O cells. When Low, the AMD Athlon system bus inputs sense thresholds between 0.6 V and 1.0 V. When High, the inputs sense thresholds between 1.0 V and 1.4 V.
AD[3:0]	I	**CPU_Div** These pins define the clock multiplier for the CPU, and are generated by the CPU. They are used internally to create the frequency ID (FID) value, which is used in the generation of SIP values sent to the AMD Athlon processor during initialization.

Table 37. Initialization Pinstrapping (Continued)

Signal	Type	Description
C/BE[3]#	I	**Reserved** This pin must always have a pullup resistor installed for proper operation.
C/BE[2]#	I	**Reserved** This pin must always have a pullup resistor installed for proper operation.
C/BE[1]#	I	**AGP4X Test Mode** This pin should be pulled up when testing AGP in the 4X rate mode. This allows a 4X clock to be driven on the AGPCLK pin, and sets the appropriate internal clock dividers.
C/BE[0]	I	**SipRomEnable** This pin enables an external serial ROM containing processor and system controller initialization parameters when pulled High. The initialization data is read from the external SIP ROM at power-on and transferred to the processor and system controller. When this pin is pulled Low, the SIP stream is generated internally and transferred to the processor and system controller. This feature is typically used only for debug and test modes.

7.2 Pin Multiplexing

Some pin functions are multiplexed on PCI pins as described in Table 38 on page 92. Note that additional pin multiplexing is required for scan testing, and is described in Chapter 3. The pin multiplexing for scan mode does not affect normal operation.

Pin multiplexing is defined for test modes only, and requires specific PCI bus signalling pins to be pulled Low during reset (RESET# asserted). Note that if these test functions are used on the motherboard in lab debugging, the normal PCI signal pullup resistors need replacing temporarily with pulldown resistors. This action should be done only for lab testing and not in a production environment. These signals include the following:

- IRDY# pin for the TEST_RESET# function
- PAR pin for PLL output test mode.

These functions are described in detail in Chapter 3.

Table 38. Pin Multiplexing Options

Primary/Secondary Pin Name	Primary Function	Secondary Function
GNT[6]#/AGPCLKOUT	PCI bus grant #6	APLL clock output for PLL test. Refer to Chapter 3 for details of this function.
GNT[5]#/SYSCLKOUT	PCI bus grant #5	SPLL clock output for PLL test. Refer to Chapter 3 for details of this function.
GNT[3]#/DDR_NAND	PCI bus grant #3	Output of the DDR DRAM interface NAND tree.
GNT[2]#/PCI_NAND	PCI bus grant #2	Output of the PCI bus interface NAND tree.
GNT[1]#/AGP_NAND	PCI bus grant #1	Output of the AGP interface NAND tree.
GNT[0]#/CPU_NAND	PCI bus grant #0	Output of the AMD Athlon™ system bus interface NAND tree.
CBE[1]#/ROM_SDA	PCI bus command/byte enable bit 1	SIP ROM data bit when using an external ROM to load processor interface initialization data.
CBE[0]#/ROM_SCK	PCI bus command/byte enable bit 0	SIP ROM clock when using an external ROM to load processor interface initialization data. This feature is enabled via pinstrapping. When this pin is sampled High during reset, the external SIP ROM is enabled.
IRDY#/TEST_RST#	PCI bus IRDY# pin	Reset pin dedicated to PLL clock dividers. Refer to Chapter 3 for details of this function. Used only for PLL testing.
TRDY#/SCAN_EN#	PCI bus TRDY# pin	Enables scan testing when TEST# is asserted. Not used in normal operation.
PAR/PLL_TEST#	PCI bus PAR (parity) pin	Enables clock testing when TEST# is asserted. The values on pinstraps AGPClock_Mux[2:0] and SysClock_Mux[2:0] strapping pins select the clock mux inputs. Refer to Chapter 3 for details of PLL test mode.

7.3 Pin States at Reset

The AMD-761 system controller default pin states are defined in Table 39 on page 93. These are listed for all output and bidirectional pins in the power-on reset state (reset) as well as the ACPI S1 and S3 power management states. Refer to “Power Management” on page 24 for details of the S1 and S3 modes.

Note that most AMD-761 internal configuration registers are initialized to a known value when RESET# is asserted. To accommodate the ACPI S3 (suspend to RAM) power management state, the memory controller registers are not initialized at power-up and must be programmed by BIOS

following the first power-up. For further details refer to Chapter 2 on page 7 and the *AMD-761™ System Controller Software/BIOS Design Guide,* order# 24081.

Table 39. Reset Pin States

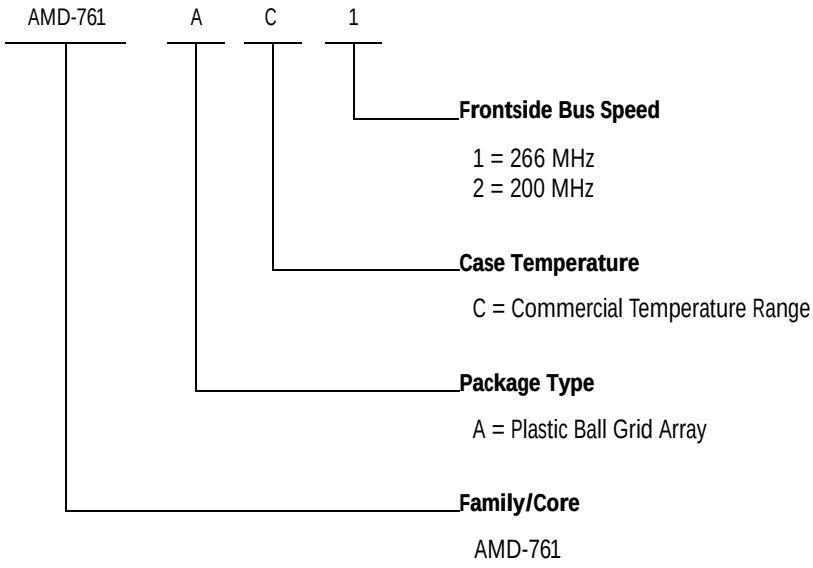
Pin Name	RESET# State	S1 State	S3 State	Comments
CLKFWDRST	1	1	Z	
CONNECT	1	0	Z	
SADDIN[14:2]#	1	1	Z	
SADDINCLK#	1	1	Z	
SDATA[63:0]#	1	Park	Z	Parked signals maintain their previous value.
SDATAINCLK[3:0]#	1	1	Z	
SDATAINVAL#	1	1	Z	
AD[31:00]	Z	Park	Z	
C/BE[3:0]#	Z	Park	Z	
DEVSEL#	Z	Z	Z	
FRAME#	Z	Z	Z	
GNT[6:0]#	Z	1	Z	
IRDY#	Z	Z	Z	
PAR	Z	Park	Z	
SBGNT#	Z	1	Z	
SERR#	Z	Z	Z	
STOP#	Z	Z	Z	
TRDY#	Z	Z	Z	
WSC#	Z	Z	Z	
CS[7:0]#	1	1	Z	
DM[8:0]	Z	Z	Z	
DQS[8:0]	Z	Z	Z	
MAA[14:0]	0	*	Z	* Unbuffered=Z, Registered=previous value
MAB[14:0]	0x7BFF	*	Z	* Unbuffered=Z, Registered=previous value
CKEA	0	0	0	
CKEB	0	0	0	
MDAT[63:0]	Z	Z	Z	
MECC[7:0]	Z	Z	Z	
CASA#	1	*	Z	* Unbuffered=Z, Registered=1
CASB#	1	*	Z	* Unbuffered=Z, Registered=1
CLKOUT[5:0]	Active	*	Z	* Unbuffered=Z, Registered=active

Table 39. Reset Pin States

Pin Name	RESET# State	S1 State	S3 State	Comments
CLKOUT[5:0]#	Active	*	Z	* Unbuffered=Z, Registered=active
RASA#	1	*	Z	* Unbuffered=Z, Registered=1
RASB#	1	*	Z	* Unbuffered=Z, Registered=1
WEA#	1	*	Z	* Unbuffered=Z, Registered=1
WEB#	1	*	Z	* Unbuffered=Z, Registered=1
A_AD[31:00]	Z	Park	Z	
A_C/BE[3:0]#	Z	Park	Z	
A_DEVSEL#	Z	Z	Z	
A_FRAME#	Z	Z	Z	
A_GNT#	1	1	Z	
A_IRDY#	Z	Z	Z	
A_PAR	Z	Park	Z	
A_STOP#	Z	Z	Z	
A_TRDY#	Z	Z	Z	
ADSTB[1:0]	Z	Z	Z	
ADSTB[1:0]#	Z	Z	Z	
SBSTB	Z	Z	Z	Input only
SBSTB#	Z	Z	Z	Input only
ST[2:0]	1	Park	Z	

8 Ordering Information

AMD standard products are available in several packages and operating ranges. The order number is formed by a combination of the elements below. Contact your AMD representative for detailed ordering information.



Conventions, Abbreviations, and References

This section contains information about the conventions and abbreviations used in this document and a list of related publications.

Signals and Bits

- Active-Low Signals—Signal names containing a pound sign, such as SFILL#, indicate active-Low signals. They are asserted in their Low-voltage state and negated in their High-voltage state. When used in this context, High and Low are written with an initial upper case letter.
- Signal Ranges—In a range of signals, the highest and lowest signal numbers are contained in brackets and separated by a colon (for example, D[63:0]).
- Reserved Bits and Signals—Signals or bus bits marked *reserved* must be driven inactive or left unconnected, as indicated in the signal descriptions. These bits and signals are reserved by AMD for future implementations. When software reads registers with reserved bits, the reserved bits must be masked. When software writes such registers, it must first read the register and change only the non-reserved bits before writing back to the register.
- Three-State—In timing diagrams, signal ranges that are high impedance are shown as a straight horizontal line half-way between the high and low levels.
- Invalid and Don't-Care—In timing diagrams, signal ranges that are invalid or don't-care are filled with a screen pattern.

Data Terminology

The following list defines data terminology:

- Quantities
  - A *word* is two bytes (16 bits)
  - A *doubleword* is four bytes (32 bits)
  - A *quadword* is eight bytes (64 bits)
  - An AMD Athlon™ processor cache line is eight quadwords (64 bytes)

- Addressing—Memory is addressed as a series of bytes on eight-byte (64-bit) boundaries in which each byte can be separately enabled.
- Abbreviations—The following notation is used for bits and bytes:
  - Kilo (K, as in 4-Kbyte page)
  - Mega (M, as in 4 Mbits/sec)
  - Giga (G, as in 4 Gbytes of memory space)

  See Table 41 for more abbreviations.
- Little-Endian Convention—The byte with the address xx...xx00 is in the least-significant byte position (little end). In byte diagrams, bit positions are numbered from right to left—the little end is on the right and the big end is on the left. Data structure diagrams in memory show low addresses at the bottom and high addresses at the top. When data items are aligned, bit notation on a 64-bit data bus maps directly to bit notation in 64-bit-wide memory. Because byte addresses increase from right to left, strings appear in reverse order when illustrated.
- Bit Ranges—In text, bit ranges are shown with a dash (for example, bits 9–1). When accompanied by a signal or bus name, the highest and lowest bit numbers are contained in brackets and separated by a colon (for example, AD[31:0]).
- Bit Values—Bits can either be set to 1 or cleared to 0.
- Hexadecimal and Binary Numbers—Unless the context makes interpretation clear, hexadecimal numbers are followed by an h and binary numbers are followed by a b.

Abbreviations and Acronyms

Table 40 contains the definitions of abbreviations used in this document.

Table 40. Abbreviations

Abbreviation	Meaning
A	Ampere
F	Farad
G	Giga-
Gbit	Gigabit
Gbyte	Gigabyte
H	Henry

Table 40. Abbreviations (Continued)

Abbreviation	Meaning
h	Hexadecimal
K	Kilo-
Kbyte	Kilobyte
M	Mega-
Mbit	Megabit
Mbyte	Megabyte
MHz	Megahertz
m	Milli-
ms	Millisecond
mW	Milliwatt
µ	Micro-
µA	Microampere
µF	Microfarad
µH	Microhenry
µs	Microsecond
µV	Microvolt
n	nano-
nA	nanoampere
nF	nanofarad
nH	nanohenry
ns	nanosecond
ohm	Ohm
p	pico-
pA	picoampere
pF	picofarad
pH	picohenry
ps	picosecond
s	Second
V	Volt
W	Watt

Table 41 contains the definitions of acronyms used in this document.

Table 41. Acronyms

Abbreviation	Meaning
AAT	AGP Address Translator
ACK	Acknowledge
ACPI	Advanced Configuration and Power Interface
AGP	Accelerated Graphics Port
APCI	AGP Peripheral Component Interconnect
API	Application Programming Interface
APIC	Advanced Programmable Interrupt Controller
BAR	Base Address Register
BIOS	Basic Input/Output System
BIST	Built-In Self-Test
BIU	Bus Interface Unit
CS	Chip Select
DDR	Double-Data Rate
DIMM	Dual Inline Memory Module
DMA	Direct Memory Access
DRAM	Direct Random Access Memory
ECC	Error Correcting Code
EIDE	Enhanced Integrated Device Electronics
EISA	Extended Industry Standard Architecture
EPROM	Enhanced Programmable Read Only Memory
FID	Frequency Integer Divisor
FIFO	First In, First Out
GART	Graphics Address Remapping Table
HSTL	High-Speed Transistor Logic
IACK	Interrupt Acknowledge
IDE	Integrated Device Electronics
IMB	Interrupt Message Bus
ISA	Industry Standard Architecture
JEDEC	Joint Electron Device Engineering Council
JTAG	Joint Test Action Group
LRU	Least-Recently Used
LSB	Least Significant Bit

Table 41. Acronyms (Continued)

Abbreviation	Meaning
LVTTL	Low Voltage Transistor Transistor Logic
MA	Memory Address
MCT	Memory Controller
MD	Memory Data
MRL	Memory Read Line
MRM	Memory Read Multiple
MSB	Most Significant Bit
MTRR	Memory Type and Range Registers
MWF	Memory Write FIFO
MWI	Memory Write-and-Invalidate
MUX	Multiplexer
NMI	Non-Maskable Interrupt
OD	Open Drain
PBGA	Plastic Ball Grid Array
PA	Physical Address
PCI	Peripheral Component Interconnect
PH	Page Hit
PLL	Phase Locked Loop
POS	Power-On Suspend
POST	Power-On Self-Test
PPA	Physical Page Address
PT	Page Tables
PTE	Page Table Entries
RAM	Random Access Memory
ROM	Read Only Memory
SBA	Sideband Address
SDRAM	Synchronous Direct Random Access Memory
SIP	Serial Initialization Packet
SMbus	System Management Bus
SMC	SDRAM Memory Controller
SPD	Serial Presence Detect
SRAM	Synchronous Random Access Memory
SROM	Serial Read Only Memory
TLB	Translation Lookaside Buffer

Table 41. Acronyms (Continued)

Abbreviation	Meaning
TTL	Transistor Transistor Logic
VAS	Virtual Address Space
VPA	Virtual Page Address
VGA	Video Graphics Adapter

Related Publications

The following books discuss various aspects of computer architecture that may enhance your understanding of AMD products:

AMD Publications

AMD Athlon™ Processor Data Sheet, order# 21016

AMD-766™ Peripheral Bus Controller Data Sheet, order# 22548

Bus Architecture

PCI Local Bus Specification, Revision 2.2, PCI Special Interest Group, Hillsboro, Oregon, 1998.

AT Bus Design, Edward Solari, IEEE P996 Compatible, Annabooks, San Diego, CA, 1990.

Accelerated Graphics Port Interface Specification, Revision 2.0, Intel Corporation, AGP Forum, 1998.

x86 Architecture

Programming the 80386, John Crawford and Patrick Gelsinger, Sybex, San Francisco, 1987.

80x86 Architecture & Programming, Rakesh Agarwal, Volumes I and II, Prentice-Hall, Englewood Cliffs, NJ, 1991.

General References

Computer Architecture, John L. Hennessy and David A. Patterson, Morgan Kaufman Publishers, San Mateo, CA, 1990.

Websites

Visit the AMD website for documentation of AMD products.

www.amd.com

Other websites of interest include the following:

- JEDEC home page—www.jedec.org
- IEEE home page—www.computer.org
- AGP Forum—www.agpforum.org