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Digital Jitter Attenuation (DJA) Controller

Introduction

The digital jitter attenuator controller is a macrocell block that is extractable from the TMXF28155 Super Mapper application-specific standard product (ASSP).

The DJA controller contains 28 DJA blocks. Each DJA block can operate in two different modes, as a DS1 or an E1 jitter attenuator. In both modes, the DJA blocks can be provisioned to operate as a second-order phase-locked loop (PLL) always, or it can switch to act as a first-order PLL during virtual tributary (VT) pointer adjustments to help meet MTIE requirements. The block will also insert the proper alarm indication signal (AIS) if the primary block AIS control input is active. The PLL bandwidth can be set over a wide range to accommodate a number of different system constraints.

Features

The DJA block accepts/delivers DS1/E1 clock, data, and AIS indications from/to the cross connect block.

- AIS will cause the correct AIS clock to be inserted, and the AIS indication will be passed back to the cross connect.

- The DJA blocks operate in the second-order PLL mode under normal conditions. The DJA blocks can be provisioned to enter the first-order PLL mode following VT-level pointer adjustments. The period of time in the first-order mode is provisionable via registers.

- The PLL bandwidth is provisionable between 0.1 Hz and 0.5 Hz. The damping factor for these bandwidths varies between 2 Hz and 0.5 Hz.

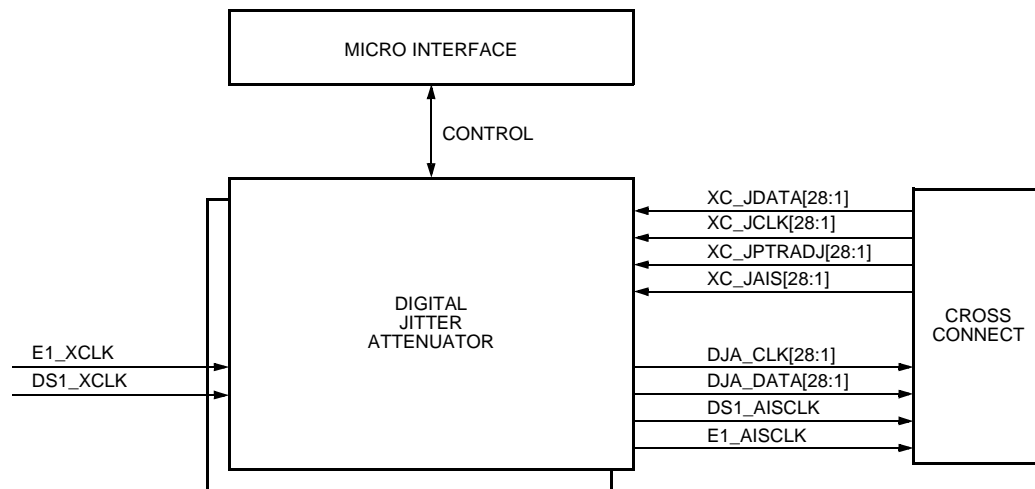Figure 1 shows the DJA block with I/O connections to other blocks within the Super Mapper device.

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Figure 1. DJA Block with I/O Connections to Other Blocks in the TMXF28155 Super Mapper

Functional Block Diagram of the DJA Block

The functional view of the DJA block, along with interconnections to the other blocks within the Super Mapper device, are shown in Figure 2.

The DJA block interfaces only to the cross connect and microprocessor interface blocks within the Super Mapper device. The input interface between the DJA block and the cross connect block consists of clock, serial data, VT pointer adjustment indication, and AIS insert indication. The output interface consists of clock, serial data, and AIS insert indication, as well as the DS1 and E1 AIS clocks for use by other blocks within the device.
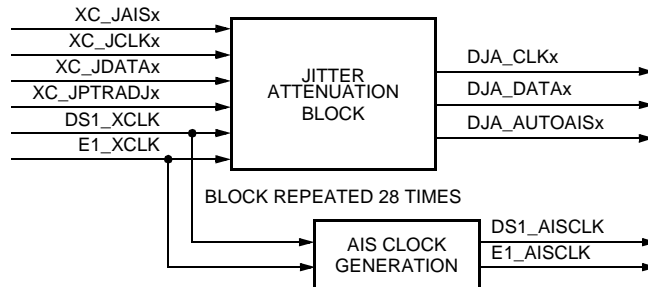
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Figure 2. Basic Functional Flow of the DJA Block

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