IS 61C67

16K X 1 HIGH SPEED CMOS STATIC RAM

PRELIMINARY
OCTOBER 1990

FEATURES

- High speed access time 15, 20, 25ns (Max.)
- Low active power- 200mW (Typical)
- Low standby power-55mW (Typical) TTL standby -10µW (Typical) CMOS standby (L-version)
- Fully static operation-no clock or refresh required
- TTL compatible inputs and outputs
- 2V data retention for battery backup (L-version)
- Single 5V power supply

DESCRIPTION

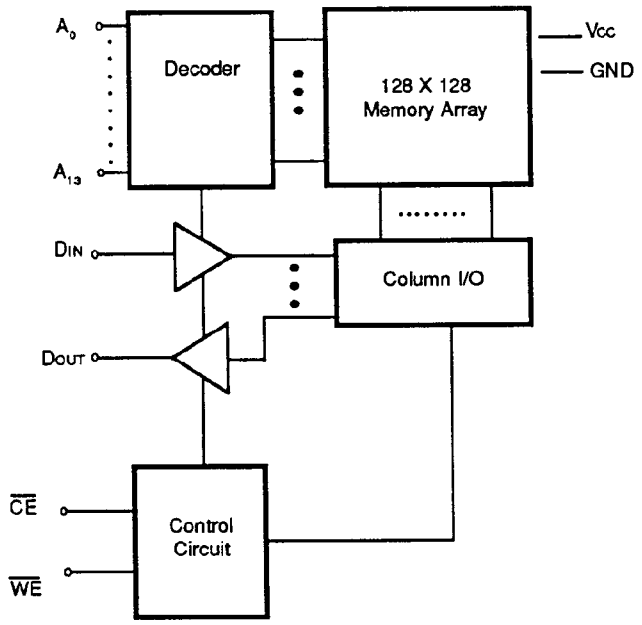
The ISSI IS61C67 is a high speed, low power, 16384- word by 1- bit CMOS static RAM. It is fabricated using ISSI's high performance CMOS double metal technology. This highly reliable process coupled with innovative circuit design techniques, yields access times as fast as 15ns maximum.

When $\overline{CE}$ is high (de-selected), the device assumes a standby mode at which the power dissipation can be reduced down to 10µW typical at CMOS input levels (L-version).

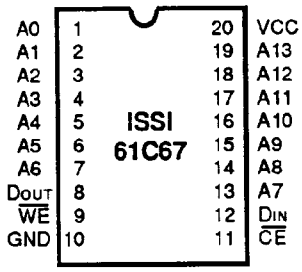
Easy memory expansion is provided by using active low Chip Enable Input. The active low Write Enable controls both writing and reading of the memory.

The IS61C67 is avaliable in 300 mil PDIP.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION



DIP

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TRUTH TABLE

MODE	$\overline{WE}$	$\overline{CE}$	DIN	DOUT	V_{CC} CURRENT
Not Selected (Power Down)	X	H	X	High Z	I_{SB_1}, I_{SB_2}
Read	H	L	X	DOUT	I_{CC_1},I_{CC_2}
Write	L	L	DIN	High Z	I_{CC_1},I_{CC_2}

SWITCHING CHARACTERISTICS OVER OPERATING RANGE (1)

Parameter	Description	IS61C67-15 IS61C67-L15		IS61C67-20 IS61C67-L20		IS61C67-25 IS61C67-L25		Units
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
READ CYCLE								
tRC	Read Access Time	15		20		25		ns
tAA	Address Access Time		15		20		25	ns
tOHA	Output Hold Time	3		3		3		ns
tACE	$\overline{CE}$ Access Time		15		20		25	ns
tLZCE	$\overline{CE}$ to Low Z Output	3		3		3		ns
tHZCE (2)	$\overline{CE}$ to High Z Output		8		10		12	ns
tPU	$\overline{CE}$ to Power Up	0		0		0		ns
tPD	$\overline{CE}$ to Power Down		15		20		20	ns
WRITE CYCLE (3)								
tWC	Write Cycle Time	15		20		25		ns
tSCE	$\overline{CE}$ to Write End	15		17		22		ns
tAW	Address Set-up Time to Write End	15		17		20		ns
tHA	Address Hold to Write End	0		0		0		ns
tSA	Address Set-up Time	0		0		0		ns
tPWE	$\overline{WE}$ Pulse Width	14		17		20		ns
tSD	Data Set-up to Write End	8		10		12		ns
tHD	Data hold to Write End	0		0		0		ns
tHZWE (2)	$\overline{WE}$ Low to High-Z Output		6		7		8	ns
tLZWE	$\overline{WE}$ High to Low-Z Output	0		0		0		ns

Notes:
1. Test conditions assume signal transition times of 5ns or less, timing reference levels of 1.5V, Input pulse levels of 0 to 3.0V and output loading specified in Figure 1a.
2. Tested with the load in Figure 1b. Transition is measured ± 500mV from steady state voltage.
3. The internal write time is defined by the overlap of $\overline{CE}$ low and $\overline{WE}$ low. All signals must be in valid states to initiate a Write, but any one can go inactive to terminate the Write. The Data input Setup and Hold timing are referenced to the rising or falling edge of the signal that terminates the write.
4. $\overline{WE}$ is high for a Read Cycle.
5. The device is continuously selected. $\overline{CE}$ = VIL.
6. Address is valid prior to or coincident with $\overline{CE}$ Low transitions.

AC TEST CONDITIONS

Input Pulse Level	0V to 3.0V
Input Rise and Fall Times	5ns
Input and Output Timing and Reference Level	1.5V

AC TEST LOADS

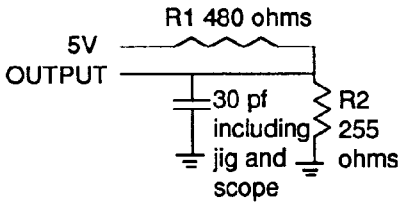


Figure 1a

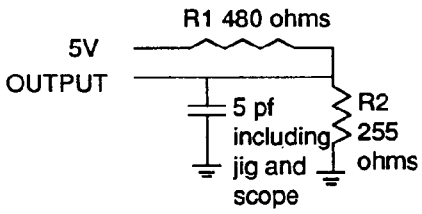
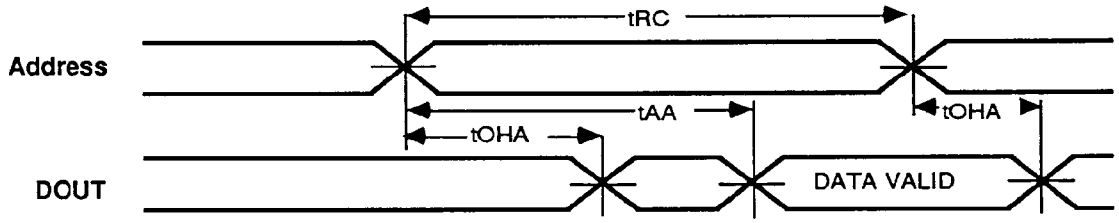


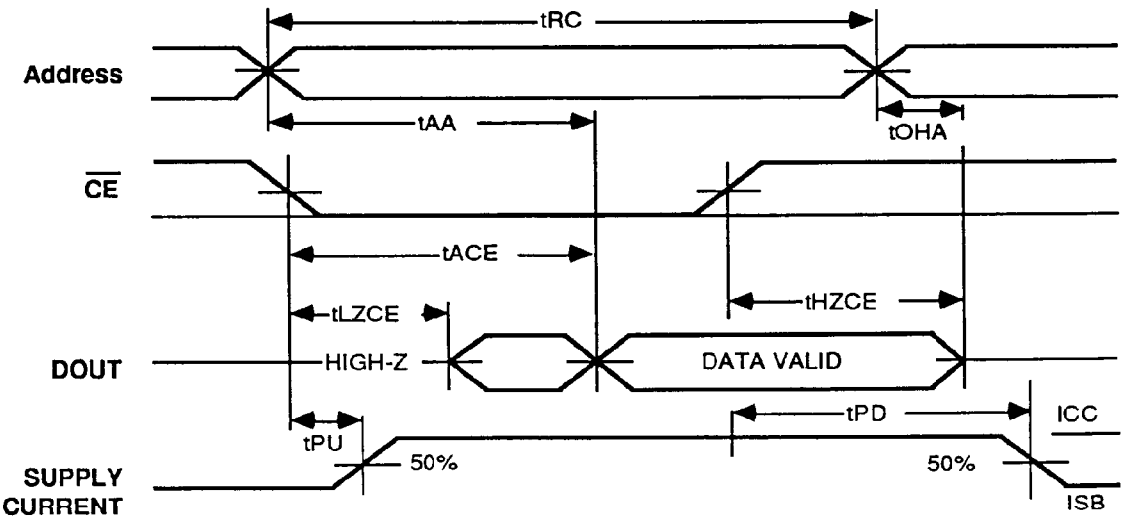
Figure 1b

AC WAVEFORMS

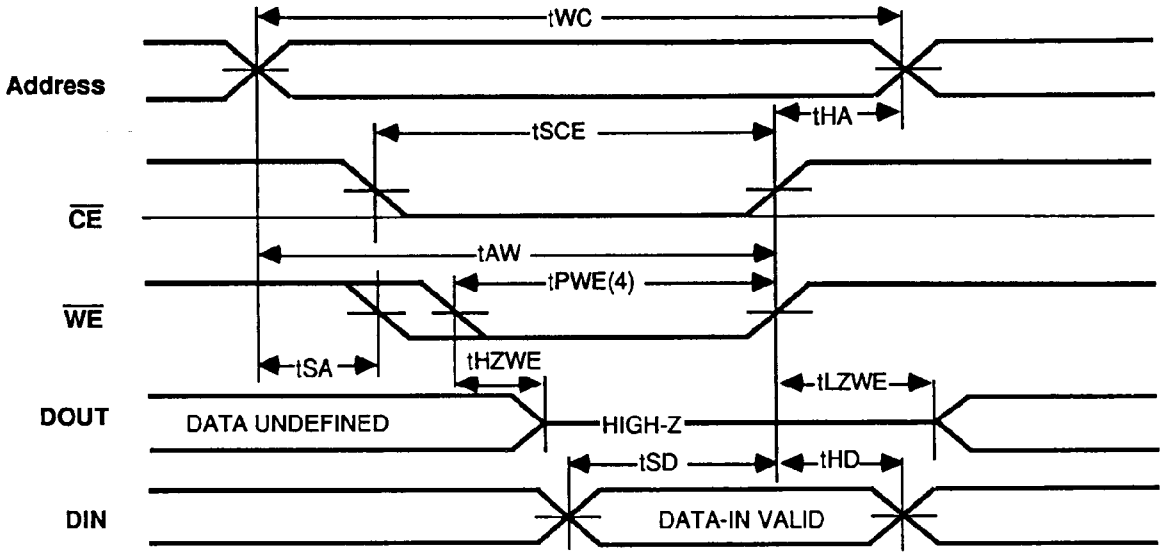
READ CYCLE NO. 1 (Note 4, 5)



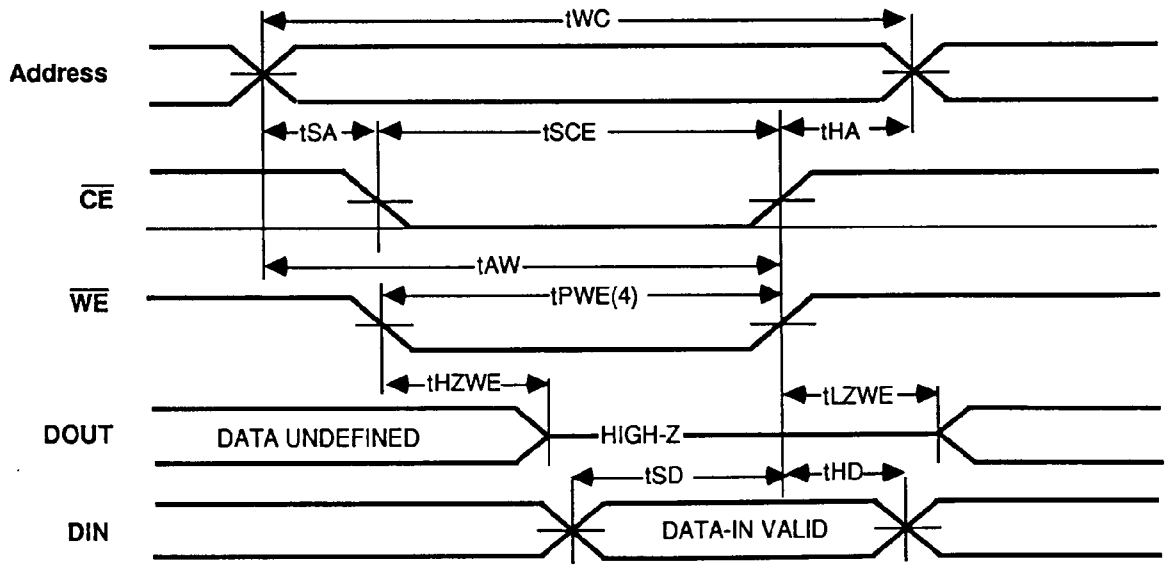
READ CYCLE NO. 2 (Note 4,6)



WRITE CYCLE NO. 1 ($\overline{WE}$ controlled) (Note 3)



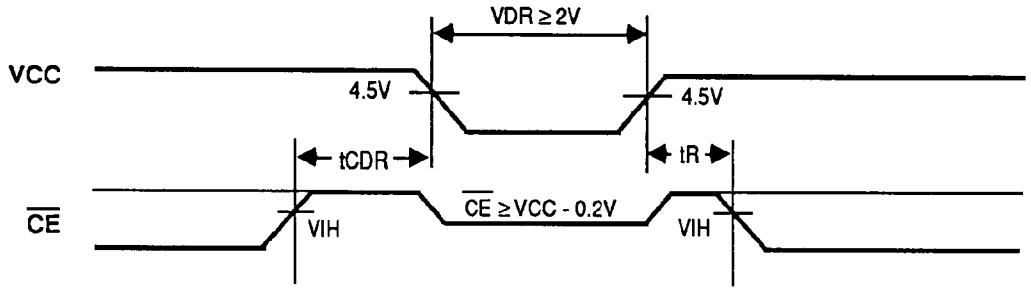
WRITE CYCLE NO. 2 ($\overline{CE}$ controlled) (Note 3)



DATA RETENTION CHARACTERISTICS (L-version only)

Parameter	Description	Test Condition	Min.	Max.	Units
VDR	VCC for retention of data	VCC = 2.0V	2.0	----	V
ICCDR	Data retention current	$\overline{CE}$ ≥ VCC - 0.2V,	-----	100	µA
tCDR	Chip deselect to data retention time	CMOS Inputs	0	-----	ns
tR	Operation recovery time		tRC	----	ns
ILI	Input leakage current		------	2	µA

DATA RETENTION WAVEFORM



PIN DESCRIPTIONS

A_0 - A_{13} Address Inputs
These 14 address inputs select one of the 16,384 1-bit words in the RAM.

$\overline{CE}$ Chip Enable Input
$\overline{CE}$ is active low. The chip enable is active to read from or write to the device. If chip enable is not active, the device is deselected and is in a standby power mode. The DOUT pins will be in the high-impedance state when the device is deselected.

GND - Ground

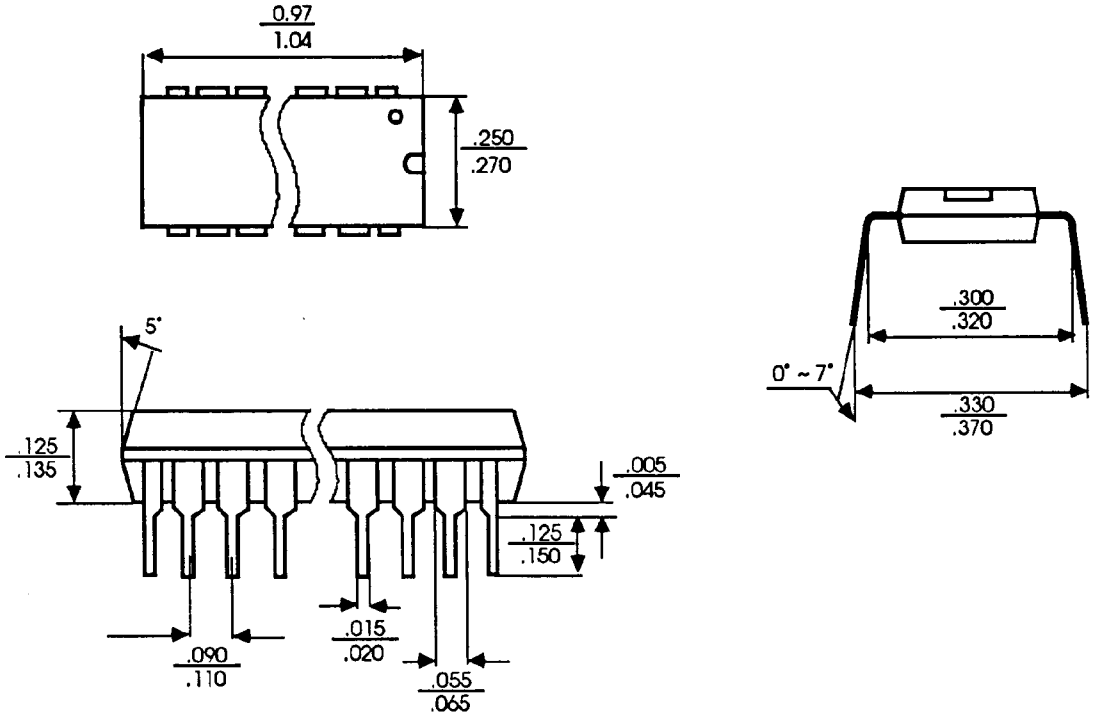
$\overline{WE}$ Write Enable Input
The write enable input is active low and controls read and write operations. With the chip selected, when $\overline{WE}$ is low Input data present on the I/O pins will be written into the selected memory location.

DIN
Data input port used to write data into the RAM.

DOUT
Data output port used to read data from the RAM.

Vcc - Power

20 PIN 300 Mil Plastic Dip Package



SPEED (ns)	ORDER PART NUMBER	PACKAGE	TEMPERATURE RANGE
15	IS61C67-15N	Plastic DIP - 300 mil	0°C to +70°C
15 Low Power	IS61C67-L15N	Plastic DIP - 300 mil	0°C to +70°C
20	IS61C67-20N	Plastic DIP - 300 mil	0°C to +70°C
20 Low Power	IS61C67-L20N	Plastic DIP - 300 mil	0°C to +70°C
25	IS61C67-25N	Plastic DIP - 300 mil	0°C to +70°C
25 Low Power	IS61C67-L25N	Plastic DIP - 300 mil	0°C to +70°C