Product Brief
August 2000

microelectronics group

Lucent Technologies
Bell Labs Innovations

LU6X14FT
1.0—1.25/2.0—2.5/3.125 Gbits/s SERDES

Description

The LU6X14FT is a quad transceiver for serial data transmission over fiber or coaxial media from 1.0 Gbits/s—3.125 Gbits/s. The device is available in a 208-pin PBGAM package. The block diagram of the chip is shown in Figure 1 on page 2. The transmitter section accepts either 8-bit unencoded data or 10-bit encoded data at the parallel input port. It also accepts the low-speed system clock at the REFCLK input and uses this clock to synthesize the internal high-speed serial bit clock. In the 1.0 Gbits/s—1.25 Gbits/s mode, the parallel input data is latched on the falling edge of the low-speed TBC clock. In the 2.0 Gbits/s to 3.125 Gbits/s mode, the parallel input data is framed by the rising and falling edges of the low-speed TBC clock. REFCLK and TBC clock are required to be the same frequency, but the phase relationship is arbitrary. The serialized data is available at the differential CML output, terminated by 50 Ω or 75 Ω, to drive either an optical transmitter or coaxial media.

The receive section receives high-speed serial data at its differential CML input port. This data is fed to the clock recovery section which generates a recovered clock and retimes the data. The retimed data is deserialized and presented as a 10-bit encoded or a 8-bit unencoded parallel data on the output port. Two-phase receive byte clocks are available synchronous with the parallel words. The receiver also recognizes the comma characters and aligns the bit stream to the proper word boundary.

The quad transceiver is controlled and configured with an 8-bit microprocessor interface. Each channel has dedicated registers that are readable and writable. The quad device also contains global registers for control of common circuitry and functions.

Potential Applications

- Stand-alone transceiver product.
- Transceiver macrocell template.

Features

- Designed to operate in Ethernet, fibre channel, *FireWire**, or backplane applications.
- Operationally compliant with the fibre channel X3T11. Provides FC-0 services at 1.0 Gbits/s—1.25 Gbits/s, 2.0 Gbits/s—2.5 Gbits/s, and 3.125 Gbits/s.
- Selectable data rate (1.0 Gbits/s—1.25 Gbits/s, 2.0 Gbits/s—2.5 Gbits/s, and 3.125 Gbits/s).
- 100 MHz—156 MHz differential CML or single-ended CMOS reference clock.
- 8-bit/10-bit parallel I/O interface.
- Programmable control and configuration interface to define the various device configurations.
- Automatic lock to reference in absence of receive data.
- CML high-speed interface I/O for use with optical transceiver, coaxial copper media, or shielded twisted pairs.
- Programmable transmit pre-emphasis optimized for backplanes.
- Requires one external resistor for bias current generation.
- Requires no external components for clock recovery and frequency synthesis.
- Under 250 mW per transceiver.
- Low powerdown dissipation.
- 1.5 V ± 5% power supply.
- 1.8 V ± 5% power supply option for differential high speed I/O circuits.
- –40 °C—70 °C ambient temperature.

* *FireWire* is a registered trademark of Apple Computer, Inc.

Block Diagrams

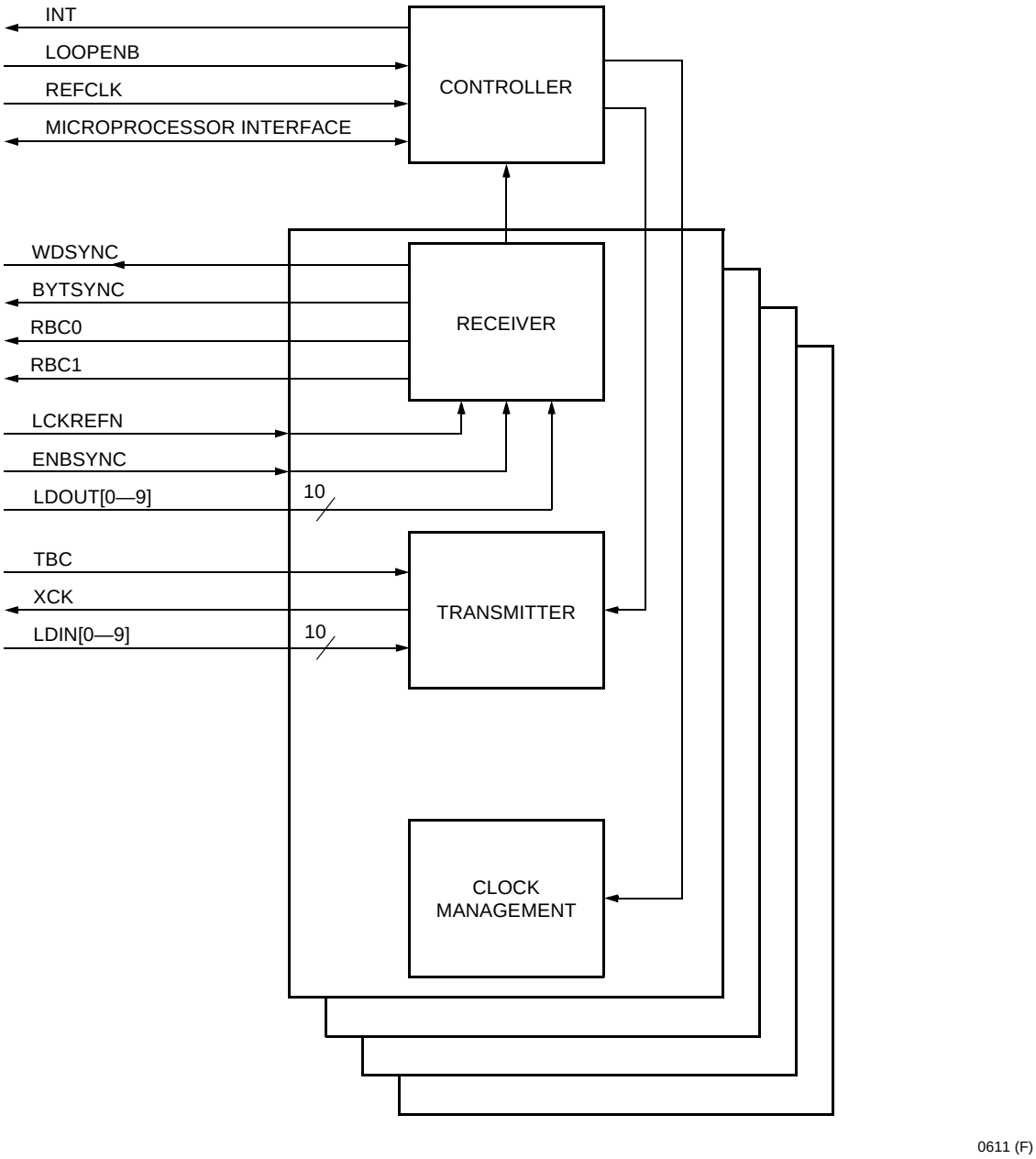
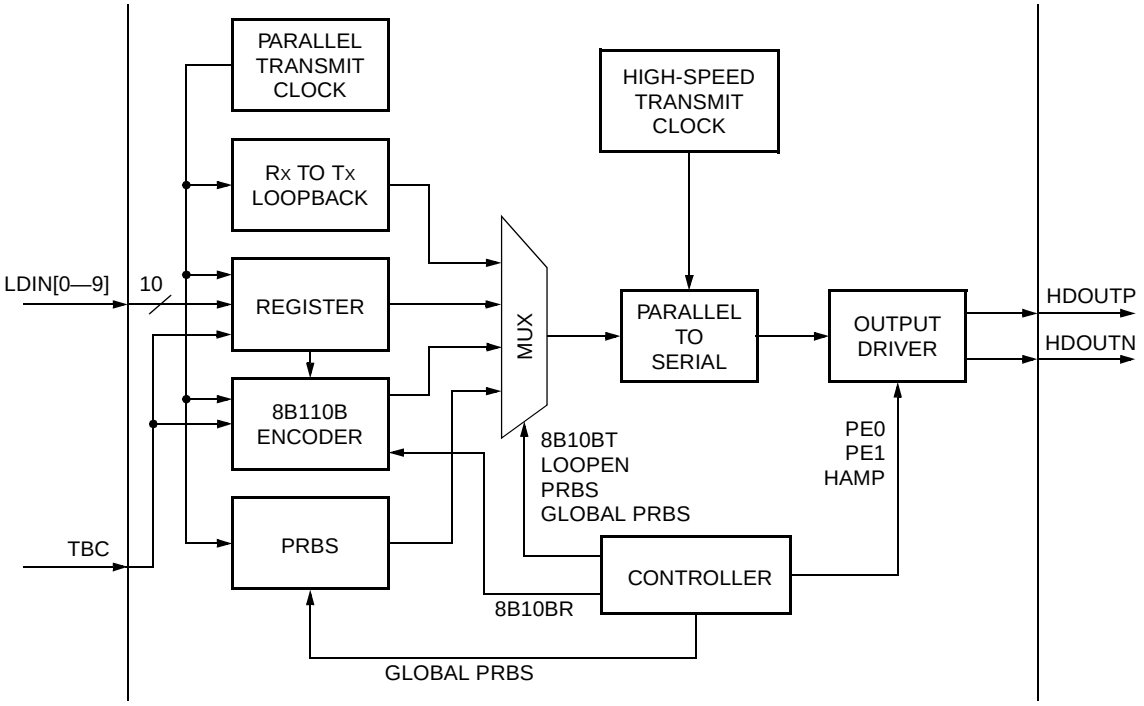


Figure 1. LU6X14FT Block Diagram

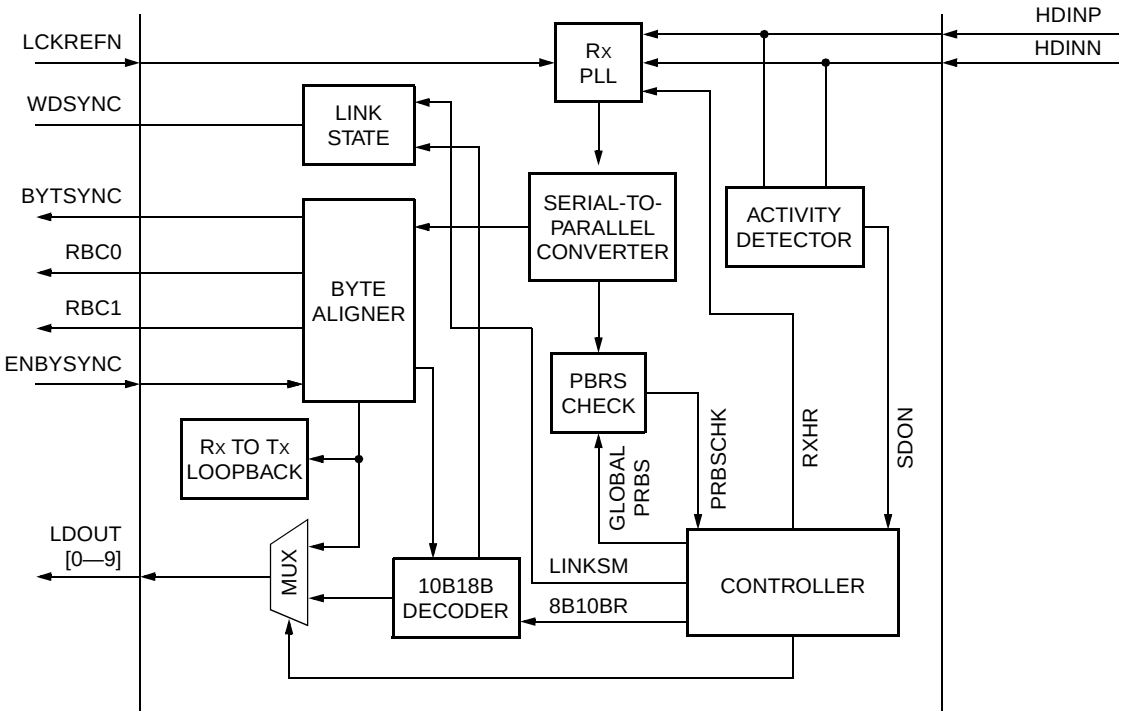
Block Diagrams (continued)



0610 (F)

Figure 2. LU6X14FT Transmit Detail

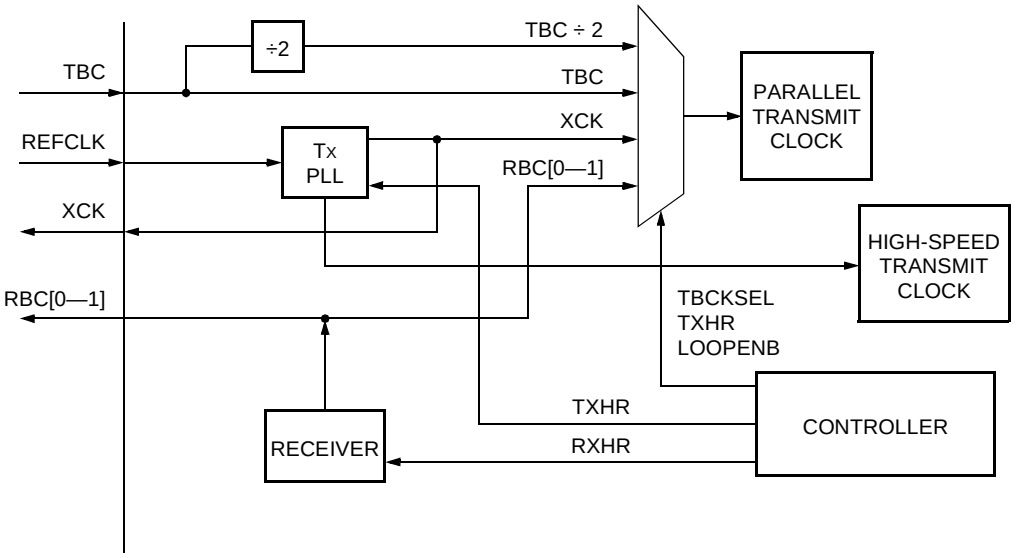
Block Diagrams (continued)



0609 (F)

Figure 3. LU6X14FT Receive Detail

Block Diagrams (continued)



0608 (F)

Figure 4. Clock Management

Functional Description

Bias Section

A fractional band-gap voltage generator is included on the chip. A precision external resistor connected between the pins RESIN and RESRT is used to generate the bias currents within the chip. The value of this resistor should be 3.32 kΩ ± 1%. The current handling capability of this resistor should be at least 300 μA.

Transmit/Receive Data Rate Selection

The high-speed transmit and receive serial data can operate at 1.0 Gbits/s—1.25 Gbits/s or 2.0 Gbits/s—3.125 Gbits/s, depending on the state of the TXHR and RXHR control bits from the microprocessor interface. The REFCLK and TBC clock are always frequency synchronous. Table 1 shows the relationship between the data rates and the input and recovered clocks.

Table 1. Input and Recovered Clock Rates for Different Data Rates

Data Rate	TBC/Reference Clock	RBC[0:1]
1.0 Gbits/s	100 MHz	50 MHz
1.25 Gbits/s	125 MHz	62.5 MHz
2.0 Gbits/s	100 MHz	100 MHz
2.5 Gbits/s	125 MHz	125 MHz
3.125 Gbits/s	156 MHz	156 MHz

Functional Description (continued)

Reference Clock

The differential clock is distributed to all of the four channels. Each channel has a differential buffer to isolate the clock from the other channels. The input clock is preferably a differential signal; however, the device can operate with a single-ended input. The input reference clock directly impacts the transmit data eye, so the clock should have low jitter. In particular, jitter components in the dc—5 MHz range should be minimized.

Transmitter Section

The block diagram of the transmitter is shown in Figure 2 on page 3. The 8-bit unencoded or 10-bit encoded parallel input data word is latched into an on-chip register with the externally supplied TBC clock and serialized at ten times the incoming parallel data rate. When the transmitter is operating in the half rate mode (1.0 Gbits/s—1.25 Gbits/s), the falling edge of the TBC clock is used to latch the data. When the transmitter is operating in the full rate mode (2.0 Gbits/s—3.125 Gbits/s), the TBC clock frames the input data so that when TBC is high a bit is latched by an internal clock and again when TBC is low. The full rate data makes transitions on both edges of the clock as shown in Figure 6 on page 7. Table 2 shows the timing margins.

TBC is the same frequency as REFCLK; however, it is assumed to be of arbitrary phase w.r.t. REFCLK. During a powerup reset sequence, the phase relationship between REFCLK, TBC, and the PLL generated high-speed clock is established. The relative phase of the input clocks, TBC and REFCLK, must remain fixed after the powerup sequence is completed.

A 256-state PRBS generator is included on the chip to enable testability in loopback mode.

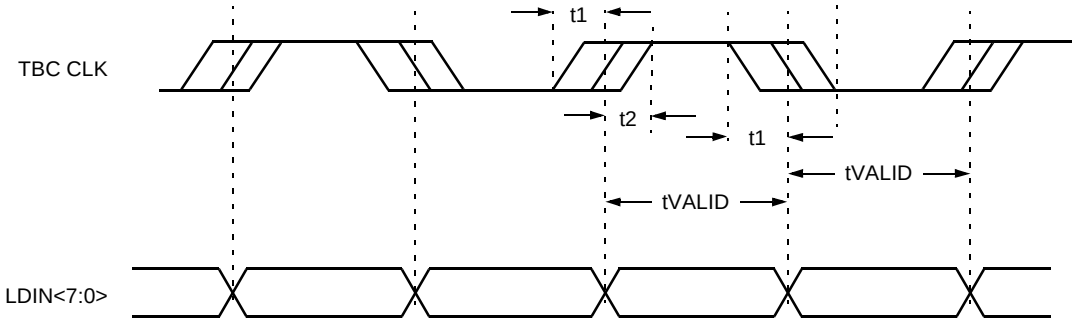


Figure 5. Transmit Timing Diagram

Table 2. Timing Relationship of LDIN and TBC Clock at Full Rate (3.125 Gbits/s)

Parameter	Minimum	Typical	Maximum	Unit
t_1	—	—	1.0	ns
t_2	—	—	0.5	ns
t_{valid}	2.5	—	—	ns

In the half-rate mode, the incoming data transitions only on the rising edge of the clock, as shown in Figure 6 on page 7. Table 3 on page 7 shows the timing relationships in this case.

Functional Description (continued)

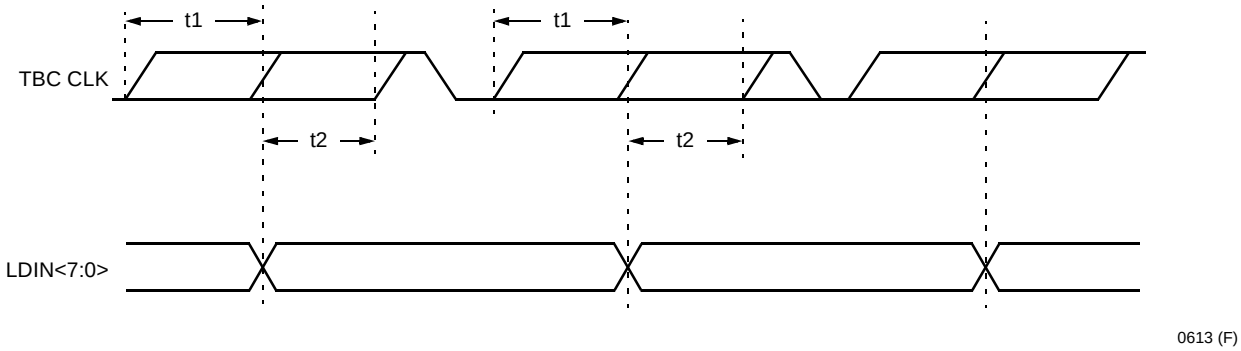


Figure 6. Transmit Timing Waveform

Table 3. Timing Relationship of LDIN and TBC Clock at Half Rate (1.25 Gbits/s)

Parameter	Minimum	Typical	Maximum	Unit
t_1	—	—	3.2	ns
t_2	—	—	3.2	ns

The maximum latency of the transmitter, counting from the corresponding edge of the data transition at the input to the instance when the first high speed serial bit is transmitted, is 5 byte periods when the 8B/10B encoder is not used. With the encoder, the maximum latency is 6 byte periods.

For additional information, contact your Microelectronics Group Account Manager or the following:

INTERNET: **http://www.lucent.com/micro**
E-MAIL: **docmaster@micro.lucent.com**
N. AMERICA: Microelectronics Group, Lucent Technologies Inc., 555 Union Boulevard, Room 30L-15P-BA, Allentown, PA 18109-3286
1-800-372-2447, FAX 610-712-4106 (In CANADA: **1-800-553-2448**, FAX 610-712-4106)
ASIA PACIFIC: Microelectronics Group, Lucent Technologies Singapore Pte. Ltd., 77 Science Park Drive, #03-18 Cintech III, Singapore 118256
Tel. (65) 778 8833, FAX (65) 777 7495
CHINA: Microelectronics Group, Lucent Technologies (China) Co., Ltd., A-F2, 23/F, Zao Fong Universe Building, 1800 Zhong Shan Xi Road, Shanghai 200233 P. R. China **Tel. (86) 21 6440 0468**, **ext. 325**, FAX (86) 21 6440 0652
JAPAN: Microelectronics Group, Lucent Technologies Japan Ltd., 7-18, Higashi-Gotanda 2-chome, Shinagawa-ku, Tokyo 141, Japan
Tel. (81) 3 5421 1600, FAX (81) 3 5421 1700
EUROPE: Data Requests: MICROELECTRONICS GROUP DATALINE: **Tel. (44) 7000 582 368**, FAX (44) 1189 328 148
Technical Inquiries: GERMANY: **(49) 89 95086 0** (Munich), UNITED KINGDOM: **(44) 1344 865 900** (Ascot),
FRANCE: **(33) 1 40 83 68 00** (Paris), SWEDEN: **(46) 8 594 607 00** (Stockholm), FINLAND: **(358) 9 4354 2800** (Helsinki),
ITALY: **(39) 2 6608131** (Milan), SPAIN: **(34) 1 807 1441** (Madrid)

August 2000
PB00-124CMPR-1

microelectronics group

Lucent Technologies
Bell Labs Innovations