

MSM64481

Built-in 512-Bit EEPROM and LCD Driver 4-Bit Microcontroller

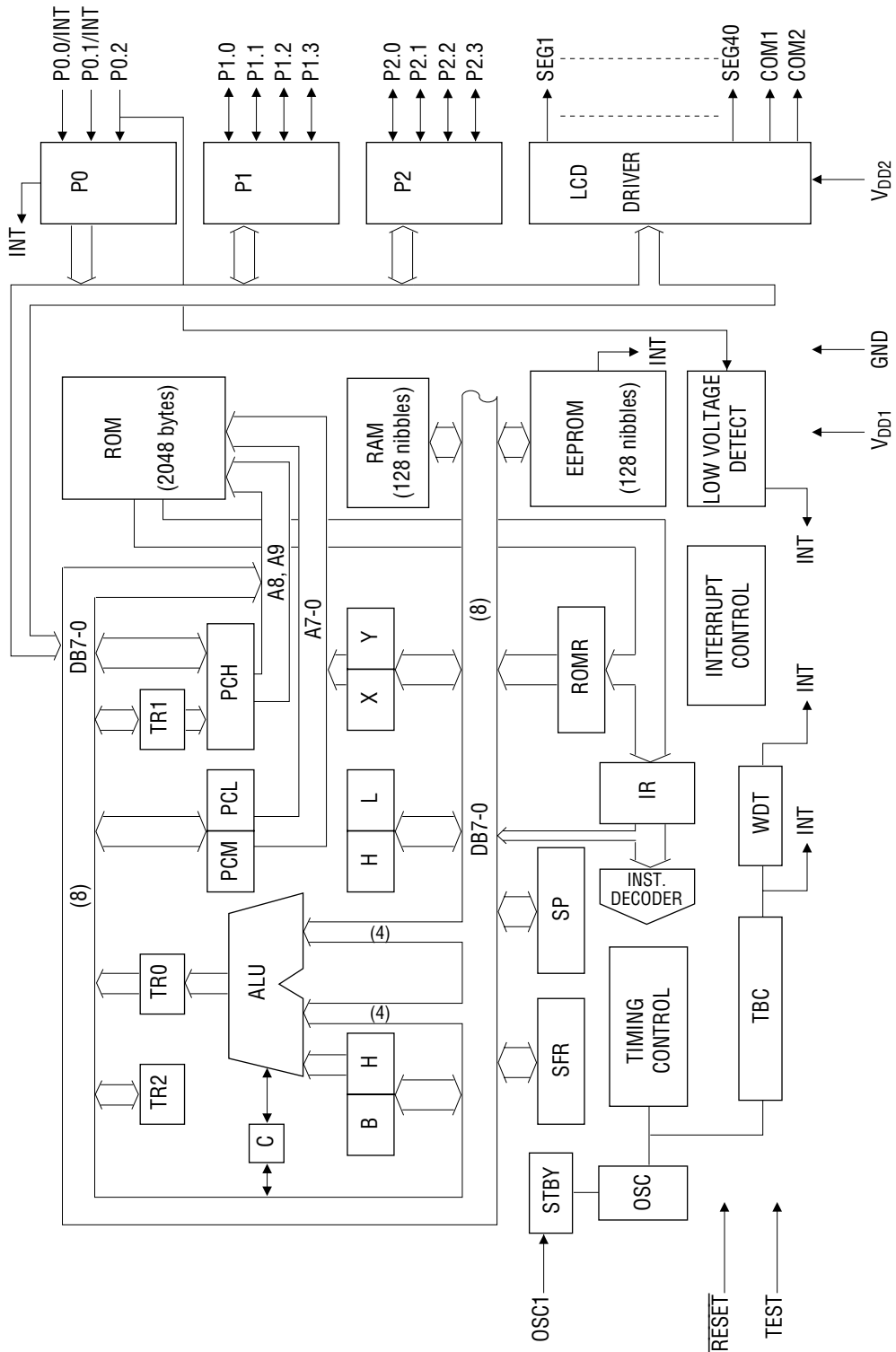
GENERAL DESCRIPTION

The MSM64481 is a 4-bit microcontroller with built-in EEPROM that incorporates OKI's nX-4s CPU core. The device contains a 2K-byte ROM, 128-nibble RAM, 128-nibble EEPROM, 1/2 duty LCD driver, time base counter, watchdog timer, low voltage detection circuit, seven interrupt sources, one 3-bit input port, two 4-bit input/output ports, and 500 kHz RC oscillator circuit (with an external capacitor C).

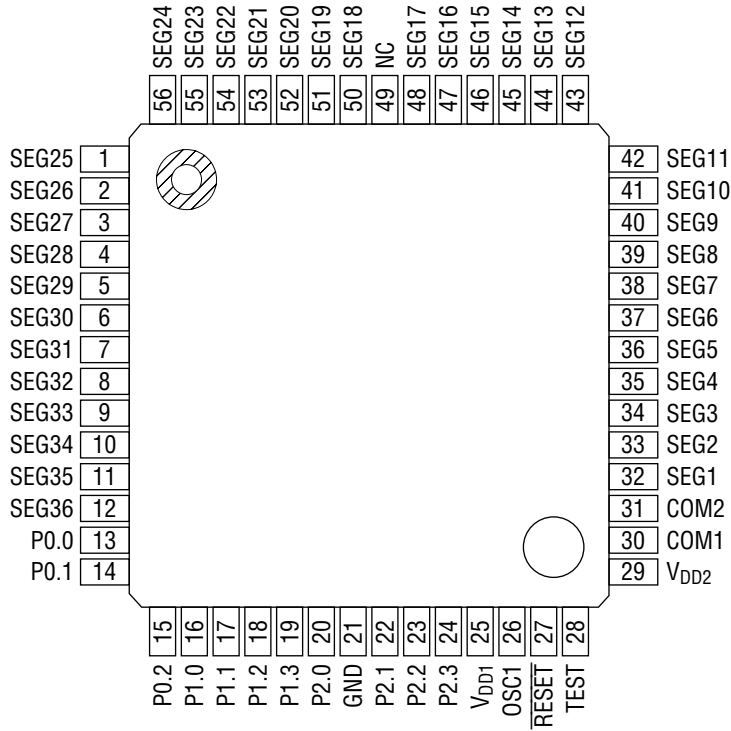
FEATURES

- Operating range
 - Operating frequency : 200 kHz to 1 MHz
 - Operating voltage : 3 to 6 V
 - Operating temperature : -40 to +85°C
- Internal program memory : 2048 bytes
- Internal data memory : 128 nibbles
- Built-in EEPROM : 128 nibbles
- Interrupt sources : 6 (3 internal, 3 external)
- Minimum instruction execution time : 6 μ s (@ 500 kHz)
- I/O Port
 - Input-output port : 2 ports \times 4 bits
 - Input port : 1 port \times 3 bits
- 1/2 duty LCD driver
 - Segment drivers : 40
 - Common drivers : 2
- Built-in watchdog timer
- CPU operating voltage : 3.0 to 5.5 V
- EEPROM writable operating voltage : 4.5 to 5.5 V
- LCD display operating voltage : 3.0 to 6.0 V
- Package options
 - 60-pin plastic QFP (QFP60-P-1519-1.00-K) : (Product name: MSM64481-014GS-K)
 - 56-pin plastic QFP (QFP56-P-910-0.65-2K) : (Product name: MSM64481-014GS-2K-H)

BLOCK DIAGRAM



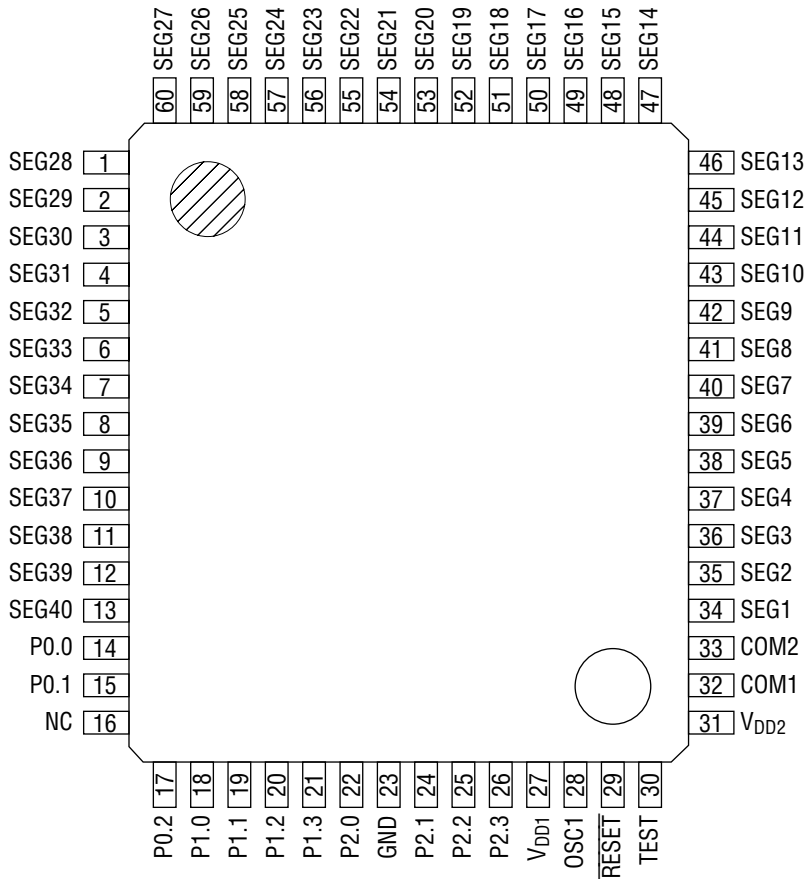
PIN CONFIGURATION (TOP VIEW)



56-Pin Plastic QFP

NC: No-connection pin

PIN CONFIGURATION (TOP VIEW) (Continued)



60-Pin Plastic QFP

NC: No-connection pin

PIN DESCRIPTIONS

Function	Symbol	Type	Description	
Power supply	V _{DD1}	—	—	
	V _{DD2}	—	Power supply for driving the LCD drivers	
Ground	GND	—	Ground	
Control	$\overline{\text{RESET}}$	I	System reset input pin. When this pin is set "L", the internal state is initialized. This pin contains a built-in pull-up resistor.	
	TEST	I	Pin for IC testing	
Ports	P0.0	I	Input port. Also used for external interrupt.	
	P0.1	I	Input port. Also used for external interrupt.	
	P0.2	I	Input port for detecting external voltage	
	P1.0 P1.1 P1.2 P1.3	I/O	I/O port	
	P2.0 P2.1 P2.2 P2.3	I/O	I/O port	
	Display drivers	COM1	0	LCD common driving outputs
		COM2	0	
		SEG1 to SEG40	0	LCD segment driving outputs
Oscillation	OSC1	I	RC oscillator pin (for an external capacitor C)	

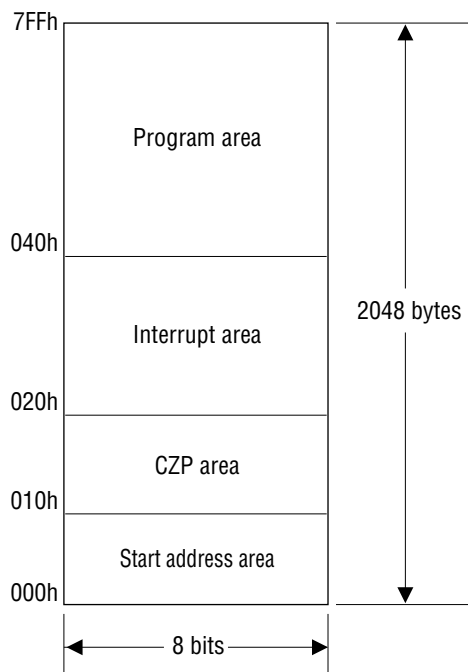
MEMORY MAPS

Program Memory (ROM)

The program memory is a memory area for program data, the interrupt area, the CZP area, and the start address area.

The data length is 8 bits. Address 0 to address 2047 is assigned to program memory.

The following figure shows the address space of program memory.



Program Memory Address Space

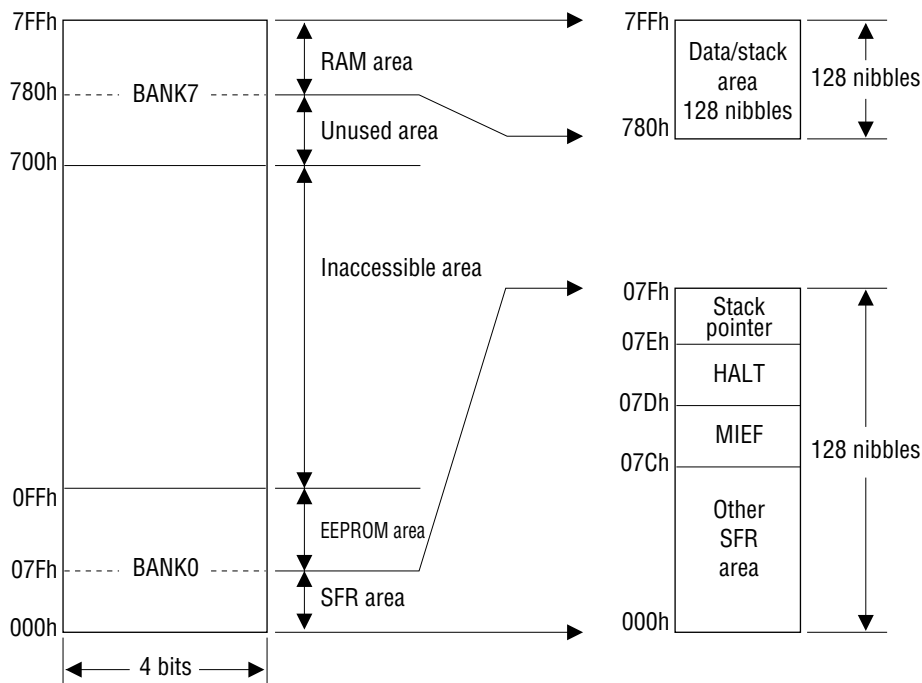
The CZP area is the start address range of a CZP subroutine of one-byte call instruction.

Data Memory (RAM)

The data memory space is assigned to RAM and special function registers (SFRs). Data Memory is located in a different address space from program memory.

The data length is 4 bits (1 nibble), and a bank unit is 256 nibbles. The data memory uses two bank areas: one for the EEPROM and SFR areas, in Bank 0; the other for RAM, including the stack, in Bank 7.

The following figure shows the address space of data memory.



Data Memory Address Space

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Condition	Rating	Unit
Power Supply Voltage	V_{DD1}	$T_a=25^{\circ}\text{C}$	-0.3 to +7	V
Power Supply Voltage for LCD Displays	V_{DD2}	$T_a=25^{\circ}\text{C}$	-0.3 to +7	V
Input Voltage	V_{IN}	$T_a=25^{\circ}\text{C}$	-0.3 to $V_{DD1}+0.3$	V
Output Voltage 1	V_{OUT1}	V_{DD1} output, $T_a=25^{\circ}\text{C}$	-0.3 to $V_{DD1}+0.3$	V
Output Voltage 2	V_{OUT2}	V_{DD2} output, $T_a=25^{\circ}\text{C}$	-0.3 to $V_{DD2}+0.3$	V
Storage Temperature	T_{STG}	—	-55 to +150	$^{\circ}\text{C}$

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Condition	Range	Unit
Operating Voltage 1 (CPU operable range)	V_{DD1}	—	3.0 to 5.5	V
Operating Voltage 2 (EEPROM writable range)	V_{DD1}	—	4.5 to 5.5	V
Operating Voltage (LCD display enable range)	V_{DD2}	—	3.0 to 6.0	V
Operating Frequency	f_{OP}	—	200 to 1000	kHz
EEPROM Rewritable Cycle	—	—	10,000	cycles
EEPROM Data Retaining Years	—	—	10	years
Operating Temperature	T_{op}	—	-40 to +85	$^{\circ}\text{C}$

ELECTRICAL CHARACTERISTICS

DC Characteristics

(V_{DD1}=5 V, V_{DD2}=6 V, T_a=-40 to +85°C unless otherwise specified)

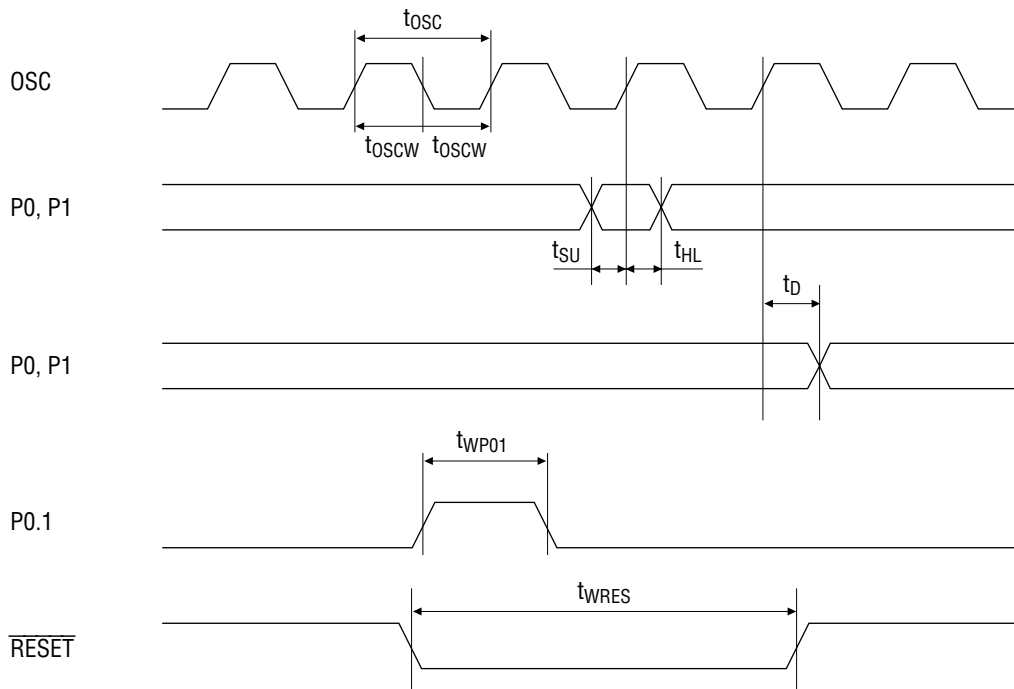
Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Input Voltage 1 (P1.0 to P1.3) (P2.0 to P2.3)	V _{IH1}	—	V _{DD1} ×0.7	—	—	V
	V _{IL1}	—	—	—	V _{DD1} ×0.2	
Input Voltage 2 (P0.0 to P0.2) (TEST, RESETB)	V _{IH2}	—	V _{DD1} ×0.7	—	—	V
	V _{IL2}	—	—	—	V _{DD1} ×0.2	
Input Current 1 (P1.0 to P1.3) (P2.0 to P2.3)	I _{IH1}	V _{IH1} =V _{DD1}	—	—	1	μA
	I _{IL1}	V _{IL1} =GND	-1	—	—	
Input Current 2 (P0.0 to P0.2) (TEST, RESETB)	I _{IH2}	V _{IH2} =V _{DD1}	—	—	1	μA
	I _{IL2}	V _{IL2} =GND	-1	—	—	
Pull-up Resistance (P1.0 to P1.3) (P2.0 to P2.3)	R _{ON}	V _{DD1} =5 V V _I =0 V	5	—	40	kΩ
Output Current 1 (P1.0 to P1.3) (P2.0 to P2.3)	I _{OH1}	V _{DD1} =4.5 V V _O =4.1 V	—	—	-2	mA
	V _{OL1}	V _{DD1} =4.5 V V _O =0.4 V	2	—	—	
Output Voltage 2 (SEG1 to SEG40)	V _{OH2}	V _{DD2} =5 V I _O =-50 μA	—	—	V _{DD2} -0.20	V
	V _{OL2}	V _{DD2} =5 V I _O =50 μA	0.20	—	—	
Output Voltage 3 (COM1 to COM2)	V _{OH3}	V _{DD2} =5 V I _O =-50 μA	—	—	V _{DD2} -0.20	V
	V _{OL3}	V _{DD2} =5 V I _O =50 μA	0.20	—	—	
Intermediate Level Output Voltage (COM1 to COM2)	V _{OM}	V _{DD2} =5 V I _O =±20 μA	2.25	2.50	2.75	V
RC Oscillation Frequency	f _{OSC}	V _{DD1} =4.5 to 5.5 V C=47 pF	500±35%			kHz
Static Current Consumption	I _{DDs} ^{*1}	CPU in halt state	—	—	20	μA
Dynamic Current Consumption	I _{DD1} ^{*2}	CPU in operation	—	—	3	mA
	I _{DD2} ^{*3}		—	—	1	
	I _{DE} ^{*2}	During write to EEPROM	—	—	5	

*1 V_{DD1}=5.5 V, operating frequency f=0 Hz*2 V_{DD1}=5.5 V, V_{DD2}=6 V, operating frequency f=500 kHz*3 V_{DD1}=5.5 V, V_{DD2}=6 V, operating frequency f=500 kHz, LCD in display state

AC Characteristics

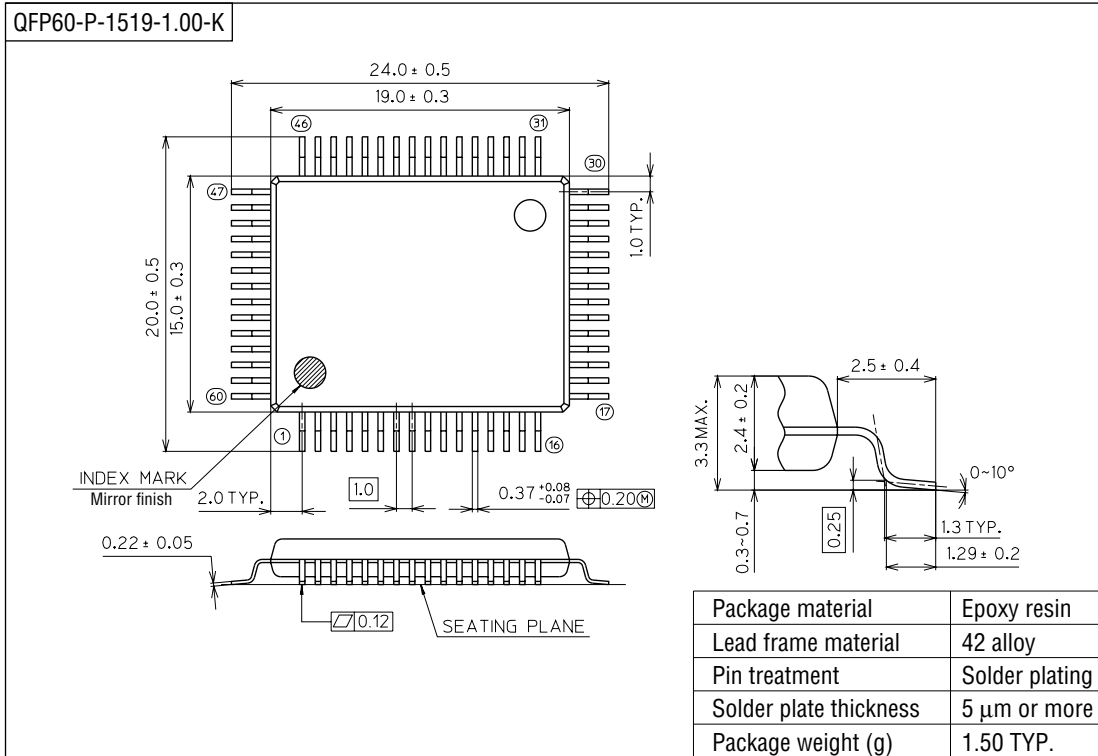
($V_{DD1}=3$ to 5.5 V, $T_a=-40$ to $+85^\circ\text{C}$ unless otherwise specified)

Parameter	Symbol	Condition	Min.	Max.	Unit
OSC Clock Pulse Width	$t_{OSC W}$	—	500	—	ns
OSC Clock Cycle	t_{OSC}	—	1	—	μs
Input Data Setup Time	t_{SU}	$V_{DD1}=4.5$ to 5.5 V	200	—	ns
Input Data Hold Time	t_{HL}	$V_{DD1}=4.5$ to 5.5 V	300	—	ns
Output Data Delay Time	t_D	$V_{DD1}=4.5$ to 5.5 V, $C_I=30$ pF	—	400	ns
P0.1 External Interrupt Pulse Width	t_{WP01}	—	$15 t_{OSC}$	—	ns
Reset Pulse Width	t_{WRES}	—	$6 t_{OSC}$	—	ns



PACKAGE DIMENSIONS

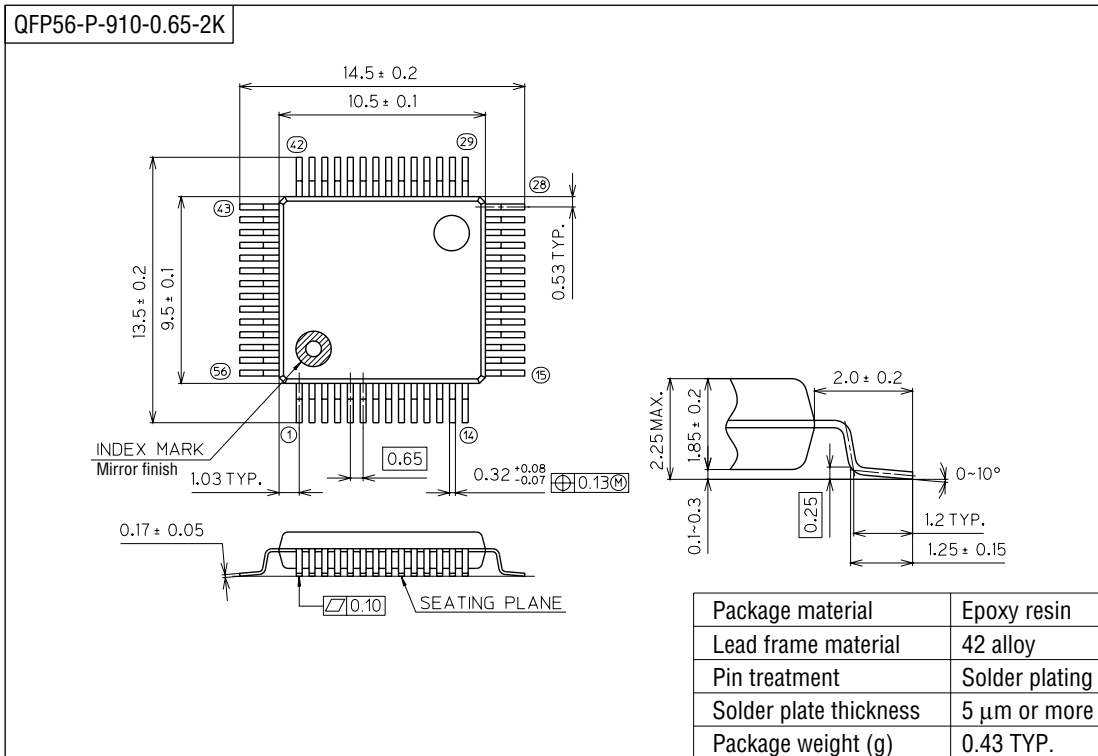
(Unit : mm)



Notes for Mounting the Surface Mount Type Package

The SOP, QFP, TSOP, SOJ, QFJ (PLCC), SHP and BGA are surface mount type packages, which are very susceptible to heat in reflow mounting and humidity absorbed in storage. Therefore, before you perform reflow mounting, contact Oki's responsible sales person for the product name, package name, pin number, package code and desired mounting conditions (reflow method, temperature and times).

(Unit : mm)



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