

## DVI / HDMI Re-Driver w/ Equalization, De-emphasis & Pre-emphasis

**Features**

- Supply voltage,  $V_{DD} = 3.3V \pm 5\%$
- Compatible with DVI, HDMI, rev 1.1, 1.2, and 1.3 signals
- Supports both AC-coupled and DC-coupled inputs
- 8-Bit, 10-Bit, and 12-Bit deep color support
- Configurable output swing control (500mV, 750mV, 1000mV)
- Configurable Pre-Emphasis levels (0dB, 1.5dB, 3.5dB, & 6.0dB)
- Configurable De-Emphasis (0dB, -1.5dB, -3.5dB, -6.0dB)
- Configurable Equalization (1dB, 3.5dB, 8dB, Optimized EQ)
- Data Rate = 2.5 Gbps (max)
- ESD protection = 6kV (Typical)
- Inputs w/ built-in termination per HDMI spec
- Propagation delay < 2ns input
- Uni-Directional
- Packaging (Pb-free & Green): 56-contact TQFN (ZB56)

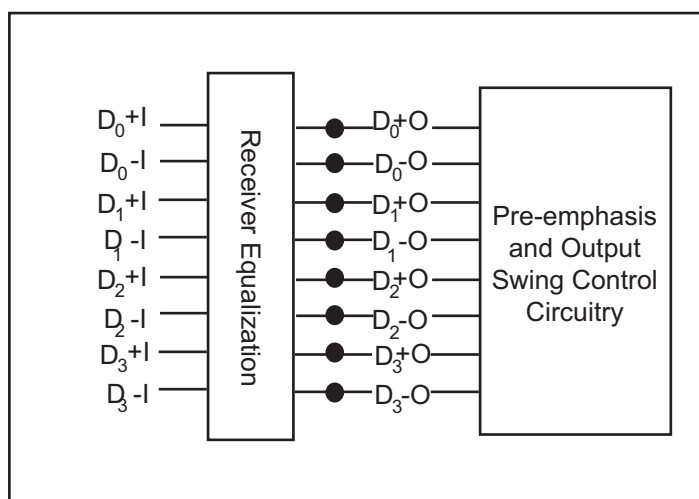
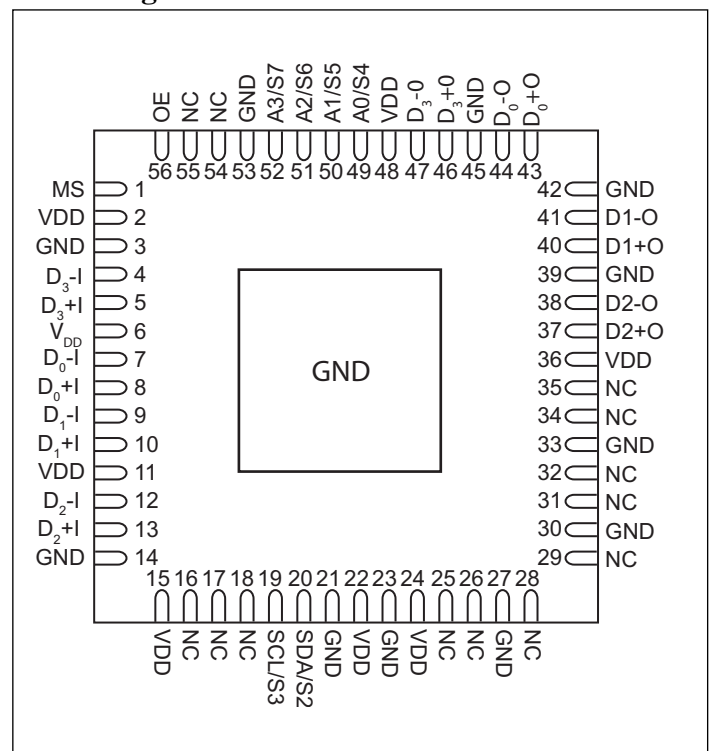
**Description**

Pericom Semiconductor's PI3HDMI411AD, active-drive switch solution is targeted for high-resolution video networks that are based on DVI/HDMI standards, and TMDS signal processing. The PI3HDMI411AD is an active single TMDS channel re-driver with Hi-Z outputs. The device drives differential signals with enhanced signal integrity to video display units. It provides three controllable output swing levels that can be controlled through pin control or I<sup>2</sup>C control, depending on the mode select pin. The swing levels are 500mV, 700mV, & 1000mV. This solution also provides a unique advanced pre-emphasis technique to increase rise and fall times which are reduced during transmission across long distances.

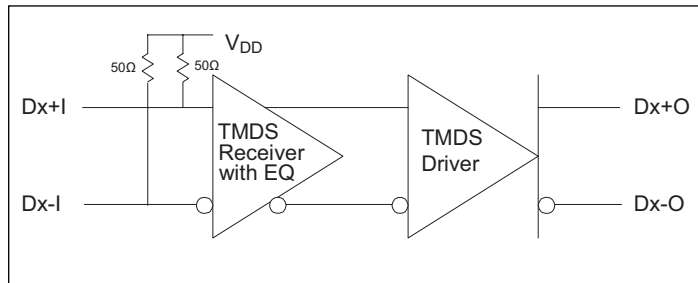
The maximum DVI/HDMI data rate of 2.5Gbps provides a 1920x1080 resolution required w/ 12 bit/channel color depth, by the next Gen HDTV and PC graphics products.

PI3HDMI411AD is the industry's first active DVI/HDMI compliant switch, which ensures transmitting high bandwidth video streams from PC graphics source to end display units.

The Optimized Equalization provides the user a single optimal setting that can provide HDMI compliance for all cable lengths: 2meter, 10meter, 15meter, and 20 meter. Pericom also offers the ability to fine tune the equalization settings in situations where cable length is known.

**Block Diagram**

**Pin Configuration**


### Function Block Description



**Notes:**

1. X = 0,1,2,3

### Maximum Ratings

(Above which useful life may be impaired. For user guidelines, not tested.)

Storage Temperature.....	-65°C to +150°C
Supply Voltage to Ground Potential.....	-0.5V to +5V
DC Input Voltage.....	-0.5V to V <sub>DD</sub>
DC Output Current.....	120mA
Power Dissipation.....	1.0W

**Note:**

Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

### Pin Description

Pin #	Pin Name	I/O	Description
2, 6, 11, 15, 22, 24, 36, 48	V <sub>DD</sub>	Power	3.3V power supply
3, 14, 21, 23, 27, 30, 33, 39, 42, 45, 53	GND	Power	0V power supply
19	SCL	I	I2C Clock Input Signal, if and only if MS = 'HIGH'
20	SDA	I/O	I2C Data Input/Output Signal, if and only if MS = 'HIGH'
1	MS	I	Mode Select Pin. If MS = 'HIGH', then I2C control is active. Pins 49-52 are I2C address and pin 19 is SCL and pin 20 is SDA. If MS = 'LOW', then I2C control is inactive and pin programmability is active.
56	OE	I	Output is enabled and normal when OE = 'HIGH'. If OE = 'LOW', both outputs, A and B, are disabled and at Hi-Z
4, 5, 7, 8, 9, 10, 12, 13	DxI, CLKI	I	Input TMDS high speed signals
37, 38, 40, 41, 43, 44, 46, 47	DxO, CLKO	O	Output TMDS high speed signals
49, 50, 51, 52	A0, A1, A2, A3	I	I2C address inputs if MS = 'HIGH'.
49, 50, 51, 52	S4, S5, S6, S7	I	If MS = 'LOW', then pins 49-52 are control bits S4-S7 for output port only, as shown in truth table on page 3 of datasheet
19	S3	I	If MS = 'LOW', then pins 19 is control bit S3, as shown in the truth table on page 3
20	S2	I	If MS = 'LOW', then pins 20 is control bit S2, as shown in the truth table on page 3
16, 17, 18, 25, 26, 28, 29, 31, 32, 34, 35, 54, 55	NC	N/A	No Connect

**BYTE 1 (Address Assignment)**

Address	A6	A5	A4	A3	A2	A1	A0	R/W
Value	1	1	0	A3	A2	A1	A0	R=1/W=0

**BYTE 2 (1st Data byte - Port output control)**

Output Control Only	S7	S6	S5	S4	S3	S2	S1	S0	Result		
									Swing (mV)	Pre-Emphasis (dB)	De-Emphasis (dB)
Swing Control	0	0	0	0	x	x	x	x	500	0	0
	0	0	0	1	x	x	x	x	750	0	0
	0	0	1	0	x	x	x	x	1000	0	0
	0	0	1	1	x	x	x	x	N/A	N/A	N/A
Pre-Emphasis	0	1	0	0	x	x	x	x	500	0	0
	0	1	0	1	x	x	x	x	500	1.5	0
	0	1	1	0	x	x	x	x	500	3.5	0
	0	1	1	1	x	x	x	x	500	6.0	0
De-Emphasis	1	0	0	0	x	x	x	x	750	0	0
	1	0	0	1	x	x	x	x	750	0	-1.5
	1	0	1	0	x	x	x	x	750	0	-3.5
	1	0	1	1	x	x	x	x	750	0	-6.0

**BYTE 3 (2nd Data byte - Port input control)**

Input Control Only	S7	S6	S5	S4	S3	S2	S1	S0	Result
Equalization (dB)	x	x	x	x	0	0	x	x	1
	x	x	x	x	0	1	x	x	3.5
	x	x	x	x	1	0	x	x	Optimized EQ Setting
	x	x	x	x	1	1	x	x	8



### TMDS Compliance Test Results

Item	HDMI 1.3 Spec	Pericom TMDS Product Spec
<b>Operating Conditions</b>		
Termination Supply Voltage, $A_{VDD}$	$3.3V \leq 5\%$	$3.30 \pm 5\%$
Terminal Resistance	$50\text{-ohm} \leq 10\%$	45 to 55-ohm
<b>Source DC Characteristics at TP1</b>		
Single-ended high level output voltage, $V_H$	$A_{VDD} \leq 10mV$	$A_{VDD} \leq 10mV$
Single-ended low level output voltage, $V_L$	$(A_{VDD} - 600mV) \leq V_L \leq (A_{VDD} - 400mV)$	$(A_{VDD} - 600mV) \leq V_L \leq (A_{VDD} - 400mV)$
Single-ended output swing voltage, $V_{swing}$	$400mV \leq V_{swing} \leq 600mV$	$400mV \leq V_{swing} \leq 600mV$
Single-ended standby (off) output voltage, $V_{off}$	$A_{VDD} \pm 10mV$ (informative)	$A_{VDD} \pm 10mV$
Single-ended standby (off) output current, $I_{off}$	$ I_{OFF}  < 100\mu A$	$ I_{OFF}  < 10\mu A$
<b>Transmitter AC Characteristics at TP1</b>		
Risetime/Falltime (20%-80%)	$75ps \leq \text{Risetime/Falltime} \leq 0.4 \text{ Tbit}$ ( $75ps \leq tr/tf \leq 242ps$ ) @ 1.65Gbps	240ps
Intra-Pair Skew at Transmitter Connector, max	0.15 Tbit (90.9ps @ 1.65Gbps)	60ps max
Inter-Pair Skew at Transmitter Connector, max	0.2 Tpixel (1.2ns @ 1.65Gbps)	100ps max
Clock Jitter, max	0.25 Tbit (151.5ps @ 1.65Gbps)	82ps max
<b>Sink Operating DC Characteristics at TP2</b>		
Input Differential Voltage Level, $V_{diff}$	$150 \leq V_{diff} \leq 1200mV$	$150mV \leq V_{DIFF} \leq 1200mV$
Input Common Mode Voltage Level, $V_{ICM}$	$100\Omega \pm 15\Omega$	$A_{VDD} - 300mV \leq V_{ICM} < A_{VDD} - 37.5mV$ or $A_{VDD} \pm 10\%$
<b>Sink DC Characteristics When Source Disabled or Disconnected at TP2</b>		
Differential Voltage Level	$A_{VDD} \pm 10mV$	$A_{VDD} \pm 10mV$



**DC Electrical Characteristics** ( $T_A = -40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$ , unless otherwise noted.  $V_{DD} = 3.3\text{V} \pm 0.3\text{V}$ )

Symbol	Parameter	Test Condition <sup>(1)</sup>	Min.	Typ. <sup>(2)</sup>	Max.	Units
$V_H$	Single-ended high level output voltage		$V_{DD} - 10\text{mV}$	$V_{DD}$	$V_{DD} + 10\text{mV}$	V
$V_L$	Single-ended low level output voltage		$V_{DD} - 600\text{mV}$		$V_{DD} - 400\text{mV}$	V
$V_{\text{swing}}$	Single-ended output swing voltage		400		600	mV
$V_{\text{OFF}}$	Single-ended standby (off) output voltage		$V_{DD} - 10\text{mV}$	$V_{DD}$	$V_{DD} + 10\text{mV}$	V
$I_{\text{OFF}}$	Single-ended standby (off) output current				10	$\mu\text{s}$
$V_{\text{OS}}$	Offset Voltage				$V_{DD} - 250\text{mV}$	V
$V_{\text{IH}}$	Minimum Input High Voltage		1.8			V
$V_{\text{IL}}$	Minimum Input Low Voltage				0.8	
$I_{\text{CC}}$	Power Supply Current				280	mA

**AC Electrical Characteristics** ( $T_A = -40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$ ,  $V_{DD} = 3.3\text{V} \pm 0.3\text{V}$ )

Symbol	Parameter	Test Conditions <sup>(1)</sup>	Min.	Typ. <sup>(2)</sup>	Max.	Units
$T_{20-80}$	Rise time/fall time (20% - 80%)		75		$0.4 T_{\text{bit}}$	Ps
	Overshoot				15% of $V_{\text{swing}} * 2$	
	Undershoot				25% of $V_{\text{swing}} * 2$	
	Intra-Pair Skew at Source Connector				60	ps
	Inter-Pair Skew at Connector				100	ps
	Clock duty cycle		40%	50%	60%	
	TMDS differential clock Jitter				62	ps
$t_{\text{PHLD}}$	Differential Propagation Delay High to Low			1		ns
$t_{\text{PLHD}}$	Differential Propagation Delay Low to High			1		ns
$t_{\text{SKD}}$	Differential Skew   $t_{\text{PHLD}} - t_{\text{PLHD}}$			25		ps
$t_{\text{PHZ}}$	Disable Time High to Z			5		ns
$t_{\text{PLZ}}$	Disable Time Low to Z			5		
$t_{\text{PZH}}$	Enable Time Z to High			1		$\mu\text{s}$
$t_{\text{PZL}}$	Enable Time Z to Low			1		

**Notes:**

- For Max. or Min. conditions, use appropriate value specified under Electrical Characteristics for the applicable device type.
- Typical values are at  $V_{DD} = 3.3\text{V}$ ,  $T_A = 25^{\circ}\text{C}$  ambient and maximum loading.

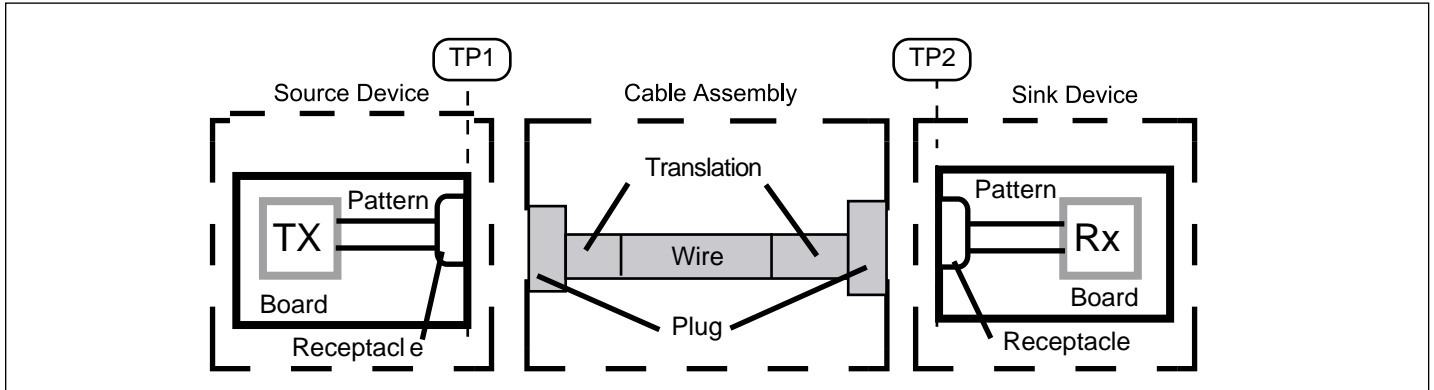
**Power Supply Characteristics**

Parameters	Description	Test Conditions <sup>(1)</sup>	Min.	Typ. <sup>(2)</sup>	Max.	Units
$I_{\text{CC}}$	Quiescent Power Supply Current	$V_{DD} = \text{Max.}, V_{\text{IN}} = V_{DD}, \text{OE} = \text{'LOW'}$		1		mA

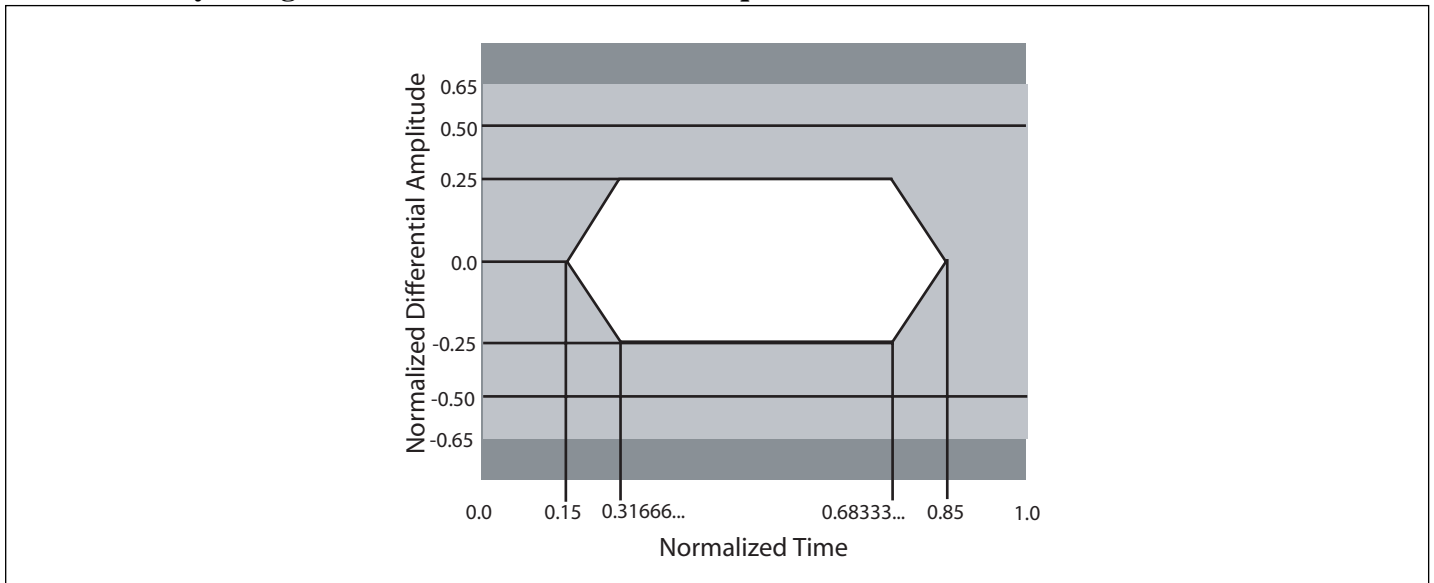
**Notes:**

- For Max. or Min. conditions, use appropriate value specified under Electrical Characteristics for the applicable device type.
- Typical values are at  $V_{DD} = 3.3\text{V}$ ,  $T_A = 25^{\circ}\text{C}$  ambient and maximum loading.

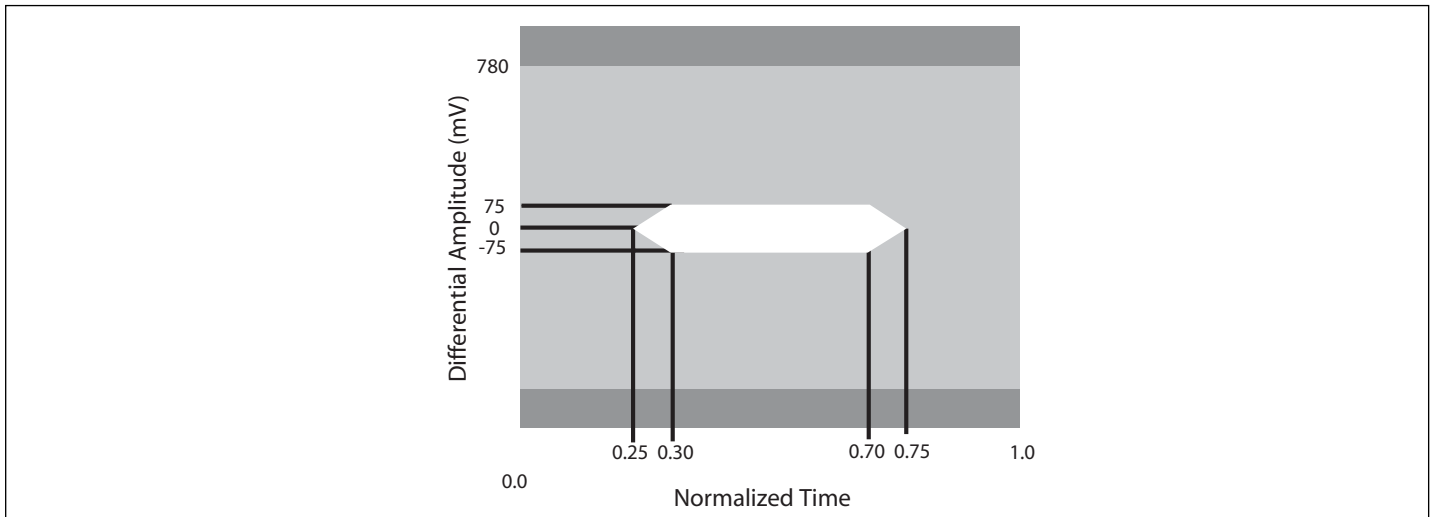
### TMDS Link Test Points



### Normalized Eye Diagram Mask at TP1 for Source Requirements



### Absolute Eye Diagram Mask at TP2 for Sink Requirements



**Application Information**

PI3HDMI411AD can be used to re-drive HDMI or DVI signals across internal cables or long FR4 trace lengths.

If a DTV is designed with a side/front HDMI connector, a Separate daughter card is needed for the side/front HDMI connector and Pericom re-driver.

ATC compliance MUST only be maintained from the front/side connector to the PI3HDMI411AD IC. After the PI3HDMI411AD signal Integrity will be taken care of through the powerful pre-emphasis technique of the Pericom solution.

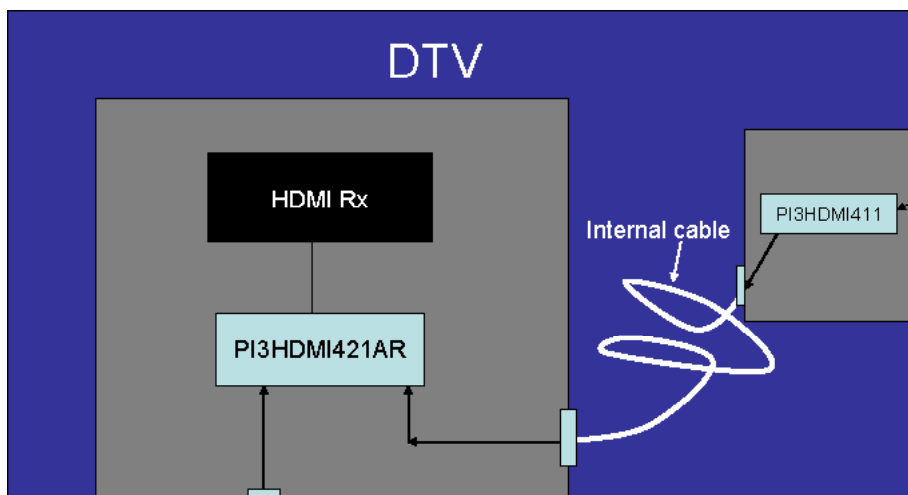


Figure 1: DTV with 2 HDMI connectors (1 HDMI in back & 1 HDMI on the side)

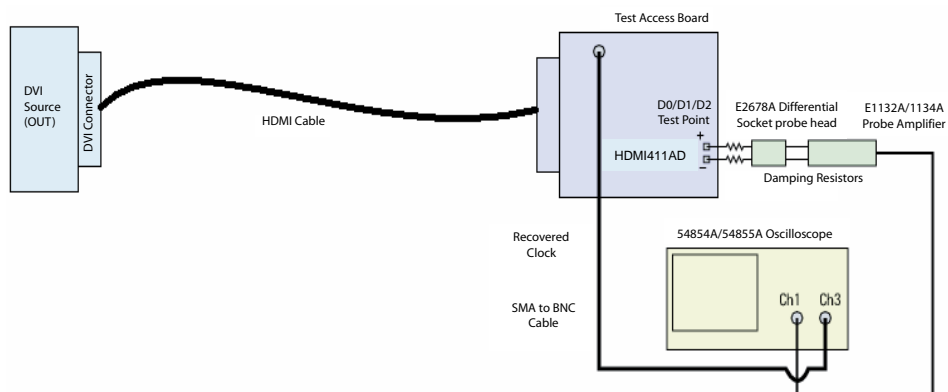


Figure 2: Signal integrity analysis test setup



Figure 3: 8bit deep color DVI/HDMI TX eye tested with 2 meter. 30 AWG HDMI cable. Setting: Optimized equalization, 0dB output pre-emphasis and de-emphasis, and Swing 500mV.

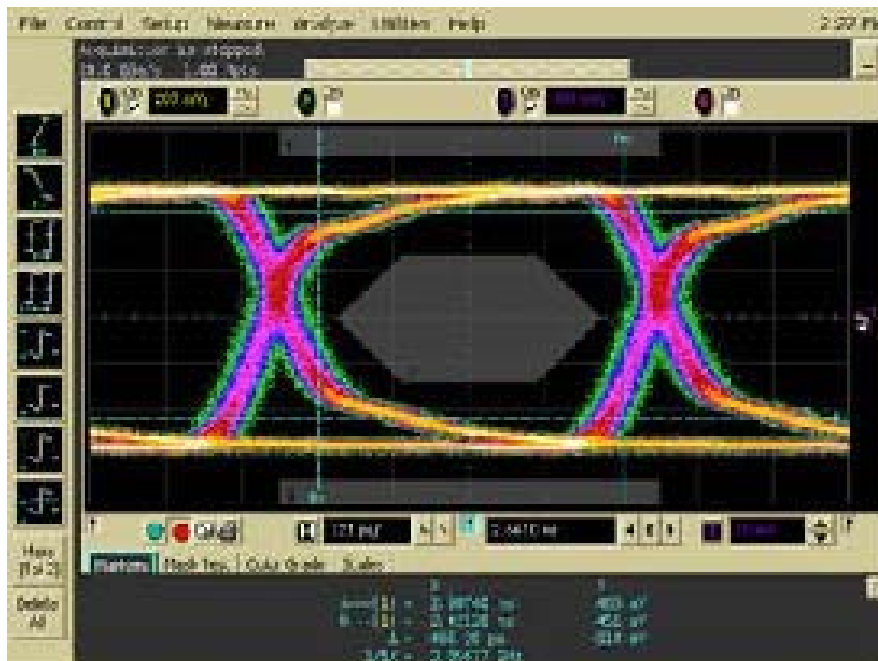
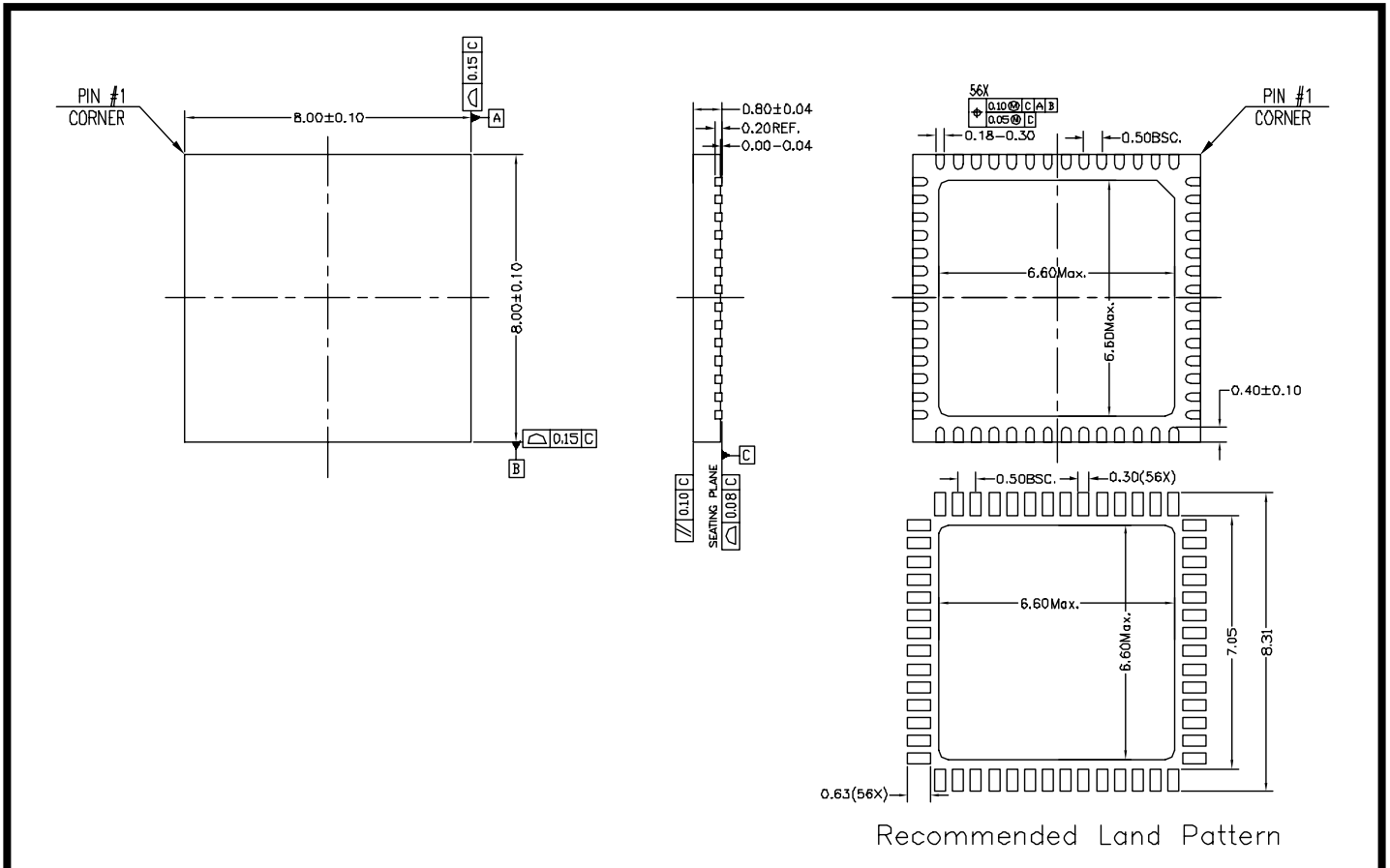



Figure 4: 8bit deep color DVI/HDMI TX eye tested with 20 meter. 24 AWG HDMI cable. Setting: Optimized equalization, 0dB output pre-emphasis and de-emphasis, and Swing 500mV.





**Notes:**

- 1) All dimensions are in millimeters, angles in Degrees.
- 2) Bilateral coplanarity zone applies to the exposed heat sink slug as well as the terminals.
- 3) Refer JEDEC MO-220 modified
- 4) Thermal Via Diameter. Recommended 0.2~0.33mm
- 5) Thermal Via Pitch. Recommended 1.27mm

	DATE: 02/17/06
DESCRIPTION: 56-contact, Thin Fine Pitch Quad Flat No-lead (TQFN)	
PACKAGE CODE: ZB56	
DOCUMENT CONTROL #: PD-2008	REVISION: C

**Ordering Information**

Ordering Code	Package Code	Package Description
PI3HDMI411ADZBE	ZB	56-pin, Pb-free & Green, TQFN, (ZB56)

**Notes:**

- Thermal characteristics can be found on the company web site at [www.pericom.com/packaging/](http://www.pericom.com/packaging/)
- E = Pb-free and Green
- Adding an X suffix = Tape/Reel