AH225

1W High Linearity InGaP HBT Amplifier

Applications

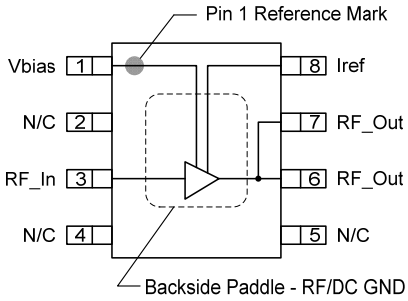
- Repeaters
- Base Station Transceivers
- High Power Amplifiers
- Mobile Infrastructure
- LTE / WCDMA / CDMA / WiMAX

SOIC-8 Package

Product Features

- 400-2700 MHz
- 15.5 dB Gain at 2140 MHz
- +31 dBm P1dB
- +46 dBm Output IP3
- 300 mA Quiescent Current
- +5 V Single Supply
- MTTF > 100 Years
- Lead-free/RoHS-compliant SOIC-8 Package

Functional Block Diagram



General Description

The AH225 is a high dynamic range driver amplifier in a low-cost surface-mount package. The InGaP/GaAs HBT is able to achieve high performance for various narrowband-tuned application circuits with up to +46 dBm OIP3 and +31.2 dBm of compressed 1dB power. The integrated active bias circuitry in the devices enables excellent stable linearity performance over temperature. It is housed in a lead-free/RoHS-compliant SOIC-8 package. All devices are 100% RF and DC tested.

The AH225 is targeted for use as a driver amplifier in wireless infrastructure where high linearity and medium power is required. The AH225 is ideal for the final stage of small repeaters or as driver stages for high power amplifiers. In addition, the amplifier can be used for a wide variety of other applications within the 400 to 2700 MHz frequency band.

Pin Configuration

Pin #	Symbol
1	Vbias
2, 4, 5	N/C
3	RF_in
6, 7	RF_Out
8	Iref
Backside Paddle	RF/DC GND

Ordering Information

Part No.	Description
AH225-S8G	1W High Linearity Amplifier
AH225-S8PCB900	920-960 MHz Evaluation Board
AH225-S8PCB1960	1930-1960 MHz Evaluation Board
AH225-S8PCB2140	2110-2170 MHz Evaluation Board

Standard T/R size = 1000 pieces on a 7" reel.

Specifications

Absolute Maximum Ratings

Parameter	Rating
Storage Temperature	-65 to 150 °C
RF Input Power, CW, 50Ω, T=25°C	+26 dBm
Device Voltage, V_{cc}, V_{bias}	+8 V
Device Current	900 mA
Device Power	+5 W

Operation of this device outside the parameter ranges given above may cause permanent damage.

Recommended Operating Conditions

Parameter	Min	Typ	Max	Units
V_{cc}	+4.5	+5	+5.25	V
I_{cq}		300		mA
T_{case}	-40		+85	°C
T_J (for >10^6 hours MTTF)			+200	°C

Electrical specifications are measured at specified test conditions. Specifications are not guaranteed over all recommended operating conditions.

Electrical Specifications

Test conditions unless otherwise noted: V_{cc} = +5 V, I_{cq} = 300 mA, T = +25°C, in a tuned application circuit.

Parameter	Conditions	Min	Typical	Max	Units
Operational Frequency Range		400		2700	MHz
Test Frequency			2140		MHz
Gain			15.5		dB
Input Return Loss			18		dB
Output Return Loss			9.4		dB
Output P1dB			+31.2		dBm
Output IP3	See Note 1		+46		dBm
WCDMA Channel Power at -50 dBc ACLR	See Note 2		+21.3		dBm
Noise Figure			6		dB
V_{cc}, V_{bias}			+5		V
Quiescent Current, I_{cq}	See Note 3		300		mA
Iref			15		mA
Thermal Resistance (jnc. to case) θ_{jc}				35	°C/W

Notes:
1. 3OIP measured with two tones at an output power of +19 dBm / tone separated by 1 MHz. The suppression on the largest IM3 product is used to calculate the 3OIP using a 2:1 rule. 2:1 rule gives relative value w.r.t. fundamental tone.
2. 3GPP WCDMA, 1±64DPCH, ±5 MHz, no clipping, PAR = 10.2 dB at 0.01% Probability.
3. This corresponds to the quiescent collector current or operating current under small-signal conditions into pins 6 and 7.

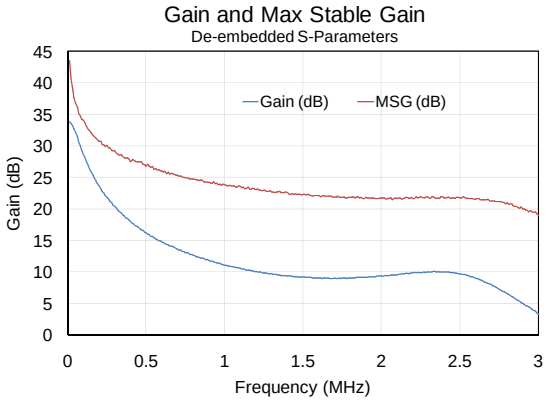
Performance Summary Table

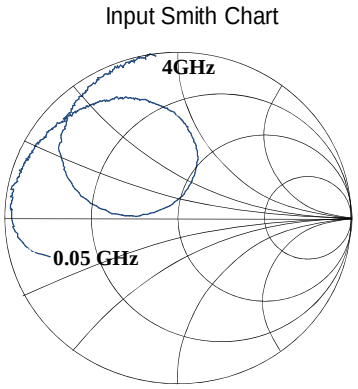
Test conditions unless otherwise noted: V_{cc} = +5 V, I_{cq} = 300 mA, T = +25°C, in an application circuit tuned for each frequency.

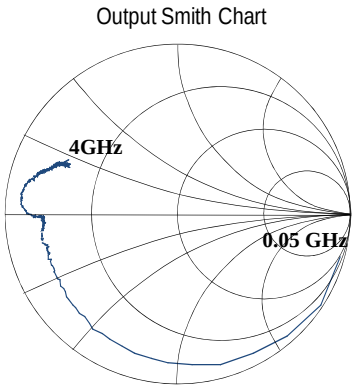
Frequency	750	940	1500	1840	1960	2140	2600	MHz
Gain	20.1	19.8	17	15.1	15.4	15.2	13.2	dB
Input Return Loss	14.5	10.5	17.2	11	15.4	18	19.4	dB
Output Return Loss	7	8.4	11	10.7	8.3	9.4	5.5	dB
Output P1dB	+30.4	+31	+31.3	+30.7	+31.3	+31	+30.5	dBm
Output IP3 [See note 4]	+45	+47.3	+48	+46	+53.6	+47	+48.7	dBm
WCDMA Channel Power at -50 dBc ACLR	+21.2	+21.7	+22	+21.6	+21.7	+21.4	+21.3	dBm

Notes:
4. OIP3 is measured with two tones at an output power of 20 dBm/tone for 750 MHz, 22 dBm/tone for 940 MHz and 19 dBm/tone for 1490, 1840, 1960, 2140, 2600 MHz application circuits respectively.

Device Characterization Data







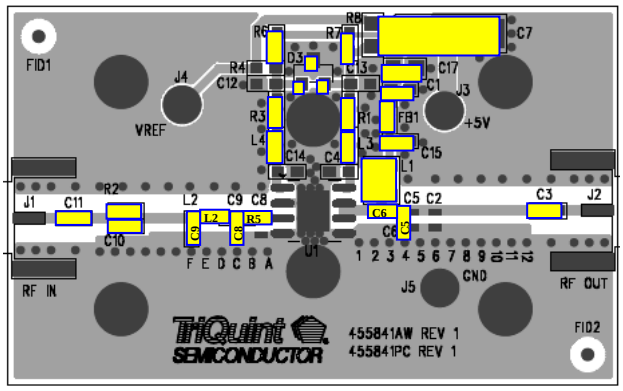
Note: The gain for the unmatched device in 50 ohm system is shown as the trace in blue color, Gain (dB). For a tuned circuit for a particular frequency, it is expected that actual gain will be higher, up to the maximum stable gain. The maximum stable gain is shown in the red line, DB [MSG]. The impedance loss plots are shown from 0.05-4 GHz.

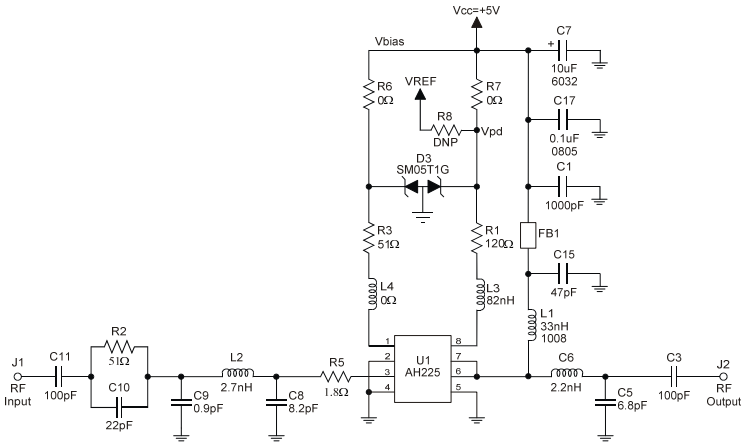
S-Parameter Data

V_{cc} = +5 V, I_{cq} = 300 mA, T = +25°C, unmatched 50 ohm system, calibrated to device leads

Freq (MHz)	S11 (dB)	S11 (ang)	S21 (dB)	S21 (ang)	S12 (dB)	S12 (ang)	S22 (dB)	S22 (ang)
50	-2.90	-165.27	32.12	136.60	-40.91	46.68	-0.94	-74.85
100	-1.57	-171.34	28.59	116.71	-38.86	31.54	-1.66	-113.38
200	-0.99	179.84	23.57	100.17	-37.78	17.25	-1.95	-143.44
400	-0.81	169.25	17.96	86.66	-37.58	7.00	-2.15	-162.82
800	-0.97	152.64	12.56	69.77	-36.47	-0.03	-2.08	-173.99
1000	-1.12	145.10	11.02	62.27	-36.53	-6.84	-2.19	-175.67
1200	-1.25	136.77	10.01	54.20	-35.91	-8.53	-2.20	-177.71
1400	-1.53	128.95	9.29	46.48	-35.54	-14.78	-2.19	-178.63
1800	-2.52	110.16	8.93	27.07	-34.79	-32.76	-2.20	-179.60
2100	-4.69	91.38	9.54	5.44	-33.84	-58.32	-1.92	-179.47
2000	-3.69	98.77	9.27	13.27	-34.06	-50.56	-2.01	179.89
2200	-6.45	86.18	9.79	-4.317	-33.35	-72.56	-1.80	179.99
2400	-13.76	87.27	10.01	-28.04	-33.51	-107.65	-1.25	179.43
2600	-10.27	171.20	8.85	-57.83	-34.02	-157.07	-0.81	175.18
2800	-4.15	159.31	6.56	-84.16	-35.29	156.89	-0.78	171.95
3000	-1.93	143.93	3.19	-104.79	-34.70	116.80	-0.99	167.43

Reference Design 700-850 MHz





Notes:

1. See PC Board Layout, page 20 for more information.
2. Vref J4 turret can be used as control voltage for device power down (low = RF off) by setting R8 = 0 Ω and R7 = no connect.
3. The primary RF microstrip characteristic line impedance is 50 Ω.
4. Do not exceed +5.5V on Vpd or Vcc or TVS diode D3 will be damaged.
5. Components shown on the silkscreen but not on the schematic are not used.
6. The edge of C6 is placed at 70 mils from the edge of AH225 RFout pin (3° at 750 MHz).
7. C5 is placed against the edge of C6.
8. The edge of R5 is placed at 10 mils from the edge of AH225 RFin pin (0.5° at 750 MHz).
9. C8 is placed against the edge of R5, L2 against C8 and C9 against L2.
10. Zero ohm jumpers may be replaced with copper traces in the target application layout.
11. DNP means Do Not Place.
12. Inductor L3 on Vpd line is critical for linearity performance.
13. The locations of C11, R2, C10 and C3 are non-critical. They can be placed closer to the device.
14. Ferrite Bead FB1 eliminates bypass line resonances between C15 and C1. Steward MI0603K300R-10.
15. All components are of 0603 size unless stated otherwise.

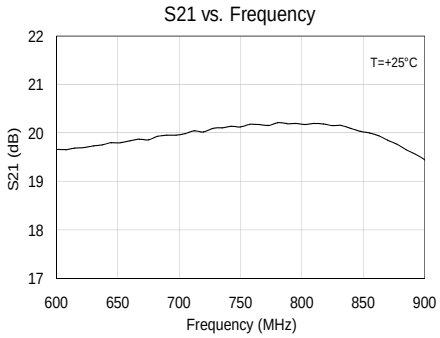
Typical Performance 700-850 MHz

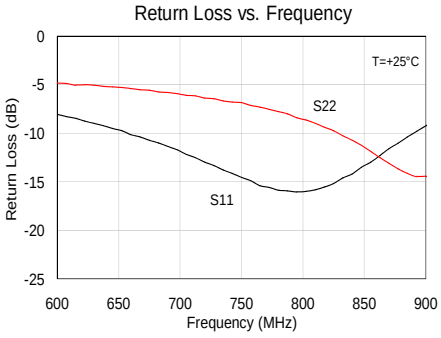
Frequency	MHz	700	750	800	850
Gain	dB	20	20.1	20.2	20
Input Return Loss	dB	12	14.5	16	13.3
Output Return Loss	dB	6	7	8.6	11.5
Output P1dB	dBm	+30.4	+30.4	+30.7	+30.6
Output IP3 at 20 dBm/tone, Δf = 1 MHz	dBm	+44.1	+45	+44.6	+44
WCDMA Channel Power at -50 dBc ACLR [1]	dBm	+20.6	+21.2	+21.4	+21
OFDMA Channel Power at 2.5% EVM [2]	dBm	+22.8	+23.6	+23.3	+23.2
Supply Voltage, Vcc	V	+5			
Quiescent Collector Current, Icq	mA	300			

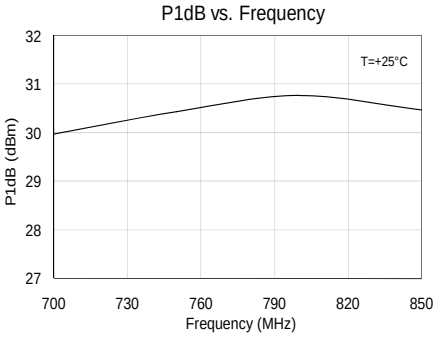
Notes:

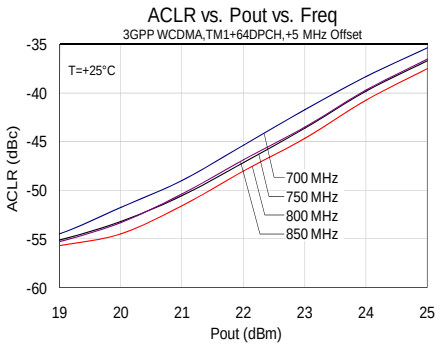
1. ACLR Test set-up: 3GPP WCDMA, TM1+64 DPCH, +5 MHz offset, PAR = 10.2 dB at 0.01% Prob.
2. EVM Test set-up: 802.16 – 2004 OFDMA, 64 QAM – ½, 1024 FFT, 20 symbols, 30 sub channels.

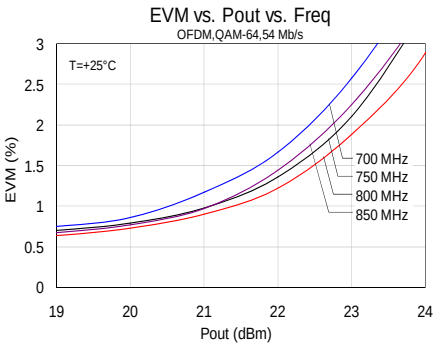
Typical Performance Plots 700-850 MHz

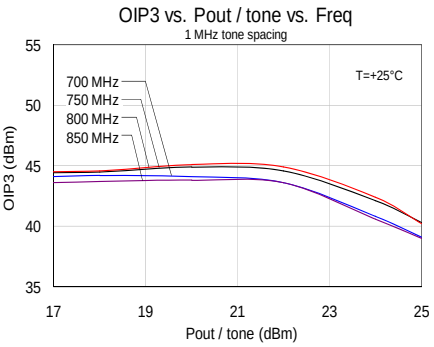




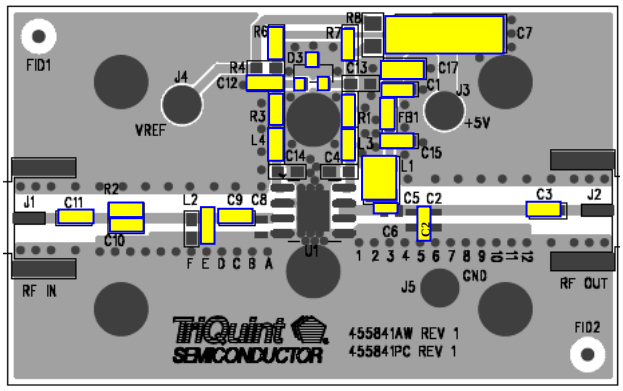


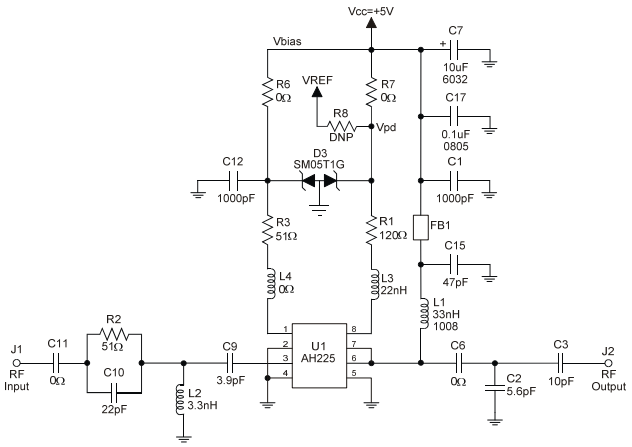






Application Circuit 920-960 MHz (AH225-S8PCB900)





Notes:

1. See PC Board Layout, page 20 for more information.
2. Vref J4 turret can be used as control voltage for device power down (low = RF off) by setting R8 = 0 Ω and R8 = no connect.
3. The primary RF microstrip characteristic line impedance is 50 Ω.
4. Do not exceed +5.5V on Vpd or Vcc or TVS diode D3 will be damaged.
5. Components shown on the silkscreen but not on the schematic are not used.
6. The edge of L2 is placed at 170 mils from the edge of AH225 RFin pin (8.5° at 940 MHz).
7. The edge of C9 is placed at 80 mils from the edge of AH225 RFin pin (4° at 940 MHz).
8. The edge of C2 is placed at 220 mils from the edge of AH225 RFout pin (11° at 940 MHz).
9. Zero ohm jumpers may be replaced with copper traces in the target application layout. C2 location will need to be re-optimized if replaced with copper trace.
10. DNP means Do Not Place.
11. Inductor L3 on Vpd line is critical for linearity performance.
12. The locations of C11, R2, C10 and C3 are non-critical. They can be placed closer to the device.
13. Ferrite Bead FB1 eliminates bypass line resonances between C15 and C1. Steward MI0603K300R-10.
14. All components are of 0603 size unless stated otherwise.

Typical Performance 920-960 MHz

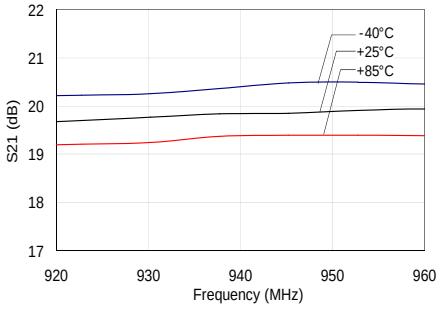
Frequency	MHz	920	940	960
Gain	dB	19.7	19.8	19.9
Input Return Loss	dB	9.6	10.5	10.4
Output Return Loss	dB	8	8.4	9
Output P1dB	dBm	+31.1	+31	+31.1
Output IP3 at 22 dBm/tone, Δf = 1 MHz	dBm	+46.2	+47.3	+48
WCDMA Channel Power at -50 dBc ACLR [1]	dBm	+21.6	+21.7	+21.6
Noise Figure	dB	9.3	9.2	9.3
Supply Voltage, Vcc	V		+5	
Quiescent Collector Current, Icq	mA		300	

Notes:

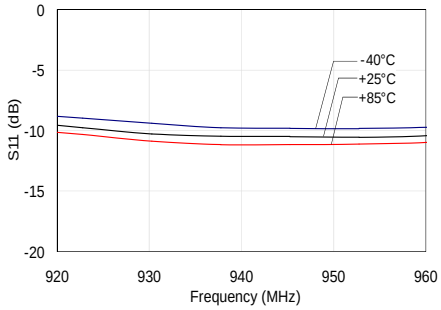
1. ACLR Test set-up: 3GPP WCDMA, TM1+64 DPCH, +5 MHz offset, PAR = 10.2 dB at 0.01% Prob.

Typical Performance Plots 920-960 MHz

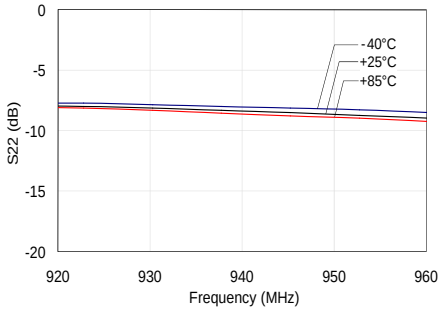
S21 vs. Frequency



S11 vs. Frequency

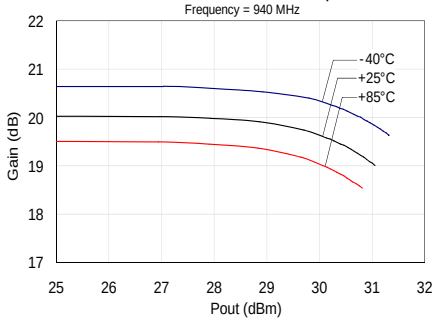


S22 vs. Frequency



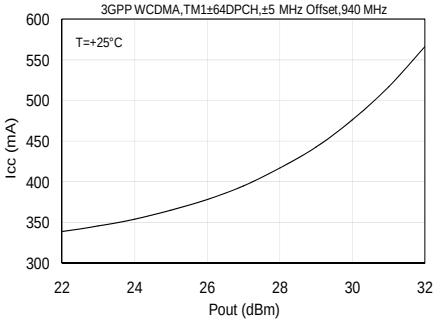
Gain vs. Pout vs. Temp

Frequency = 940 MHz

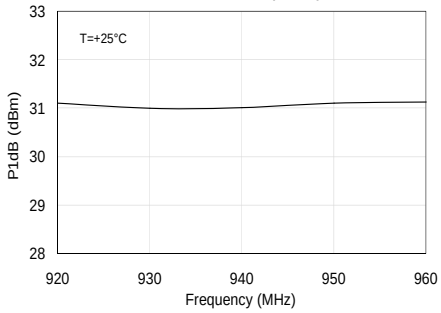


Icc vs. Pout

3GPP WCDMA,TM1±64DPCH,±5 MHz Offset,940 MHz

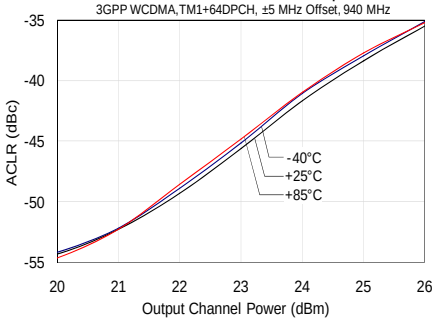


P1dB vs. Frequency



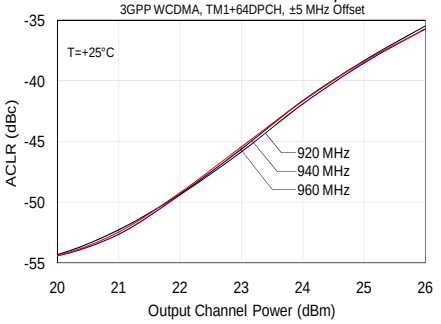
ACLR vs. Pout vs. Temp

3GPP WCDMA,TM1+64DPCH, ±5 MHz Offset, 940 MHz

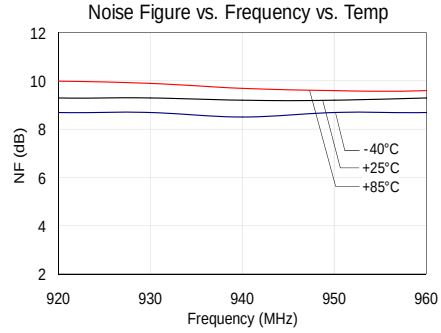


ACLR vs. Pout vs. Freq

3GPP WCDMA, TM1+64DPCH, ±5 MHz Offset

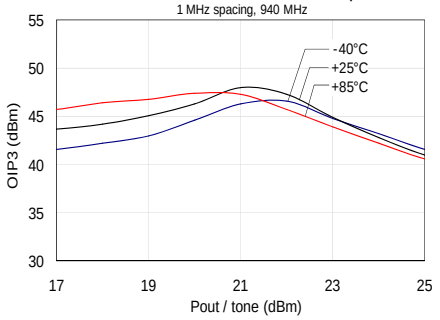


Noise Figure vs. Frequency vs. Temp



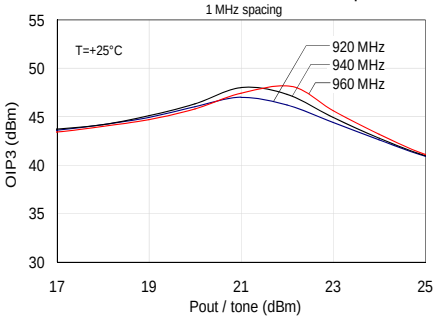
OIP3 vs. Pout/Tone vs. Temp

1 MHz spacing, 940 MHz



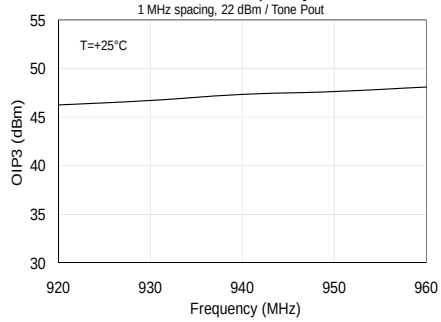
OIP3 vs. Pout/Tone vs. Freq

1 MHz spacing

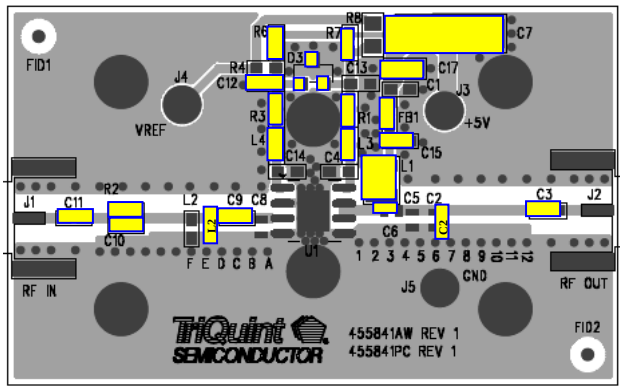


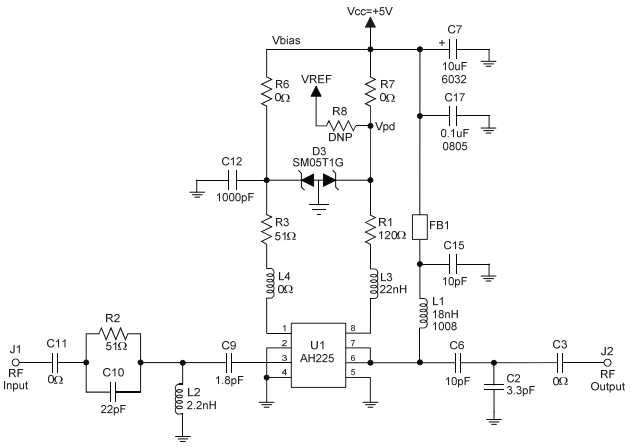
OIP3 vs. Frequency

1 MHz spacing, 22 dBm / Tone Pout



Reference Design 1475-1510 MHz





Notes:

1. See PC Board Layout, page 20 for more information.
2. Vref J4 turret can be used as control voltage for device power down (low = RF off) by setting R8 = 0 Ω and R8 = no connect.
3. The primary RF microstrip characteristic line impedance is 50 Ω.
4. Do not exceed +5.5V on Vpd or Vcc or TVS diode D3 will be damaged.
5. Components shown on the silkscreen but not on the schematic are not used.
6. The edge of L2 is placed against the edge of C9.
7. The edge of C9 is placed at 75 mils from the edge of AH225 RFin pin (6° at 1490 MHz).
8. The edge of C2 is placed at 300 mils from the edge of AH225 RFout pin (24° at 1490 MHz).
9. Zero ohm jumpers may be replaced with copper traces in the target application layout.
10. DNP means Do Not Place.
11. Inductor L3 on Vpd line is critical for linearity performance.
12. The locations of C11, R2, C10 and C3 are non-critical. They can be placed closer to the device.
13. Ferrite Bead FB1 eliminates bypass line resonances between C15 and C1. Steward MI0603K300R-10.
14. All components are of 0603 size unless stated otherwise.

Typical Performance 1475-1510 MHz

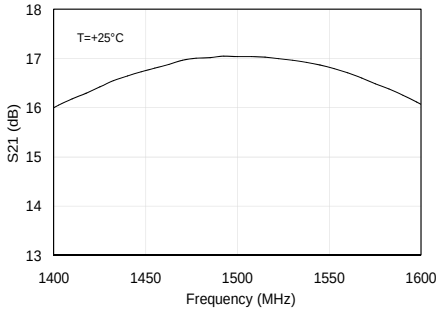
Frequency	MHz	1475	1490	1510
Gain	dB	17	17	17
Input Return Loss	dB	17.5	17.2	15.2
Output Return Loss	dB	10	11	13
Output P1dB	dBm	+31.4	+31.3	+31
Output IP3 at 19 dBm/tone, Δf = 1 MHz	dBm	+47.6	+48	+47
WCDMA Channel Power at -50 dBc ACLR [1]	dBm	+22	+22	+21.8
OFDMA Channel Power at 2.5% EVM [2]	dBm	+23.9	+23.9	+23.7
Supply Voltage, Vcc	V		+5	
Quiescent Collector Current, Icq	mA		300	

Notes:

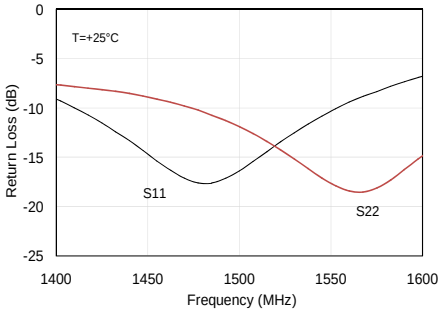
1. ACLR Test set-up: 3GPP WCDMA, TM1+64 DPCH, +5 MHz offset, PAR = 10.2 dB at 0.01% Prob.
2. EVM Test set-up: 802.16 – 2004 OFDMA, 64 QAM – ½, 1024 FFT, 20 symbols, 30 sub channels.

Typical Performance Plots 1475-1510 MHz

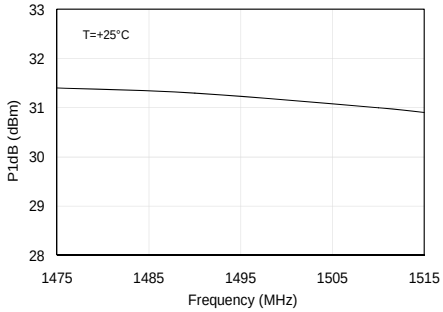
S21 vs. Frequency



Return Loss vs. Frequency

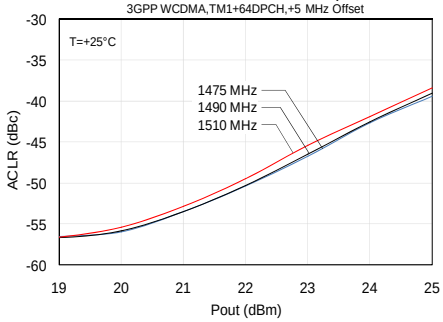


P1dB vs. Frequency



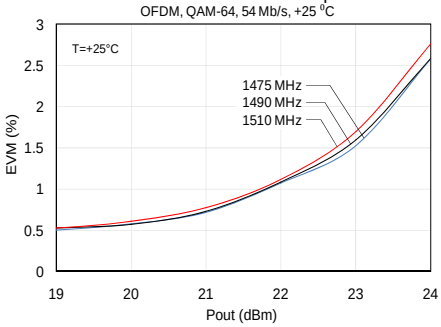
ACLR vs. Pout vs. Freq

3GPP WCDMA,TM1+64DPCH,+5 MHz Offset



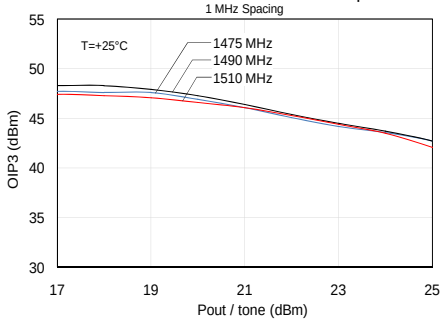
EVM vs. Pout vs. Freq

OFDM, QAM-64, 54 Mb/s, +25 °C

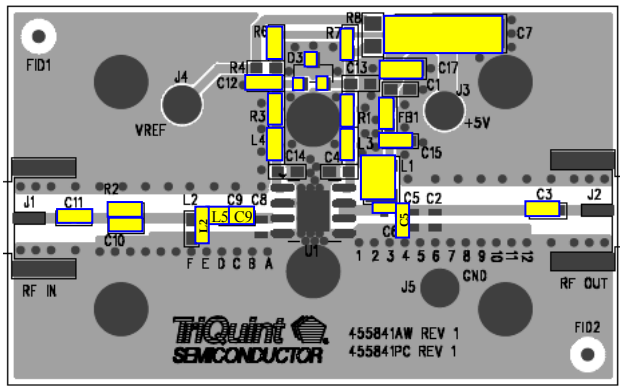


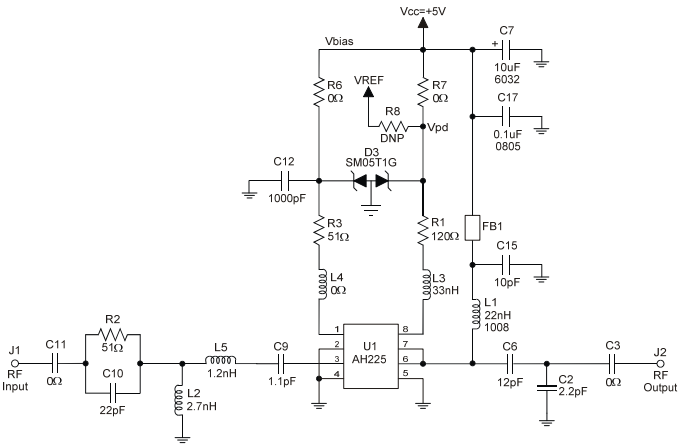
OIP3 vs. Pout / tone vs. Freq

1 MHz Spacing



Reference Design 1805-1880 MHz





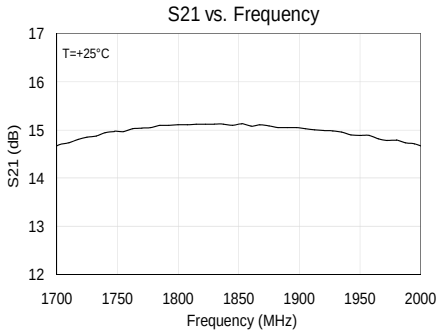
Notes:
1. See PC Board Layout, page 20 for more information.
2. Vref J4 turret can be used as control voltage for device power down (low = RF off) by setting R8 = 0 Ω and R8 = no connect.
3. The primary RF microstrip characteristic line impedance is 50 Ω.
4. Do not exceed +5.5V on Vpd or Vcc or TVS diode D3 will be damaged.
5. Components shown on the silkscreen but not on the schematic are not used.
6. The edge of C9 is placed at 10 mils from the edge of AH225 RFin pin (0.5° at 1840 MHz).
7. The edge of L2 is placed against the edge of L5.
8. The edge of C6 is placed at 80 mils from the edge of AH225 RFout pin (8° at 1840 MHz).
9. The edge of C5 is placed against the edge of C6.
10. Zero ohm jumpers may be replaced with copper traces in the target application layout.
11. DNP means Do Not Place.
12. Inductor L3 on Vpd line is critical for linearity performance.
13. The locations of C11, R2, C10 and C3 are non-critical. They can be placed closer to the device.
14. Ferrite Bead FB1 eliminates bypass line resonances between C15 and C1. Steward MI0603K300R-10.
15. All components are of 0603 size unless stated otherwise.

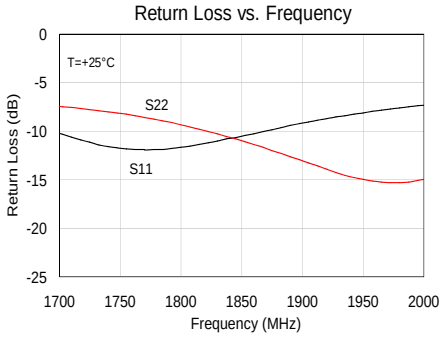
Typical Performance 1805-1880 MHz

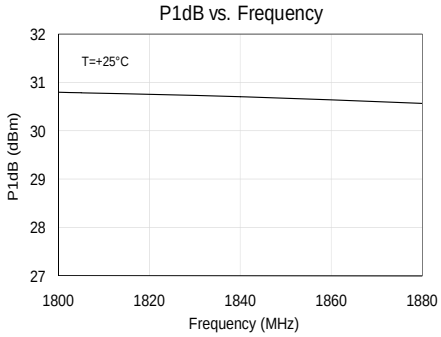
Frequency	MHz	1805	1840	1880
Gain	dB	15.1	15.1	15.1
Input Return Loss	dB	12	11	10
Output Return Loss	dB	9.5	10.7	12
Output P1dB	dBm	+30.8	+30.7	+30.6
Output IP3 at 19 dBm/tone, Δf = 1 MHz	dBm	+46.2	+46	+45
WCDMA Channel Power at -50 dBc ACLR [1]	dBm	+21.7	+21.6	+21.4
OFDMA Channel Power at 2.5% EVM [2]	dBm	+23.6	+23.5	+23.3
Noise Figure	dB	5.7	5.7	5.8
Supply Voltage, Vcc	V		+5	
Quiescent Collector Current, Icq	mA		300	

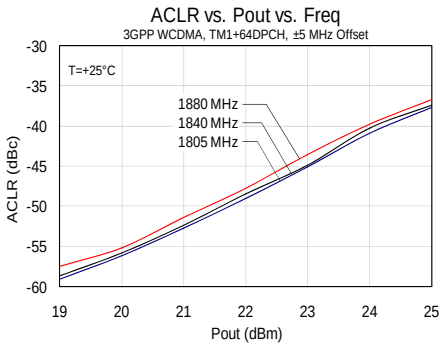
Notes:
1. ACLR Test set-up: 3GPP WCDMA, TM1+64 DPCH, +5 MHz offset, PAR = 10.2 dB at 0.01% Prob.
2. EVM Test set-up: 802.16 – 2004 OFDMA, 64 QAM – ½, 1024 FFT, 20 symbols, 30 sub channels.

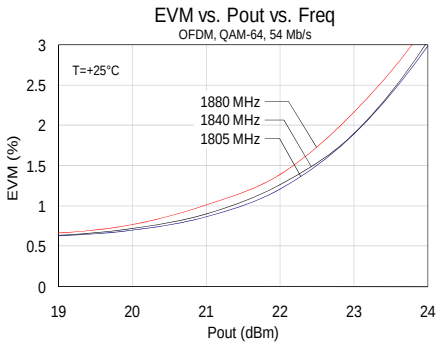
Typical Performance Plots 1805-1880 MHz

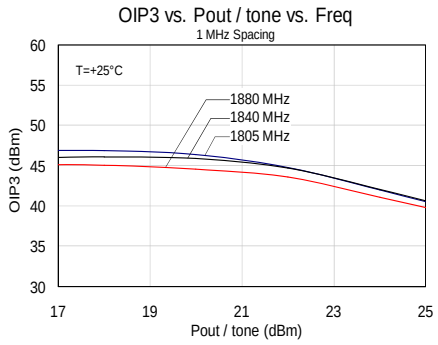




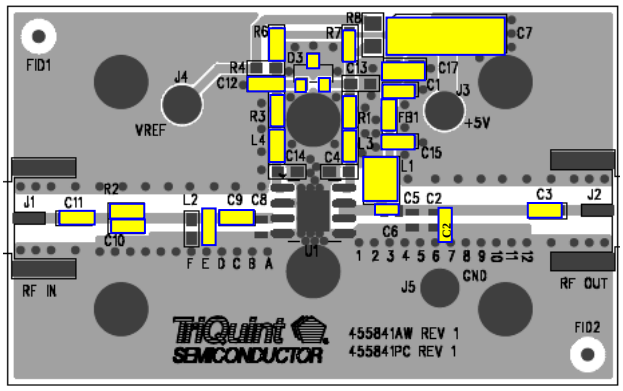


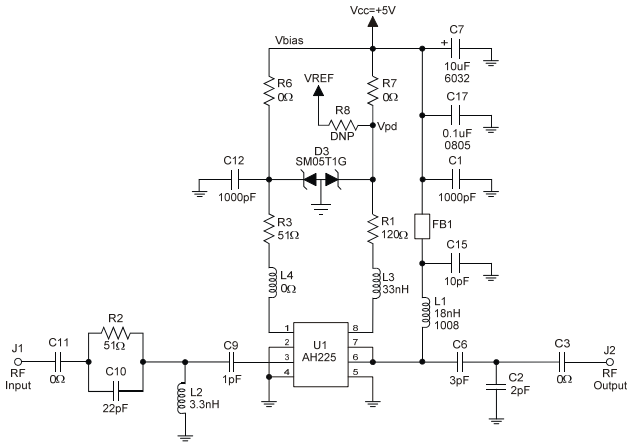






Application Circuit 1930-1990 MHz (AH225-S8PCB1960)





Notes:

1. See PC Board Layout, page 20 for more information.
2. Vref J4 turret can be used as control voltage for device power down (low = RF off) by setting R8 = 0 Ω and R8 = no connect.
3. The primary RF microstrip characteristic line impedance is 50 Ω.
4. Do not exceed +5.5V on Vpd or Vcc or TVS diode D3 will be damaged.
5. Components shown on the silkscreen but not on the schematic are not used.
6. The edge of L2 is placed at 140 mils from the edge of AH225 RFin pin (14.7° 1960 MHz).
7. The edge of C9 is placed at 80 mils from the edge of AH225 RFin pin (8.4° 1960 MHz).
8. The edge of C2 is placed at 315 mils from the edge of AH225 RFout pin (33° at 1960 MHz).
9. The edge of C6 is placed at 80 mils from the edge of AH225 RFout pin (8.4° at 1960 MHz).
10. Zero ohm jumpers may be replaced with copper traces in the target application layout.
11. DNP means Do Not Place.
12. The locations of C11, R2, C10 and C3 are non-critical. They can be placed closer to the device.
13. Ferrite Bead FB1 eliminates bypass line resonances between C15 and C1. Steward MI0603K300R-10.
14. All components are of 0603 size unless stated otherwise.

Typical Performance 1930-1990 MHz

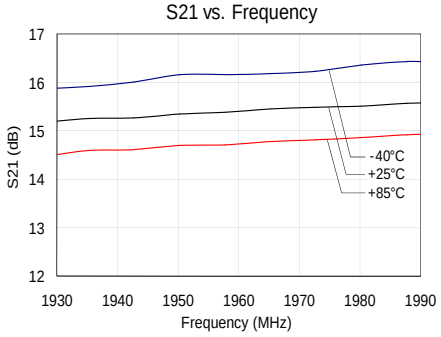
Frequency	MHz	1930	1960	1990
Gain	dB	15.2	15.4	15.6
Input Return Loss	dB	16	15.4	14.5
Output Return Loss	dB	7	8.3	9.6
Output P1dB	dBm	+31.2	+31.3	+31.1
Output IP3 at 19 dBm/tone, Δf = 1 MHz	dBm	+51.3	+53.6	+47.5
WCDMA Channel Power at -50 dBc ACLR [1]	dBm	+21.8	+21.7	+21.7
Noise Figure	dB	5.9	5.9	6
Supply Voltage, Vcc	V		+5	
Quiescent Collector Current, Icq	mA		300	

Notes:

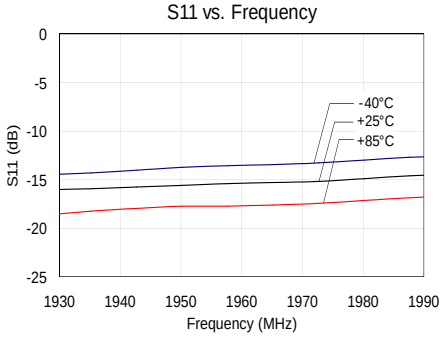
1. ACLR Test set-up: 3GPP WCDMA, TM1+64 DPCH, +5 MHz offset, PAR = 10.2 dB at 0.01% Prob.

Typical Performance Plots 1930-1990 MHz

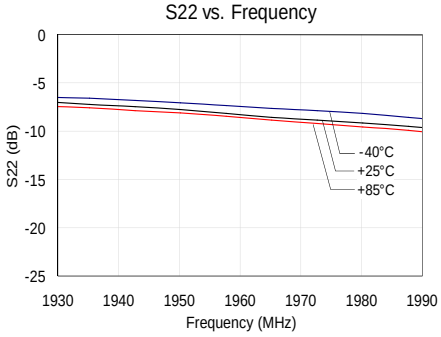
S21 vs. Frequency



S11 vs. Frequency

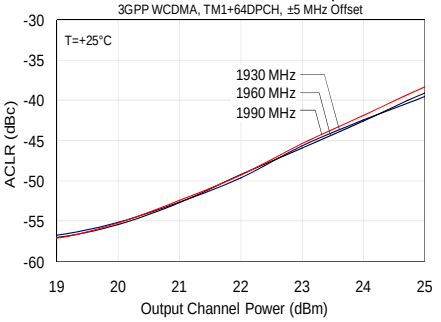


S22 vs. Frequency



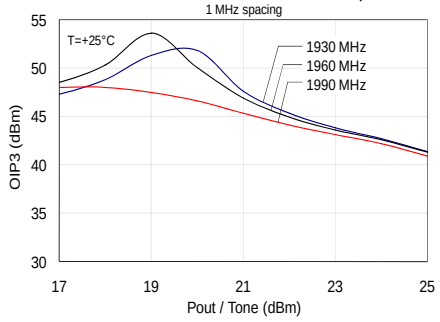
ACLR vs. Pout vs. Freq

3GPP WCDMA, TM1+64DPCH, ±5 MHz Offset



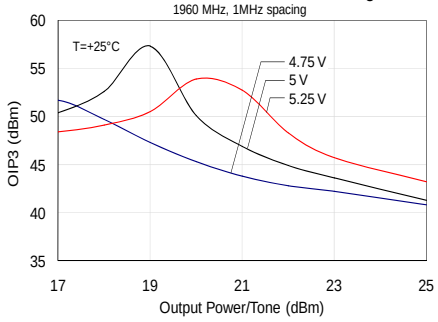
OIP3 vs. Pout / Tone vs. Freq

1 MHz spacing



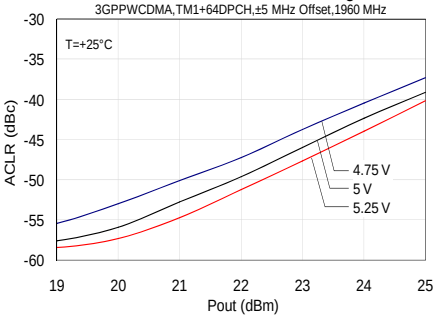
OIP3 vs. Pout/Tone vs. Bias Voltage

1960 MHz, 1MHz spacing

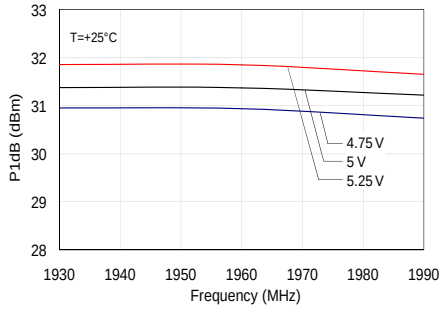


ACLR vs. Pout vs Bias Voltage

3GPPWCDMA,TM1+64DPCH,±5 MHz Offset,1960 MHz

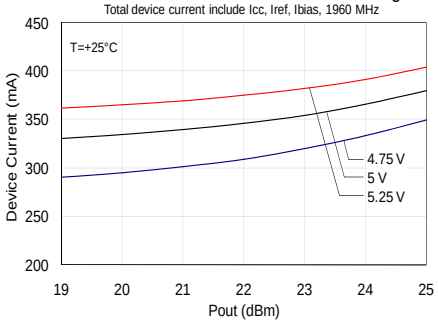


P1dB vs. Freq vs. Bias Voltage



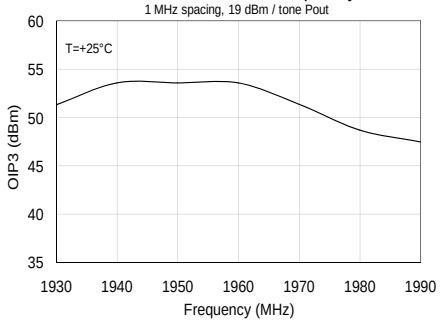
Total device current vs. Pout vs. Bias Voltage

Total device current include Icc, Iref, Ibias, 1960 MHz

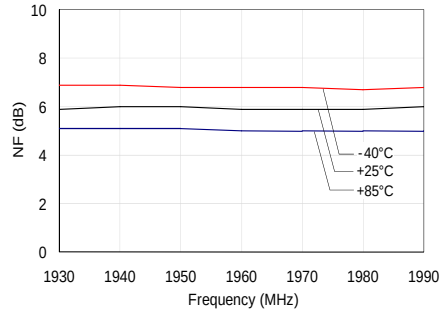


OIP3 vs. P1dB vs. Frequency

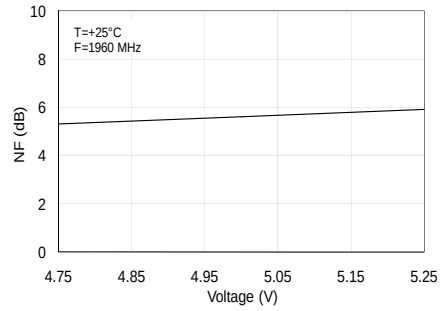
1 MHz spacing, 19 dBm / tone Pout



Noise Figure vs. Frequency



Noise Figure vs. Bias Voltage

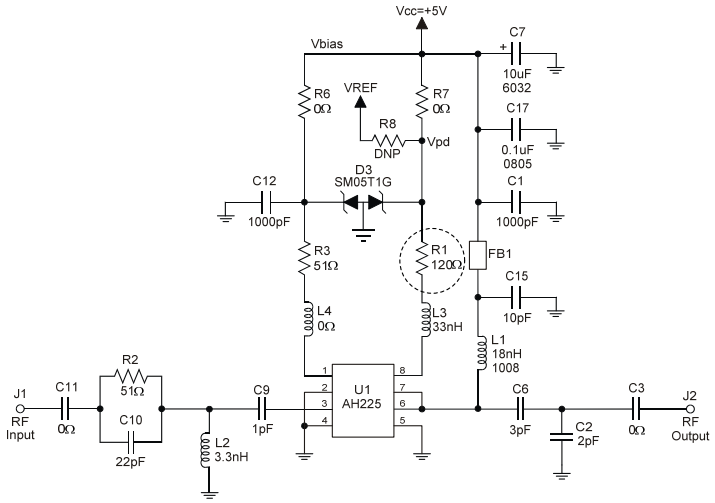


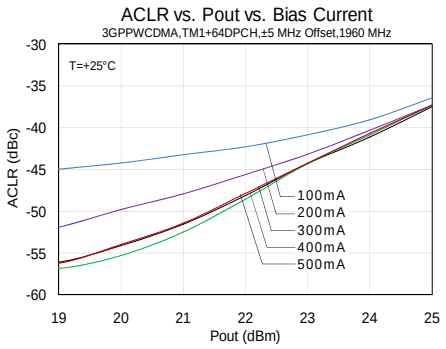
Reduced Bias Configurations Application Note

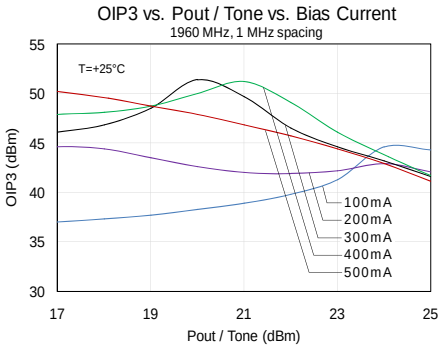
The AH225 can be configured to be operated with lower bias current by varying the Vpd resistor-R1 as highlighted on the schematic below. Lowering the current has little effect on the gain, OIP3, and P1dB performance of the device, but will slightly lower the ACLR performance of the device as shown below. It is expected that variation of the bias current for other frequency applications will produce similar performance results. The data below represents data taken from the AH225-S8PCB1960 with data taken at 1960 MHz.

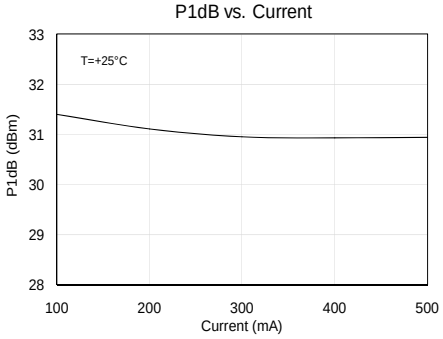
R1 (Ω)	Icq (mA)	Gain (dB)	Pdiss (W)	P1dB (dBm)	OIP3 (dBm)[1]	Pout (dBm)[2]
56.2	500	15.6	2.5	+30.9	+48.7	+21.4
82	400	15.4	2	+30.9	+48.7	+21.6
120	300	15.2	1.5	+30.9	+48.5	+21.4
200	200	14.8	1	+31.1	+43.5	+19.9
403	100	14	0.5	+31.4	+37.7	+15

Notes:
1. OIP3 is measured with two tones at output power of 19 dBm / tone separated by 1 MHz spacing.
2. ACLR Test set-up: 3GPP WCDMA, TM1+64 DPCH, +5 MHz offset, PAR = 10.2 dB at 0.01% Prob. Pout (Channel power) at -50 dBc ACLR is shown in the table above.

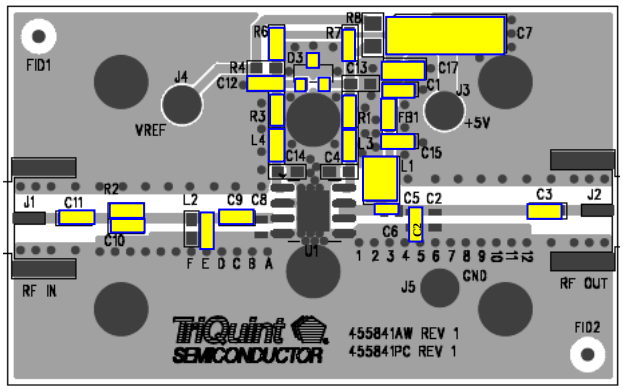


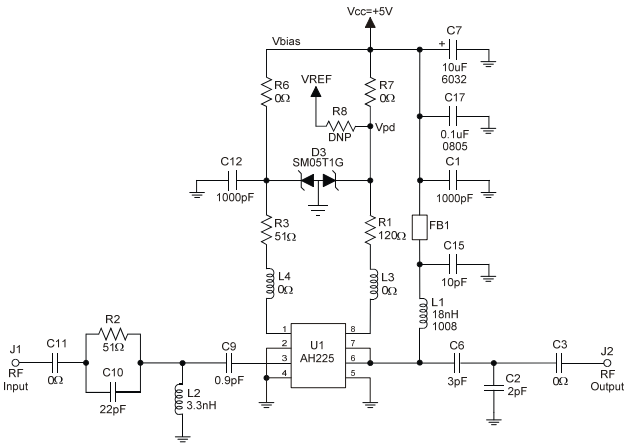






Application Circuit 2110-2170 MHz (AH225-S8PCB2140)





Notes:
1. See PC Board Layout, page 20 for more information.
2. Vref J4 turret can be used as control voltage for device power down (low = RF off) by setting R8 = 0 Ω and R8 = no connect.
3. The primary RF microstrip characteristic line impedance is 50 Ω.
4. Do not exceed +5.5V on Vpd or Vcc or TVS diode D3 will be damaged.
5. Components shown on the silkscreen but not on the schematic are not used.
6. The edge of L2 is placed at 225 mils from the edge of Ah225 RFin pin (24° at 2140 MHz).
7. The edge of C9 is placed at 80 mils from the edge of AH225 RFin pin (9° at 2140 MHz).
8. The edge of C2 is placed at 200 mils from the edge of AH225 RFout pin (23° at 2140 MHz).
9. The edge of C6 is placed at 80 mils from the edge of AH225 RFout pin (9° at 2140 MHz).
10. Zero ohm jumpers may be replaced with copper traces in the target application layout.
11. DNP means Do Not Place.
12. Inductor L3 on Vpd line is critical for linearity performance.
13. The locations of C11, R2, C10 and C3 are non-critical. They can be placed closer to the device.
14. Ferrite Bead FB1 eliminates bypass line resonances between C15 and C1. Steward MI0603K300R-10.
15. All components are of 0603 size unless stated otherwise.

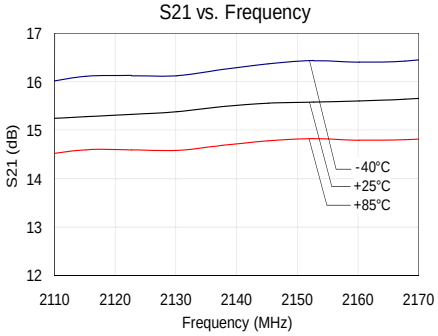
Typical Performance 2110-2170 MHz

Frequency	MHz	2110	2140	2170
Gain	dB	15.2	15.5	15.6
Input Return Loss	dB	20	18	17
Output Return Loss	dB	7.7	9.4	12
Output P1dB	dBm	+31.5	+31.2	+31.1
Output IP3 at 19 dBm/tone, Δf = 1 MHz	dBm	+45.6	+46	+46.1
WCDMA Channel Power at -50 dBc ACLR [1]	dBm	+20.9	+21.3	+21
Noise Figure	dB	6	6	5.9
Supply Voltage, Vcc	V		+5	
Quiescent Collector Current, Icq	mA		300	

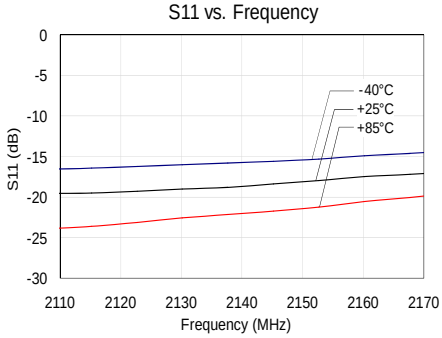
Notes:
1. ACLR Test set-up: 3GPP WCDMA, TM1+64 DPCH, +5 MHz offset, PAR = 10.2 dB at 0.01% Prob.

Typical Performance Plots 2110-2170 MHz

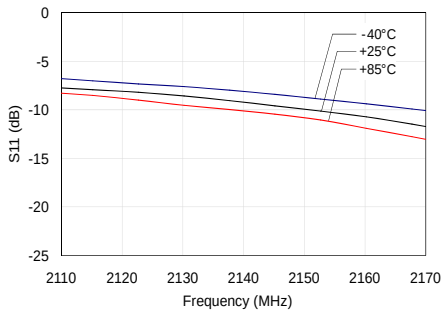
S21 vs. Frequency



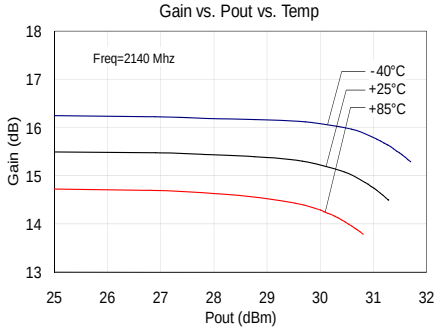
S11 vs. Frequency



S22 vs. Frequency

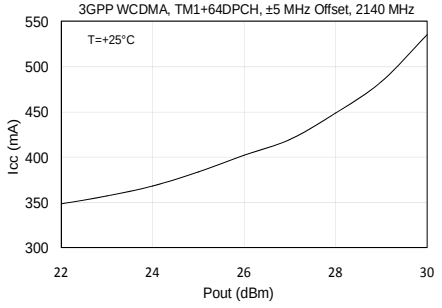


Gain vs. Pout vs. Temp

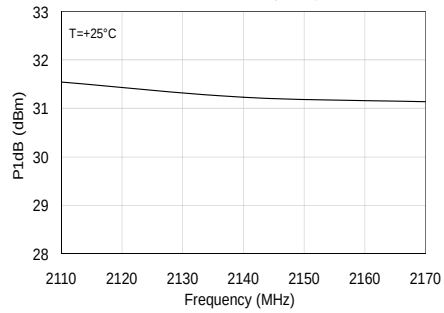


Icc vs. Pout

3GPP WCDMA, TM1+64DPCH, ±5 MHz Offset, 2140 MHz

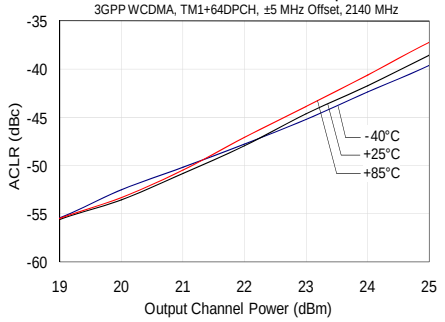


P1dB vs. Frequency



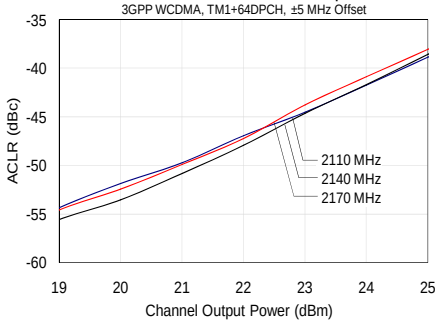
ACLR vs. Pout vs. Temp

3GPP WCDMA, TM1+64DPCH, ±5 MHz Offset, 2140 MHz

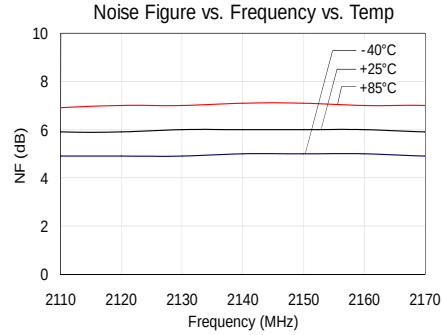


ACLR vs. Pout vs. Freq

3GPP WCDMA, TM1+64DPCH, ±5 MHz Offset

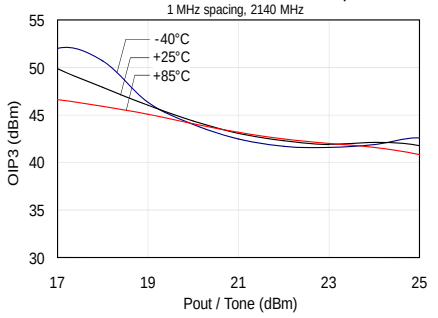


Noise Figure vs. Frequency vs. Temp



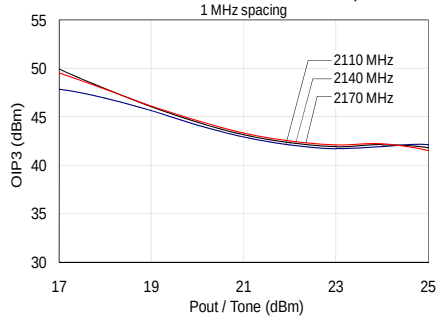
OIP3 vs. Pout/Tone vs. Temp

1 MHz spacing, 2140 MHz



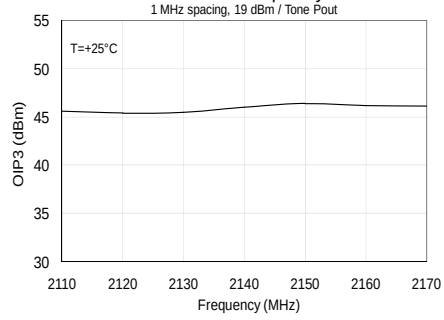
OIP3 vs. Pout/Tone vs. Freq

1 MHz spacing

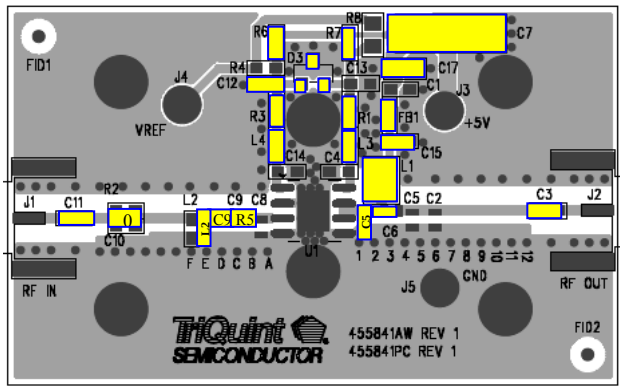


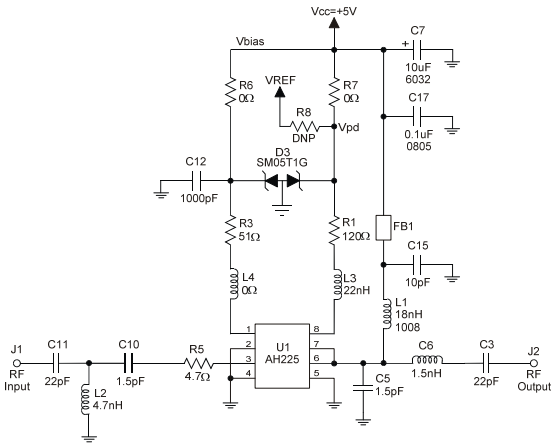
OIP3 vs. Frequency

1 MHz spacing, 19 dBm / Tone Pout



Reference Design 2500-2700 MHz





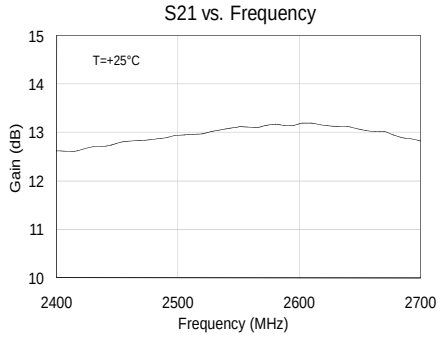
Notes:
1. See PC Board Layout, page 20 for more information.
2. Vref J4 turret can be used as control voltage for device power down (low = RF off) by setting R8 = 0 Ω and R8 = no connect.
3. The primary RF microstrip characteristic line impedance is 50 Ω.
4. Do not exceed +5.5V on Vpd or Vcc or TVS diode D3 will be damaged.
5. Components shown on the silkscreen but not on the schematic are not used.
6. The edge of C6 is placed at 75 mils from the edge of AH225 RFout pin (10.4° at 2600 MHz).
7. C5 is placed against the edge of C6.
8. The edge of R5 is placed at 10 mils from the edge of AH225 RFin pin (1.5° at 2600 MHz).
9. The edge of C9 is placed at 10 mils from the edge of R5 (1.5° at 2600 MHz).
10. L2 is placed against the edge of C9.
11. Zero ohm jumpers may be replaced with copper traces in the target application layout.
12. DNP means Do Not Place.
13. The multilayer inductor L3 on Vpd line is critical for linearity performance.
14. The locations of C11, R2, C10 and C3 are non-critical. They can be placed closer to the device.
15. Ferrite Bead FB1 eliminates bypass line resonances between C15 and C1. Steward MI0603K300R-10.
16. All components are of 0603 size unless stated otherwise.

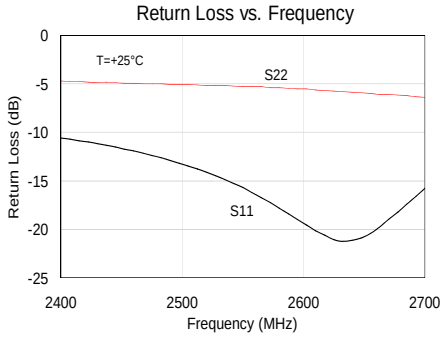
Typical Performance 2500-2700 MHz

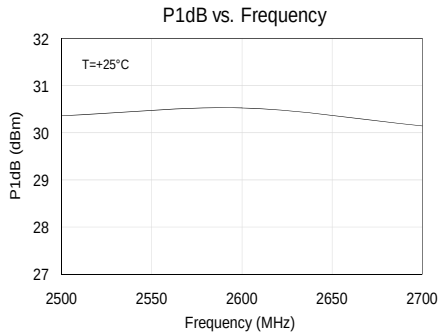
Frequency	MHz	2500	2600	2700
Gain	dB	12.9	13.2	12.8
Input Return Loss	dB	13.3	19.4	15.8
Output Return Loss	dB	5.2	5.5	6.4
Output P1dB	dBm	+30.4	+30.5	+30.2
Output IP3 at 19 dBm/tone, Δf = 1 MHz	dBm	+50	+48.7	+44.8
WCDMA Channel Power at -50 dBc ACLR [1]	dBm	+21.3	+21.3	+20.9
OFDMA Channel Power at 2.5% EVM [2]	dBm	+23	+23	+22.7
Supply Voltage, Vcc	V		+5	
Quiescent Collector Current, Icq	mA		300	

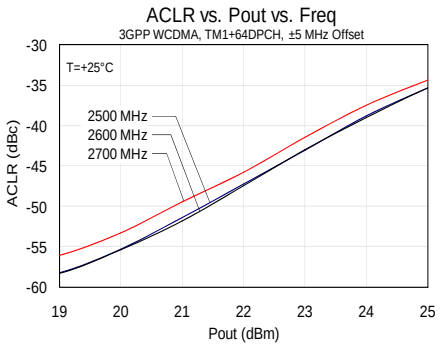
Notes:
1. ACLR Test set-up: 3GPP WCDMA, TM1+64 DPCH, +5 MHz offset, PAR = 10.2 dB at 0.01% Prob.
2. EVM Test set-up: 802.16 – 2004 OFDMA, 64 QAM – ½, 1024 FFT, 20 symbols, 30 sub channels.

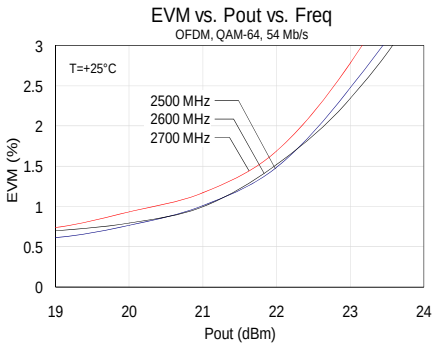
Typical Performance Plots 2500-2700 MHz

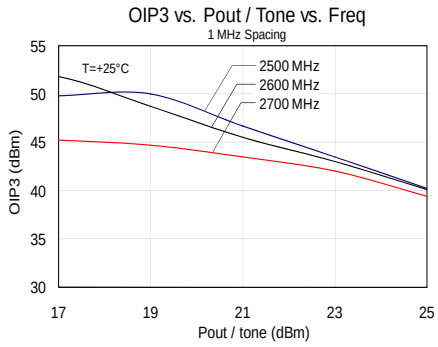




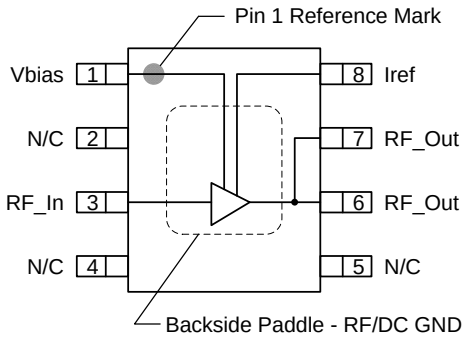








Pin Description



Pin	Symbol	Description
1	Vbias	Voltage supply for active bias. Connect to same supply voltage as Vcc.
2, 4, 5	N/C	No internal connection. This pin can be grounded or N/C on PCB.
3	RF_in	RF Input. Requires matching for operation.
6	RF_out	RF Output and DC supply voltage.
7	RF_out	See pin 6.
8	Iref	Reference current into internal active bias current mirror. Current into Iref sets device quiescent current. Also, can be used as on/off control.
Backside Paddle	RF/DC GND	Use recommended via pattern shown on page 20 and ensure good solder attach for optimum thermal and electrical performance.

Application Board Information

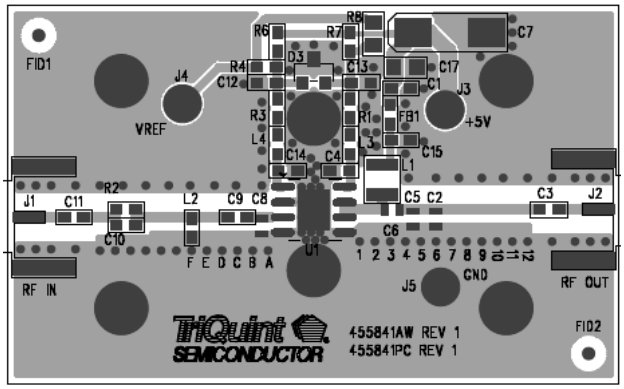
PC Board Layout

Top RF layer is .014" Getek, ϵ_r = 4.0, 4 total layers (0.062" thick) for mechanical rigidity. Metal layers are 1-oz copper. Microstrip line details: width = .030", spacing = .026".

The silk screen markers 'A', 'B', 'C', etc. and '1', '2', '3', etc. are used as placemarkers for the input and output tuning shunt capacitors – C8, C5 and C2. The markers and vias are spaced in .050" increments.

The pad pattern shown has been developed and tested for optimized assembly at TriQuint Semiconductor. The PCB land pattern has been developed to accommodate lead and package tolerances. Since surface mount processes vary from company to company, careful process development is recommended.

For further technical information, Refer to www.TriQuint.com

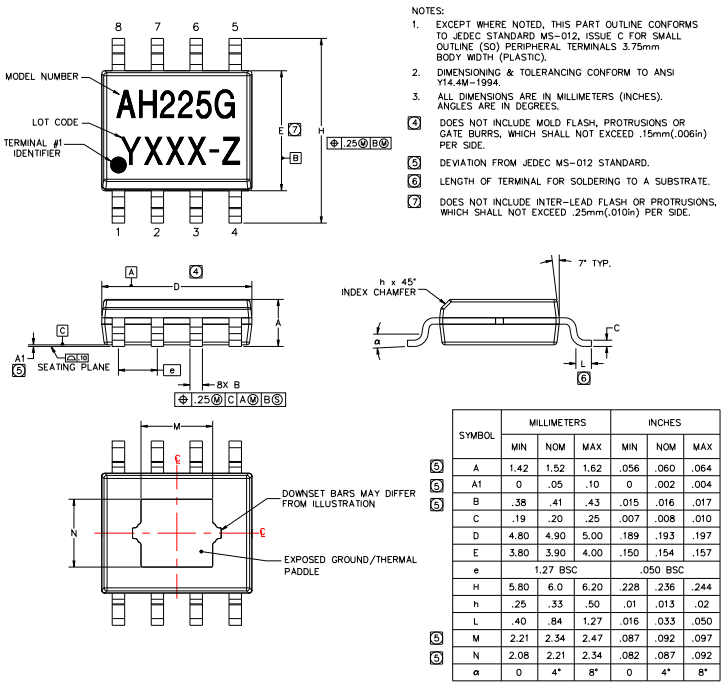


Mechanical Information

Package Information and Dimensions

This package is lead-free/RoHS-compliant. The plating material on the leads is NiPdAu. It is compatible with both lead-free (maximum 260 °C reflow temperature) and lead (maximum 245 °C reflow temperature) soldering processes.

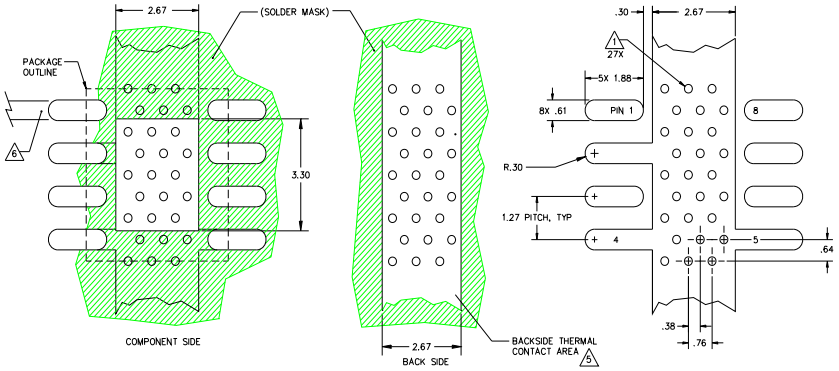
The AH225 will be marked with an "AH225G" designator with a lot code marked below the part designator. The "Y" represents the last digit of the year the part was manufactured, the "XXXX" is an auto-generated number, and "Z" refers to a wafer number in a lot batch.



NOTES:
1. EXCEPT WHERE NOTED, THIS PART OUTLINE CONFORMS TO JEDEC STANDARD MS-012, ISSUE C FOR SMALL OUTLINE (SO) PERIPHERAL TERMINALS 3.75mm BODY WIDTH (PLASTIC).
2. DIMENSIONING & TOLERANCING CONFORM TO ANSI Y14.4M-1994.
3. ALL DIMENSIONS ARE IN MILLIMETERS (INCHES). ANGLES ARE IN DEGREES.
4. DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS, WHICH SHALL NOT EXCEED .15mm(.006in) PER SIDE.
5. DEVIATION FROM JEDEC MS-012 STANDARD.
6. LENGTH OF TERMINAL FOR SOLDERING TO A SUBSTRATE.
7. DOES NOT INCLUDE INTER-LEAD FLASH OR PROTRUSIONS, WHICH SHALL NOT EXCEED .25mm(.010in) PER SIDE.

SYMBOL	MILLIMETERS			INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	1.42	1.52	1.62	.056	.060	.064
A1	0	.05	.10	0	.002	.004
B	.38	.41	.43	.015	.016	.017
C	.19	.20	.25	.007	.008	.010
D	4.80	4.90	5.00	.189	.193	.197
E	3.80	3.90	4.00	.150	.154	.157
e	1.27 BSC			.050 BSC		
H	5.80	6.0	6.20	.228	.236	.244
h	.25	.33	.50	.01	.013	.02
L	.40	.84	1.27	.016	.033	.050
M	2.21	2.34	2.47	.087	.092	.097
N	2.08	2.21	2.34	.082	.087	.092
α	0	4°	8°	0	4°	8°

Mounting Configuration



Notes:
1. A heat sink underneath the area of the PCB for the mounted device is strictly required for proper thermal operation. Damage to the device can occur without the use of one.
2. Ground / thermal vias are critical for the proper performance of this device. Vias should use a .35mm (#80 / .0135") diameter drill and have a final plated thru diameter of .25 mm (.010") or equivalent.
3. Add as much copper as possible to inner and outer layers near the part to ensure optimal thermal performance.
4. Mounting screws can be added near the part to fasten the board to a heat sink. Ensure that the ground / thermal via region contact the heat sink.
5. Do not put solder mask on the backside of the PC board in the region where the board contacts the heat sink.
6. RF Trace width depends upon the PC board material and construction.
7. Use 1 oz. Copper minimum.
8. All dimensions are in millimeters (inches). Angles are in degrees.

Product Compliance Information

ESD Information

Caution! ESD-Sensitive Device

ESD Rating:	Class 1C
Value:	Passes ≥ 1000 V min.
Test:	Human Body Model (HBM)
Standard:	JEDEC Standard JESD22A114-E

ESD Rating:	Class IV
Value:	Passes ≥ 1000 V min.
Test:	Charged Device Model (CDM)
Standard:	JEDEC Standard JESD22C101-C

MSL Rating

Level 2 at +260 °C convection reflow
The part is rated Moisture Sensitivity Level 2 at 260°C per JEDEC standard IPC/JEDEC J-STD-020.

Solderability

Compatible with the latest version of J-STD-020, Lead free solder, 260°.

This part is compliant with EU 2002/95/EC RoHS directive (Restrictions on the Use of Certain Hazardous Substances in Electrical and Electronic Equipment).

This product also has the following attributes:

- Lead Free
- Halogen Free (Chlorine, Bromine)
- Antimony Free
- TBBP-A ($C_{15}H_{12}Br_40_2$) Free
- PFOS Free
- SVHC Free

Contact Information

For the latest specifications, additional product information, worldwide sales and distribution locations, and information about TriQuint:

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Email: info-sales@tqs.com **Fax:** +1.503.615.8902

For technical questions and application information:

Email: sjcapplications.engineering@tqs.com

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