Introduction

The SY69952 Serial Transceiver is used in SONET/SDH and ATM applications to recover clock and data information from a 155.52MHz or 51.84MHz NRZ (Non Return to Zero) or NRZI (Non Return to Zero Invert on ones) serial data stream. This device also provides a bit rate Transmit clock, from a byte rate source through the use of a frequency multiplier PLL, and differential data buffering for the Transmit side of the system. This device is compliant with all relevant SONET/SDH specifications including ANSI T1X1.6/91-022, ANSI T1X1.3/93-006R1 Draft and ITU/CCITT G958.

General Requirements

For optimum performance of SY69952, loop filter networks are required. The loop filter network can be achieved using very few low cost external components. The purpose of the loop filter network is to minimize jitter characteristics of the device. In addition, proper power supply filtering techniques can also minimize jitter and matched impedance techniques should be used to maximize operating frequency and minimize wave-form distortion.

FORMULAS FOR CALCULATION OF CONTROLLED IMPEDANCE RUNS

Microstrip

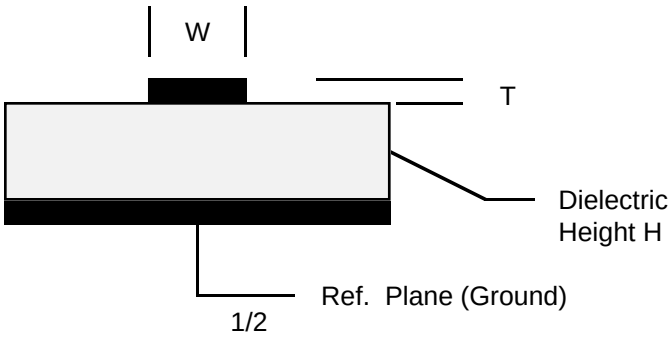


Figure 1

Stripline

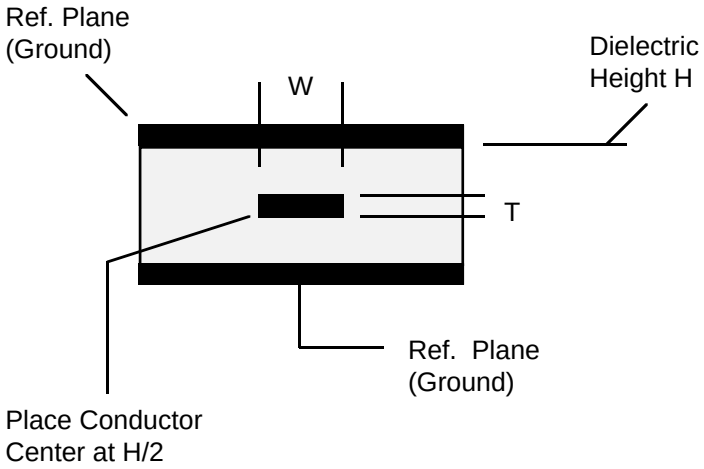


Figure 2

Requirements: W/(H-T)<0.35 AND T/H<0.25

$$\frac{87}{\sqrt{Er + 1.41}} \text{Ln} \frac{5.98\,H}{0.8\,W + T}$$

H is the height of the Dielectric to the Ground (Ref. Plane)

W is the Trace Width (Design Variable)

Er is the Dielectric Constant –
Consult with your Board Fabrication House (4.4 Typical)

T is the thickness of the run –
Consult with your Board Fabrication House (Typically 0.0022 with Plating)

$$\frac{60}{\sqrt{Er}} \text{Ln} \frac{4H}{0.536\pi W + 0.67\pi T}$$

H is the height of the Dielectric to the Ground (Ref. Plane)

W is the Trace Width (Design Variable)

Er is the Dielectric Constant –
Consult with your Board Fabrication House (4.4 Typical)

T is the thickness of the run –
Consult with your Board Fabrication House (Typically 0.0022 with Plating)

PIN DEFINITIONS

Pin	Pin No.	Type	Description
ROUT+	1	Receive	If Unused NC or VCC. Route away from TX, & Digital Runs.(1)
ROUT–	2	Receive	If Unused NC or VCC. Route away from TX, & Digital Runs.(1)
RIN+	3	Receive	Route away from TX, & Digital Runs.(1)
RIN–	4	Receive	Route away from TX, & Digital Runs.(1)
MODE	5	Control	No/LOW Frequency Switching.
VCC	6	Power	Isolation from system supply. Decouple with RF beads (or inductor or common mode chokes), NPO/COG ceramic and tantalum caps.(2)
CD	7	Control	LOW Frequency Switching. Routing should avoid noisy areas so run is not conduit. Use common mode choke to isolate.(2)
$\overline{\text{LOOP}}$	8	Control	No/LOW Frequency Switching. Routing should avoid noisy areas so run is not a conduit. Use common mode choke to isolate.(2)
REFCLK–	9	Reference	Route away from TX, & Digital Runs.(1)
REFCLK+	10	Reference	Route away from TX, & Digital Runs.(1)
TOUT–	11	Transmit	Route away from TX, & Digital Runs.(1)
TOUT+	12	Transmit	Route away from TX, & Digital Runs.(1)
PLL1+	13	Transmit	Place filter components next to IC. Do not route any signal near or beneath these pins or the TX filter connected to them. Use a ground guard around the filter components to collapse fields.
PLL1–	14	Transmit	Place filter components next to IC. Do not route any signal near or beneath these pins or the TX filter connected to them. Use a ground guard around the filter components to collapse fields.
PLL2–	15	Receive	Place filter components next to IC. Do not route any signal near or beneath these pins or the TX filter connected to them. Use a ground guard around the filter components to collapse fields.
PLL2+	16	Receive	Place filter components next to IC. Do not route any signal near or beneath these pins or the TX filter connected to them. Use a ground guard around the filter components to collapse fields.
TSER–	17	Transmit	Route away from Receiver runs.(1)
TSER+	18	Transmit	Route away from Receiver runs.(1)
TCLK+	19	Transmit	Route away from Receiver runs.(1)
TCLK–	20	Transmit	Route away from Receiver runs.(1)
VCC	21	Power	Isolation from system supply. Decouple with RF beads (or inductor or common mode chokes), NPO/COG ceramic and tant caps.(2)
VEE (GND)	22	Ground	Tie to system ground. If the system GND is noisy then isolation from system GND with RF bead (or inductor or common mode choke). Ensure adequate current capacity.(2)
VCC	23	Power	Isolation from system supply. Decouple with RF beads (or inductor or common mode chokes), NPO/COG ceramic and tant caps.(2)
$\overline{\text{LFI}}$	24	Alarm	LOW Frequency Switching. Routing should avoid noisy areas so run is not conduit. Use common mode choke to isolate.(2)

PIN DEFINITIONS (Continued)

Pin	Pin No.	Type	Description
RSER+	25	Receive	Route away from TX, & Digital Runs.(1)
RSER–	26	Receive	Route away from TX, & Digital Runs.(1)
RCLK+	27	Receive	Route away from TX, & Digital Runs.(1)
RCLK–	28	Receive	Route away from TX, & Digital Runs.(1)

NOTES:

1. **a)** These runs are to be held to an impedance of 50Ω. See **Microstrip** or **Stripline** above. Parallel Termination 130/82Ω shall be placed at their destinations; **b)** Runs must be of equal length to their corresponding differential counterpart. For example: RSER+ is equal to RSER–, RCLK+ is equal to RCLK–, etc.; **c)** These pairs must experience the same terrain of the PWB; **d)** Runs shall be constant distance to ground throughout their route. This will reduce crosstalk; **e)** Transmit runs shall be separated from receive runs.
2. Effective use of Common Mode Chokes or RF Beads dictate the following rules: **a)** Single Ended Signals shall utilize one half and the other should be connected to Grounds. This recommendation includes VCC. For this application ensure the Choke's)or RF Bead's) Max. Impedance is below the Fundamental (First) Harmonic; **b)** Differential Signals would have the positive signal on one half and the negative signal on the other. For this application ensure the Choke's max. Impedance is beyond the third harmonic. Failure to do so will result in sinusoidal waveforms instead of square waveforms. RF Beads are NOT recommended for this application; **c)** Separation of Grounds would have noisy ground on both of the inputs and clean (Analog or Receive) Ground on both of the outputs. For this application ensure the Choke's (or RF Bead's) Max. Impedance is below the Fundamental (First) Harmonic.

LAYOUT RECOMMENDATIONS (OPTIONAL)

The layout in figure 3 shows a typical configuration for very dense systems. The emphasis is on the loop filters PLL1 and PLL2 which are surrounded by a ground guard plane to reduce electromagnetic interference.

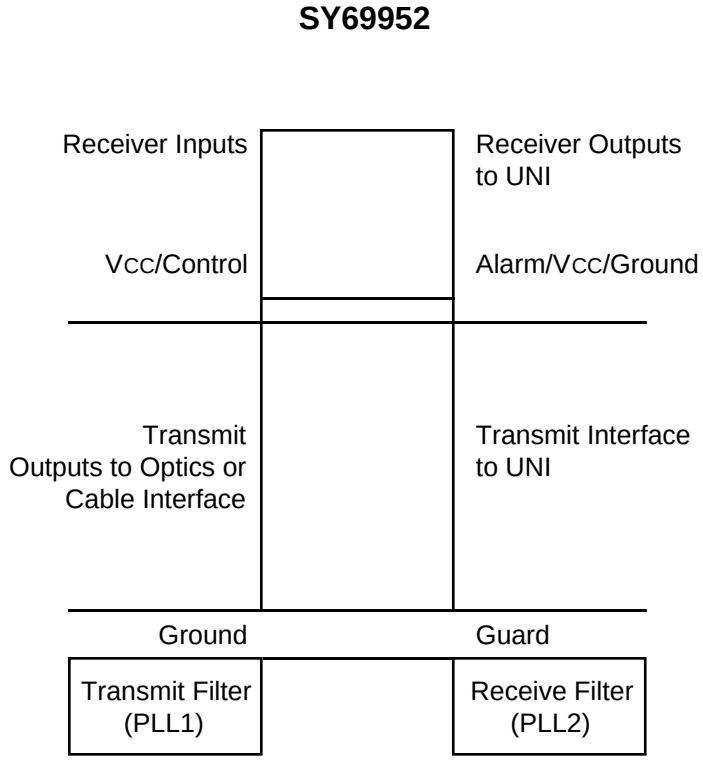


Figure 3

LOOP FILTER ADJUSTMENT

This section is ONLY applicable if initial values of external loop filters need to be adjusted for tuning the SY69952 to a layout or for customer's desired jitter response. R1 and C1 control response to Lower and Mid Range Modulation Frequencies. And C2 (optional) controls the the response to High Range Modulation Frequencies.

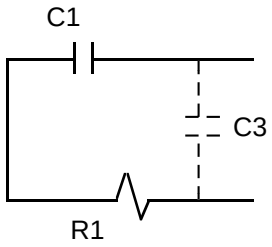


Figure 4

Transmit Filter Recommended Values:

PLL1+, Pin 13, C1 = 0.1µF,

PLL1–, Pin 14, R1 = 500Ω,

Optional PLL1+ and PLL1–, C2 = 47pF

Receive Filter Recommended Values:

PLL2+, Pin 16, C1 = 0.1µF,

PLL2–, Pin 15, R1 = 120Ω,

Optional PLL2+ and PLL2–, C2 = 47pF

If Jitter Amplitude response adjustment is required the following is an explanation of typical Loop Filter characteristics.

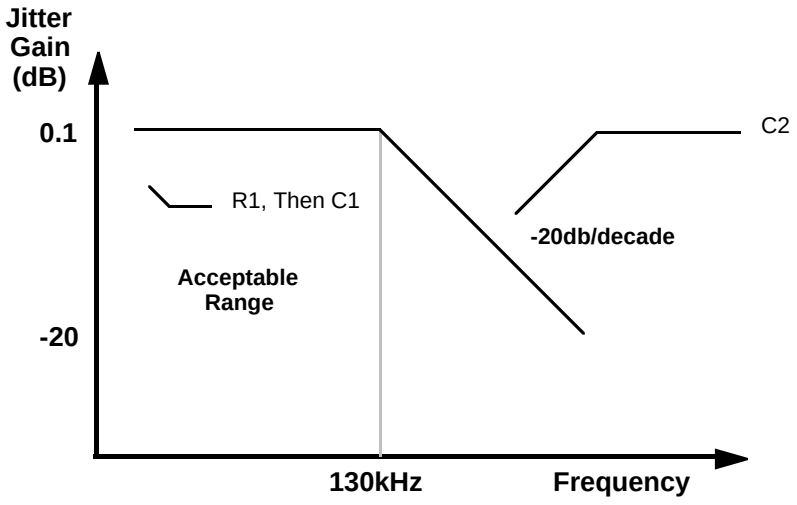
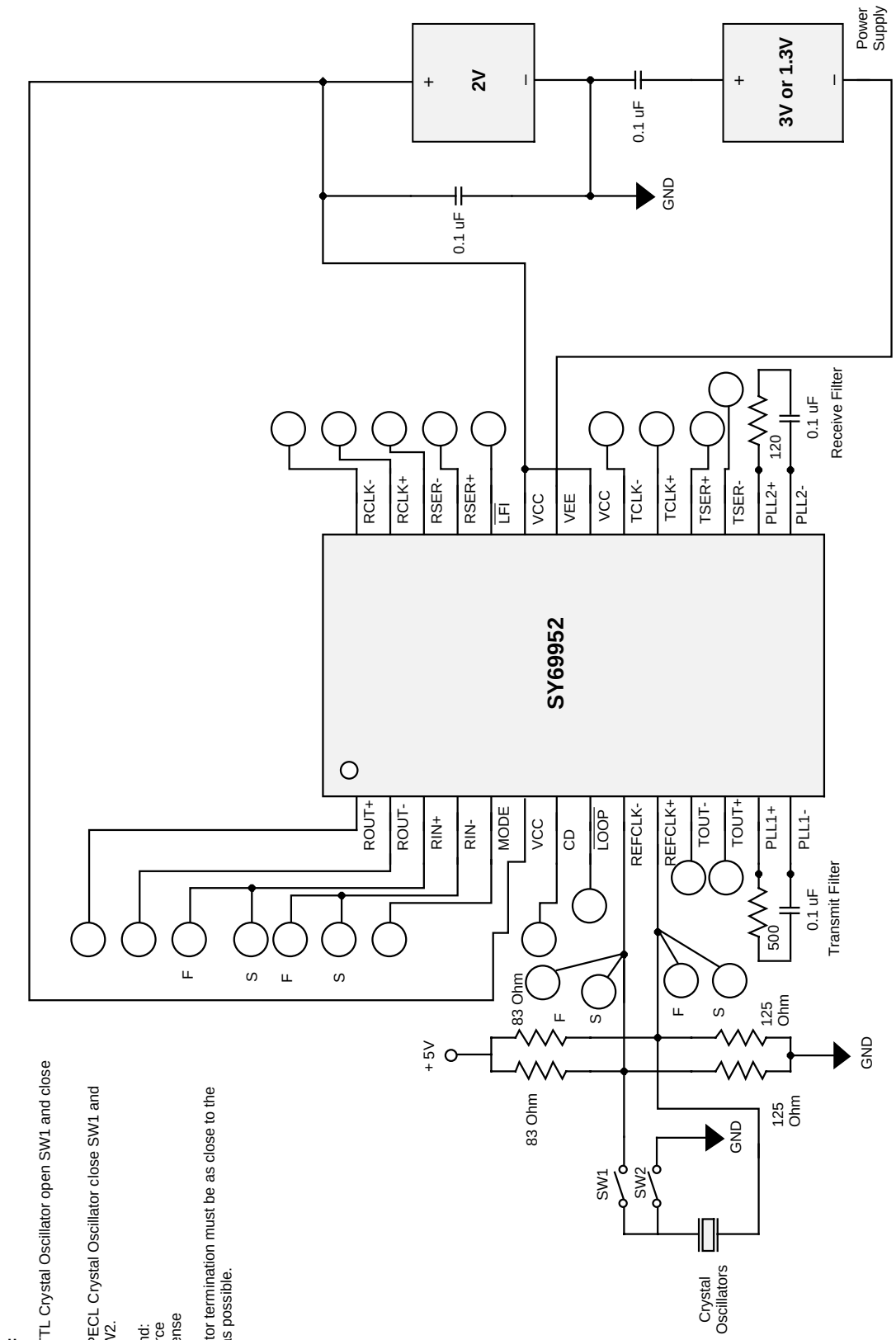


Figure 5

CONFIGURATION LAYOUT WITH SPLIT POWER SUPPLY



NOTES:

1. For TTL Crystal Oscillator open SW1 and close SW2.
2. For PECL Crystal Oscillator close SW1 and open SW2.
3. Legend:
   F: Force
   S: Sense
4. Resistor termination must be as close to the device as possible.

MICREL-SYNERGY 3250 SCOTT BOULEVARD SANTA CLARA CA 95054 USA
TEL + 1 (408) 980-9191 FAX + 1 (408) 914-7878 WEB http://www.micrel.com