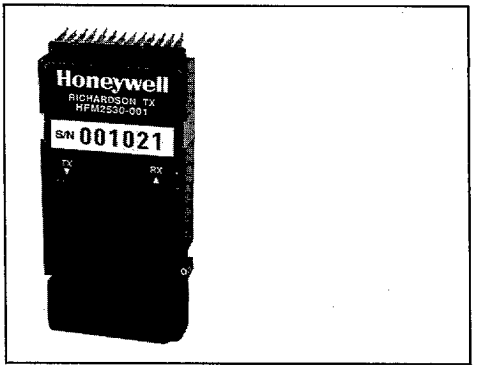
HFM2530-001

1300 nm FDDI (125 Mb/s) Transceiver Module

FEATURES

- Data Rate 10Mb/s to 125Mb/s, NRZ
- Power Supply Voltage Single +5 V
- Industry Standard FDDI 2 footprint
- FDDI MIC Receptacle Integrated Package
- Differential ECL (100 K) electrical interface
- Signal Detect Function



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DESCRIPTION

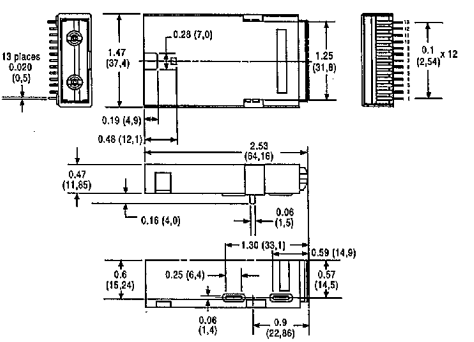
The HFM2530 is a 1300 nm FDDI (Fiber Distributed Data Interface) Fiber Optic transceiver module that provides a low cost solution to the requirements of FDDI over multimode fiber. The module is intended for the long wavelength 125 Mb/s, ANSI X3T12 format, although it will operate with other protocols. Typical uses include: LANs (Local Area Networks) clustered workstation links, and connections to mass storage devices.

The module is designed and tested to meet the FDDI link distance requirements for long wavelength, which is up to 2 Km over 50 or 62.5 micron fiber cable.

The HFM2530 consists of independent Transmitter (TX) and Receiver (RX) functions combined in a single transceiver module. The transmitter consists of a high reliability 1300 nm LED which couples to a fiber optic cable through the MIC (Media Interface Connector) connector. The TX is driven with a differential ECL (Emitter Coupled Logic) signal applied to TX In+ and TX In-. This signal is converted to a suitable modulation current by an LED driver Integrated Circuit (IC).

The optical receiver consists of a PIN+Preamp assembly and a Silicon Bipolar Post-amp IC. Optical input is coupled to the receiver with either a 50/125 micron fiber or a 62.5/125 micron fiber through an SC connector. Output from the module consists of differential PECL data signals on RX Out+ and RX Out- and a single PECL signal detect function RX Signal Detect.

OUTLINE DIMENSIONS in inches (mm)



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Pinout

1. GND_{RX}	8. $Case_{TX}$
2. Received data (RX In+)	9. V_{CCTX}
3. Received data (RX In-)	10 Sending data (TX Out+)
4. Signal detect (SD+)	11 Sending data (TX Out-)
5. Signal detect (SD-)	12 V_{BB}
6. V_{CCRX}	13 GND_{TX}
7. $Case_{RX}$	

Notes

1 V_{CCTX} and V_{CCRX} (or GND_{TX} and GND_{RX}) are not connected internally.

2 Case pins should be connected to GND pattern on the PCB.

3 Reference voltage is used only when single signal is used instead of differential ECL signals.

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RECEIVER INPUT TABLE

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	TEST CONDITIONS
Duty Cycle Distortion	DCD			1.0	ns	
Data Dependent Jitter	DDJ			1.2	ns	
Random Jitter	RJ			0.76	ns	
Optical Power	P_{IN}	-31.0		-14.0	dBm	

RECEIVER SIDE ELECTRICAL INTERFACE

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	TEST CONDITIONS
Supply Voltage	V_{CCRX}	4.75	5.0	5.25	V	
Supply Current	I_{RX}	25	70	120	mA	(1)
Output Voltage (High)	V_{OH}	V_{CCRX} -1.03		V_{CCRX} -0.88	V	(2) (3)
Output Voltage (Low)	V_{OL}	V_{CCRX} -1.81		V_{CCRX} -1.62	V	(2) (3)
Rise Time (20%-80%)	t_R	0.45	1.0	2.0	ns	(2) (3) (4)
Fall Time (80%-20%)	t_F	0.45	1.0	2.0	ns	(2) (3) (4)

Notes

1. Output currents are not included. 50% duty cycle data pattern at 125 Mb/s.
2. Output Load Resistance R_L = 50 to V_{CCRX} - 2.0 V. Transmission lines connected to RX In+ and RX In- should be symmetrical.
3. V_{CCRX} = 5.0 V, Ta = 25°C.
4. Measured at RX.

RECEIVER SIDE ELECTRO-OPTICAL INTERFACE CHARACTERISTICS

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	TEST CONDITIONS
Eye opening	T_{EYE}	2.1			ns	(1)
Signal Assert Power	P_A		-33	-31	dBm	(2)
Signal Assert Time	T_A		10	100	µs	
Signal DeAssert Power	P_D	-45 or Pb	-36		dBm	(2)
Signal DeAssert Time	T_D		10	350	µs	
Signal Hysteresis	P_{HYS}	1.5			dB	(3)

Notes

1. Eye opening shall be measured at peak-to-peak (BER = 2.5 x 10^{-10}) using DDJ test patterns outlined in Appendix -A of FDDI PMD. The input DDJ is 1.2 ns (peak-to-peak), input DCD (Duty Cycle Distortion) is 1.0 ns (peak-to-peak) and input RJ (Random Jitter) is 0.76 ns (peak-to-peak). See Receiver Input Table.
2. SD Assert/Deassert Times are measured using Idle symbols (62.5 MHz square wave). SD Assert/Deassert Power is measured by increasing/decreasing the input optical power using Idle symbols (62.5 MHz square wave). Pb is an input optical power which yields a BER of 0.01 or less.
3. Hysteresis is the difference between SD Assert Power and SD Deassert Power.

TRANSMITTER SIDE ELECTRICAL INTERFACE

T_A = 0 to 70°C, V_{CC} = 4.75 to 5.25 V, V_{EE} = GND, unless otherwise specified

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	TEST CONDITIONS
Supply Voltage	V_{CCTX}	4.75	5.0	5.25	V	
Supply Current	I_{TX}	40	90	160	mA	(1)
Input Voltage (High)	V_{IH}	V_{CCTX} -1.17		V_{CCTX} -0.73	V	(2)
Input Voltage (Low)	V_{IL}	V_{CCTX} -1.95		V_{CCTX} -1.45	V	(2)
Input Current (High)	I_{IH}			400	µA	(2)
Input Current (Low)	I_{IL}			150	µA	(2)
Reference Voltage	V_{BB}	V_{CCTX} - 1.41		V_{CCTX} - 1.23	V	(3)

Notes

1. Input bias currents are not included in Supply Current. 50% duty cycle data pattern at 125 Mb/s.
2. V_{CCTX} = 5.0 V, Ta = 25°C.
3. V_{BB} should only be connected to TX In+ or TX In-

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TRANSMITTER SIDE ELECTRO-OPTICAL INTERFACE CHARACTERISTICS

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	TEST CONDITIONS
Average Output Power	P_O	-19.0	-16.0	-14.0	dBm	(1)
Output Power (Input Low)	P_{OL}			-45	dBm	(2)
Eye opening	T_{EYE}	6.1		8.0	ns	(3)
Rise Time (10%-90%)	t_R	0.6	1.5	3.5	ns	(4) (5)
Fall Time (90%-10%)	t_F	0.6	2.0	3.5	ns	(4) (5)
Center Wavelength	λ_{CE}	1270	1330	1380	nm	(4)
Spectral Width (FWHM)	$\Delta\lambda$				nm	(5)

Notes

1. Average optical power is measured at the end of 100 m length 62.5/125/0.275 graded index fiber cable using the Halt Line State (12.5 MHz square wave) at the beginning of life (BOL).
2. Optical Power (Input Low) is measured using Quiet Line State (steady state low data).
3. The value is peak-to-peak (BER = 2.5 x 10^{-10}). The input signal is DDJ (Data Dependent Jitter) test pattern outlined in FDDI PMD (Physical Media Dependent)
4. The optical spectral width (full width half maximum) conforms to boundaries outlined in Figure 1. This data conforms to ANSI X3T9.5 / 84-48, Rev. 8. The rise and fall time use the Halt Line State (12.5 MHz square wave).
5. Refer to Figure 1: Spectral Width vs Center Wavelength

ORDER GUIDE

Description	Catalog Listing
1300 NM FDDI (125 Mb/s) Fiber Optic Transceiver Module	HFM2530-001

CAUTION

The inherent design of this component causes it to be sensitive to electrostatic discharge (ESD). To prevent ESD-induced damage and/or degradation to equipment, take normal ESD precautions when handling this product.

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RECOMMENDED TEST CIRCUIT

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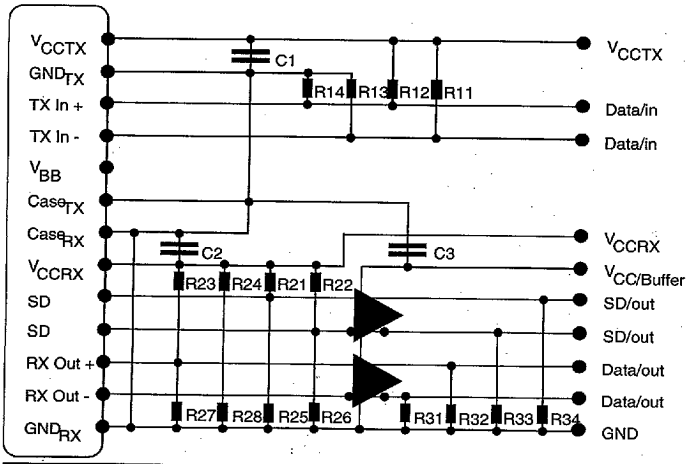

IC1	MC10H116
R11, R12, R21, R22, R23, R24	82 Ω
R13, R14, R25, R26, R27, R28	130 Ω
R31, R32, R33, R34	510 Ω
C1, C2, C3	0.1 µF ceramic capacitor
V_{CCTX}	4.75-5.25 VDC Input
V_{CCRX}	4.75-5.25 VDC Input
$V_{CC/Buffer}$	5.2 VDC Input

FUNCTIONAL BLOCK DIAGRAM

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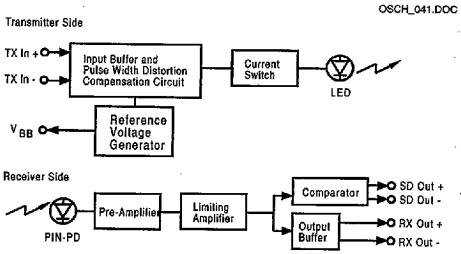

Fig. 1 Spectral width VS center wavelength

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