

LC74HC132M



3034A

CMOS High-Speed Standard Logic
LC74HC Series

Quad 2-Input Schmitt Trigger NAND Gate

©2244

Features

- The LC74HC132M consists of 4 identical 2-input Schmitt trigger NAND gates.
- Uses CMOS silicon gate process technology to achieve operating speeds similar to LS-TTL (74LS132) with the low power dissipation and high noise margin of standard CMOS ICs.
- Has buffered inputs and outputs, improving the output transition characteristics.
- All inputs and outputs are protected from damage.
- The LC74HC132M is functionally as well as pin-out compatible with the standard 74LS TTL logic family.

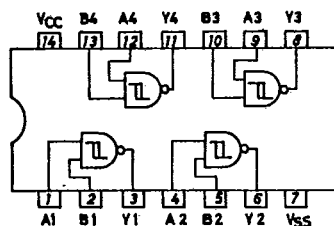
Absolute Maximum Ratings/ $T_a=25\pm 2^\circ\text{C}$, $V_{SS}=0\text{V}$

Maximum Supply Voltage	V_{CC} max	$V_{SS}-0.5$ to $V_{SS}+7.0$	V
Maximum Input Voltage	V_{IN} max	$V_{SS}-0.5$ to $V_{CC}+0.5$	V
Maximum Output Voltage	V_{OUT} max	$V_{SS}-0.5$ to $V_{CC}+0.5$	V
Maximum Output Current	I_{OUT}	Per output	± 25 mA
Current Dissipation	I_{CC}/I_{Gnd}		± 50 mA
Clamp Diode Current	I_K	Per input pin (Input protector)	± 20 mA
Allowable Power Dissipation	P_d max	Per package, $T_a \leq 85^\circ\text{C}$	150 mW
Storage Temperature	T_{stg}		-65 to $+150$ $^\circ\text{C}$
Lead Temperature and Time	T_{sol}	$t=10\text{sec}$	260 $^\circ\text{C}$

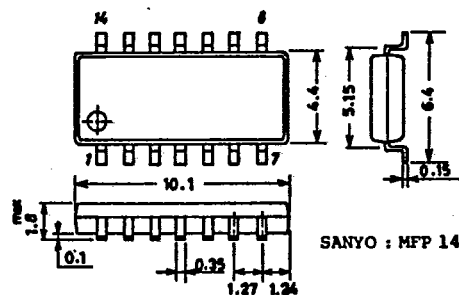
Allowable Operating Conditions/ $V_{SS}=0\text{V}$

Supply Voltage	V_{CC}	2.0 to 6.0	V
Input Voltage	V_{IN}	0 to V_{CC}	V
Output Voltage	V_{OUT}	0 to V_{CC}	V
Operating Temperature	T_{opg}	-40 to $+85$	$^\circ\text{C}$
Input Rise/Fall Time	t_r, t_f	0 to 500	ns

Pin Assignment



Case Outline 3034A-M141C (unit: mm)



For details, refer to the description of the LC74HC132.