All-in-OneMemory
SST88VP1107

Fact Sheet

FEATURES:

- **All-in-OneMemory: Managed Memory Sub-system for Code and Data in a Single Package**
  - Execute-in-place (XIP) Non-volatile area
    - NOR area
    - Pseudo-NOR™ (PNOR™) area
    - High-speed Pseudo-NOR (High-speed PNOR) area
  - RAM area
  - Memory-mapped ATA (mATA) NAND Disk area
- **Factory Default Memory Configuration**
  - NOR - 512 KByte (fixed)
  - High-speed PNOR - 128 KByte (re-configurable)
  - PNOR - 128 MByte (re-configurable)
  - RAM - 12 MByte (re-configurable)
  - mATA - 120 MByte (re-configurable)
- **Simple Host Interface**
  - Standard PSRAM interface for all areas
  - 16-bit Bus with required WAIT function
  - Asynchronous/Synchronous Single-access Read/Write cycles
  - Synchronous operation up to 80MHz
  - Page Mode and Burst Mode support in High-speed PNOR, PNOR, and RAM areas
  - Burst length up to 32 Words
- **4Mbit Built-in SST SuperFlash®**
  - Standard NOR bus interface and operation
  - Fast erase and program with SuperFlash
  - Immediately available upon power-up
  - Active in the deep power-down mode
- **Configurable High-speed PNOR and PNOR**
  - Full address range XIP emulated by using RAM as cache and NAND as non-volatile storage
  - Configurable memory area size to optimize NAND usage for code and data storage
  - Built-in cache controller provides cache coherence without host intervention
  - Configurable cache size for optimum performance and RAM usage
  - Dynamic Paging for optimum memory usage and Static Paging for minimum access latency
  - Built-in NAND controller provides Flash File System (FFS) without host intervention
- **Standard PSRAM**
  - Up to 8 MWord (128Mbit) of RAM for host
- **Memory-Mapped ATA (mATA) NAND Disk Area**
  - Up to 2 Gbit of data storage for host
  - Standard ATA protocol with bus cycles decoded on memory space
  - Built-in NAND controller performs NAND Disk function
- **Fast Asynchronous Access Time**
  - NOR: 50 ns
  - High-speed PNOR: 90 ns initial, 30 ns page access
  - PNOR: 150 ns initial, 55 ns page access
  - RAM: 130 ns initial, 55 ns page access
  - mATA: 70 ns
- **Read/Write Performance**
  - NOR:
    - Read: 40 MBytes/sec, Write: 200 KBytes/sec
  - High-speed PNOR (cache-hit):
    - Read: 140 MBytes/sec, Write: 145 MBytes/sec
  - PNOR (cache-hit):
    - Read:120 MBytes/sec, Write:130 MBytes/sec
  - RAM:
    - Read:120 MBytes/sec, Write: 130 MBytes/sec
  - mATA:
    - Read: 22 MBytes/sec, Write: 7 MBytes/sec
- **Protection and Security in NOR Area**
  - Secure Boot capability
  - 256 Word unique ID for enhanced security
  - 32 KWord hardware bottom boot block protection
  - Two 32 KWord One Time Programmable (OTP) protected areas
  - 64-bit password protection
- **Superior NAND Flash Management**
  - Superior data integrity through robust hardware ECC
    - Corrects random bit errors for SLC and MLC NAND
  - Built-in Microcontroller with intelligent firmware
    - Flash File System in embedded SuperFlash
    - Periodic Refresh to ensure NAND data integrity
    - Wear-leveling to prolong product life
    - Multi-tasking technology to boost NAND flash performance
- **Efficient Power Management Unit**
  - Immediate disabling of unused circuitry
  - Fast boot time from power-down
- **Low Power Consumption**
  - Active Mode current: 75 mA (typical)
  - Stand-by Mode curent: 500 µA (typical)
  - Deep Power-down mode current: 300 µA (typical)
- **1.8V and 3.0V Power Supplies**
- **Host Interface Voltage Selection Through V_{DDQ}**
  - 1.8V or 3.0V
- **Temperature Range**
  - 0° to +70°C for commercial operation
  - -25°C to +85°C for wireless operation
- **Package Available**
  - 80-Ball Low-Profile Ball Grid Array (LBGA) 10x13mm
- **All non-Pb (lead-free) devices are RoHS Compliant**

NOR Area

- **Direct Mapped and Dedicated 512 KWord (4Mb) SuperFlash for Performance-critical Code and Data**
- **Standard NOR Bus Interface and Operation**
- **Immediately Available upon Power-On**
- **Available in the Deep Power-Down Mode**
- **Asynchronous Single-access Read/Write Mode**
  - 50 ns access time
- **Synchronous Single-access Read/Write Mode up to 80MHz**
  - 4 cycles initial latency for Read
  - 3 cycles initial latency for Write
- **Super Fast Word Program**
  - 7 µs (typical)
- **Super Fast Sector-Erase Capability**
  - Uniform 2 KWord sectors
  - Sector-Erase Time: 18 ms (typical)
- **Super Fast Block-Erase Capability**
  - Uniform 32 KWord blocks
  - Block-Erase Time: 18 ms (typical)
- **NOR Area-Erase Capability**
  - Area-Erase Time: 40 ms (typical)
- **Erase-Suspend /-Resume Capability**
  - Read while Erase-Suspend
  - Program while Erase-Suspend
- **JEDEC Standard Compliant**
  - Flash EEPROM command sets
- **Optional Two-Cycle Command Mode**
- **End-of-Write detection**
  - Supports both toggle bits and data polling
- **Secure Boot Capability**
- **Hardware Bottom Boot Block Protection through NWP# Input pin**
  - 32 KWord bottom boot-block protection
- **Two 32 KWord user-programmable OTP areas**
- **256 Word Security-ID**
  - SST: 128 Word
  - User: 128 Word
- **Volatile and Non-volatile Block Protection**
- **64-bit Password Protection**
- **Superior Reliability with SST SuperFlash**
  - Endurance: Minimum 100,000 cycles (typical)
  - Greater than 100 years data retention

Pseudo-NOR™ Area

- **Emulates NOR memory using PSRAM and NAND**
  - Offers XIP access
  - Area size configurable up to 64 MWord
  - Built-in cache controller and Flash File System
  - Automatically loads on-demand page from NAND flash to cache
- **Improved NAND Reliability with Cache**
  - Minimizes Read Disturb Errors
  - Extends Write Endurance
- **Standard PSRAM bus Interface and Operation with Required Wait Function**
- **Uniform 1 KWord cache page size**
- **Four configurable regions**
  - All regions combined total size up to 64 MWord
  - Each region size 0 to 64 MWord
  - Each region served by a configurable PSRAM cache zone
- **Four configurable PSRAM cache zones**
  - Four cache zones combined total size up to 8 MWord
  - Each cache zone size 0 to 8 MWord
  - Cache zone has Two Host-configurable Options for Cache Operations
    - Static and Dynamic Paging modes
- **Asynchronous Single-access Read/Write Mode**
  - 150 ns access time
- **Asynchronous Page-Read Mode**
  - 55 ns page read time
- **Synchronous Burst Read/Write Mode up to 80MHz**
  - 10 cycles initial latency for Read
  - 7 cycles initial latency for Write

High-Speed Pseudo-NOR Area

- **Emulating High-speed NOR Memory Using SRAM and NAND without Host Intervention**
  - Offers XIP access
  - Area size configurable up to 64 MWord
  - Built-in cache controller and Flash File System
  - Automatically loads on-demand page from NAND flash to cache
- **Improved NAND Reliability with Cache**
  - Minimizes Read Disturb Errors
  - Extends Write Endurance
- **Standard PSRAM Bus Interface and Operation with Wait Function**
- **Embedded 2 KWord High-speed SRAM as Cache**
- **Uniform 1 KWord Cache Page Size**
- **One Configurable Region up to 64 MWord**
  - Region served by a cache zone in the high-speed SRAM
  - Cache zone has Two Host-configurable Options for Cache Operations
    - Static and dynamic paging modes
- **Asynchronous Single-access Read/Write Mode**
  - 90 ns access time
- **Asynchronous Page Read Mode**
  - 30 ns page read time
- **Synchronous Burst Read/Write Mode up to 80MHz**
  - 4 cycles initial latency for Read
  - 3 cycles initial latency for Write

RAM Area

- **Standard PSRAM Bus Interface and Operation**
- **Served by portion of PSRAM not used by the PNOR Cache Zones**
  - Up to 8 MWord (128Mbit) RAM space
- **Asynchronous Single-access Read/Write Mode**
  - 130 ns access time
- **Asynchronous Page-Read Mode**
  - 55 ns page read time
- **Synchronous Burst Read/Write Mode up to 80 MHz**
  - 9 cycles Initial latency for Read
  - 6 cycles Initial latency for Write

Memory-Mapped ATA NAND Disk Area

- **Standard ATA Protocol with Bus Cycles Decoded on Memory Space**
- **ATA Task File Registers are Memory-Mapped**
- **Built-in NAND controller performs NAND Disk Function**
  - Up to 128 MWord (2 Gbit) mass storage space
- **Asynchronous Single-access Read/Write Mode**
  - 70 ns access time
- **Synchronous Single-Access Read/Write Mode up to 80MHz**
  - 3 cycles Initial latency for Read/Write
- **8 Word address space for ATA Task File Registers**
- **256 Word address space for Data Registers**
- **Performance optimized ATA Controller**
- **Fast Wake-up Time**
  - Standby to Read/Write: 200 ns (typical)

PRODUCT DESCRIPTION

The SST88VP1107 is a reliable, high-performance, single-package, managed memory subsystem for code and data storage that is easy to use. Designed for embedded applications including mobile phones and portable consumer electronics, this product provides an all-in-one memory solution through its unique capability to configure its various memory resources. Providing code storage (NOR), data storage (NAND), and system RAM (PSRAM) functions all on a single bus, the SST88VP1107 is well suited for manufacturers who need high density memory with enhanced performance, superior quality, and reliability.

The All-in-OneMemory includes a boot NOR Flash, NAND controller, Cache controller, high-speed SRAM, PSRAM, and NAND Flash memory in a Multi Chip Package (MCP). The embedded NOR Flash offers a fast boot time, and provides many advanced data protection features for secure boot and code protection. The dedicated, performance-optimized NAND controller provides efficient data integrity, defect management, and wear-leveling by combining a robust hardware Error Correction Code (ECC) and a sophisticated Flash File System (FFS) in the embedded SuperFlash® memory. A built-in cache controller provides both static and dynamic paging modes, with controller-managed, cache-coherence operations.

The SST88VP1107 utilizes the advantages of both NOR and NAND flash memories to attain faster Read, Program, and Erase operations. This unified code and data storage solution allows the host to configure the memory-area and cache sizes for optimum memory utilization.

The All-in-OneMemory is highly configurable. The host device can define a variety of memory configurations using any of the following areas: a direct mapped high-performance 4 Mbit boot NOR memory area, two directly addressable Pseudo-NOR memory areas emulated by RAM and NAND, a directly addressable host RAM memory area, and a performance optimized mass storage area.

Through advanced data protection features, the SST All-in-OneMemory provides robust embedded security. The boot NOR area comes pre-programmed with a 128 Word unique security ID. For greater system security, program the additional 128 Word ID which creates a unique 256 Word security ID. In addition, the boot NOR area offers added security through 32 KWord hardware bottom boot-block protection, two 32 KWord One Time Programmable (OTP) secure areas, volatile block protection, non-volatile block protection, and 64 bit password protection.

The SST88VP1107 offers a built-in Flash File System (FFS) that makes the NAND flash memory management transparent to the host system. This eliminates the need for FFS software on the host, and reduces software development effort and time. The FFS also provides efficient defect management and effective wear-leveling algorithms to ensure even use of NAND flash media, which extend the longevity of the storage device.

The hardware Error Correction Code (ECC) module ensures superior data integrity and reliability by using an advanced ECC algorithm to correct random bit errors for both SLC and MLC NAND flash.

The built-in cache in the High-speed PNOR and PNOR areas improves reliability of these areas. Having a cache in front of the NAND flash helps to reduce the read disturb errors by minimizing repeated direct read access of a page to the NAND flash. The built-in cache also helps to extend the endurance of the storage device by minimizing direct write access to the NAND flash.

The SST88VP1107 is offered in both commercial and wireless temperature ranges in an 80-Ball LBGA package. See Figure 2-1 for pin assignments and Table 2-1 for pin descriptions.

1.0 FUNCTIONAL BLOCKS

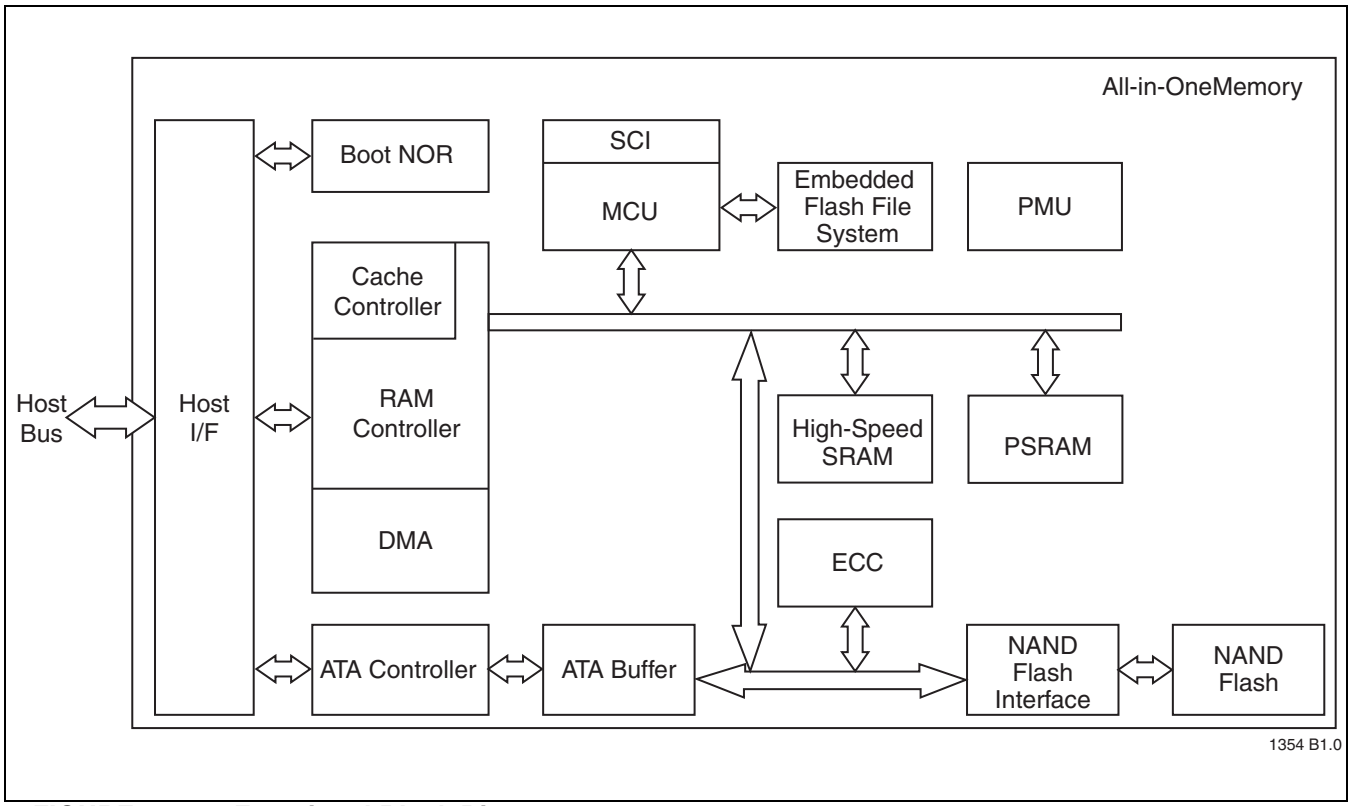

FIGURE 1-1: Functional Block Diagram

2.0 PIN ASSIGNMENTS

The pin assignments for the SST88VP1107 are shown in Figure 2-1 below. For the pin descriptions see Table 2-1.

The active low signals have the suffix "#." The I/O buffer types are listed in Table 2-2.

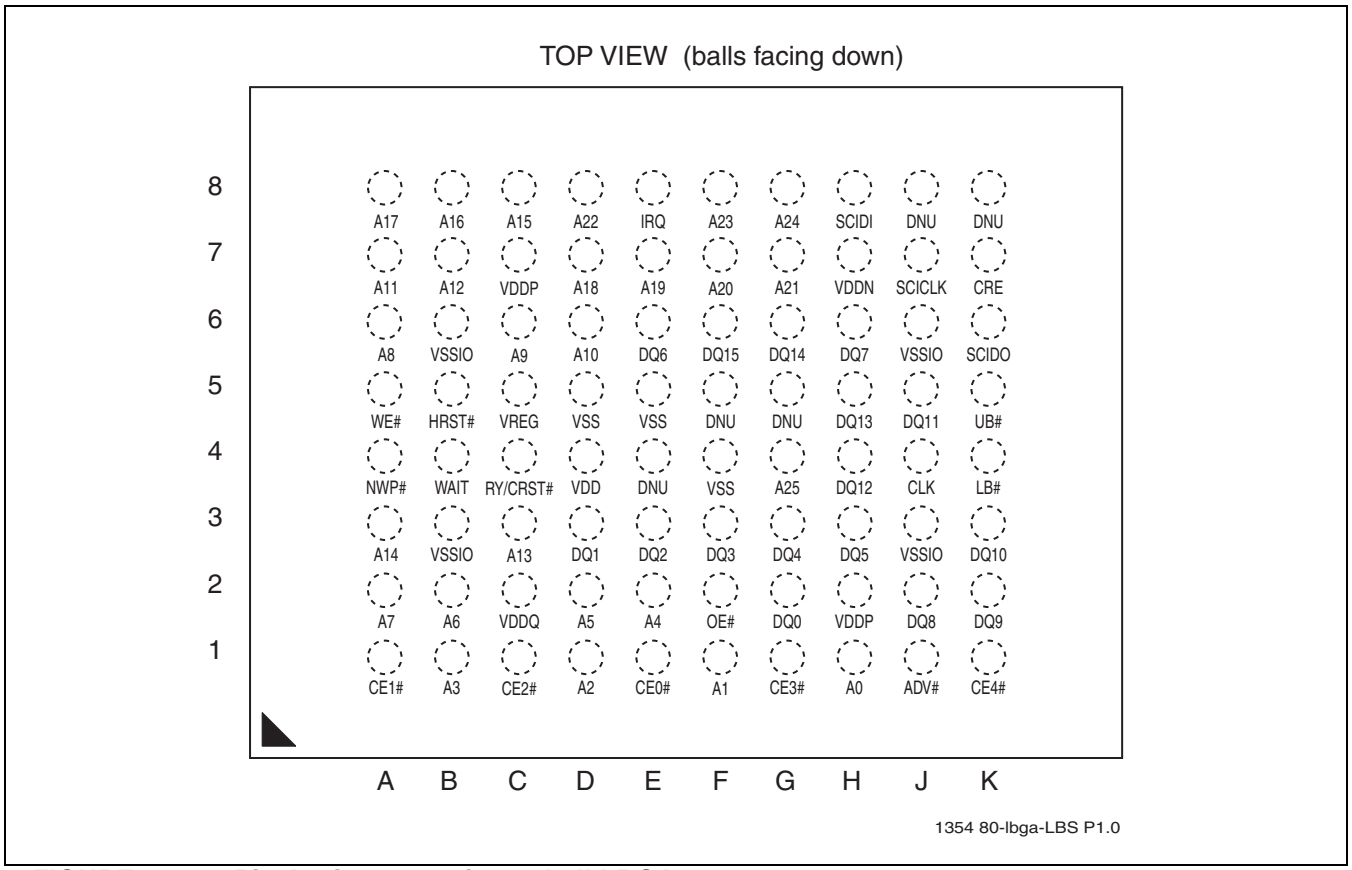

FIGURE 2-1: Pin Assignments for 80-ball LBGA

2.1 Pin Descriptions

The pins and functions of each pin are shown in Table 2-1.

TABLE 2-1: Pin Descriptions (1 of 3)

Symbol	Pin Location	Pin Type	I/O Type	Name and Functions
Host Interface				
CLK	J4	I	I1	Clock Input for the Synchronous Mode
HRST#	B5	I	I1	Hardware Reset Input (active low)
RY/CRST#	C4	O	O1	Ready/CPU Reset#. Indicates to the host system that the device is in power-up initialization or reset. The host can use this output signal as Ready signal or host CPU Reset signal. A logic high state indicates that the device is ready for normal operations. Active high when used as a Ready signal and active low when used as a Reset.
CE0#	E1	I	I1	Chip Enable for NOR area (active low)
CE1#	A1	I	I1	Chip Enable for High-speed PNOR, PNOR, and RAM areas in 3-Chip-Enable mode. (factory default)
CE2#	C1	I	I1	Must be tied to high in 3-Chip-Enable Mode (factory default). Used for other Chip Enable Modes. (active low)
CE3#	G1	I	I1	Must be tied to high in 3-Chip-Enable Mode (factory default). Used for other Chip Enable Modes. (active low)
CE4#	K1	I	I1	Chip Enable for memory-mapped ATA (mATA) area (active low)
CRE	K7	I	I1	Host Bus Configuration Register Enable (active high)
ADV#	J1	I	I1	Address Valid (active low)
OE#	F2	I	I1	Output Enable (active low)
WE#	A5	I	I1	Write Enable (active low)
UB#	K5	I	I1	Upper Byte Select (active low)
LB#	K4	I	I1	Lower Byte Select (active low)
NWP#	A4	I	I1	Write Protect Input for NOR area. Protects Bottom Boot Block from Erase/Program operations (active low)
WAIT	B4	OZ	OZ1	WAIT signal. When asserted, indicates to the host system that the output data is not valid during read operations and that the input data will not be latched by the device during write operations. In NOR and mATA areas, the WAIT output signal should be ignored in the Asynchronous Mode. The polarity of the WAIT output signal can be configured (default active high).
IRQ	E8	O	O1	mATA area Interrupt Request to Host

TABLE 2-1: Pin Descriptions (Continued) (2 of 3)

Symbol	Pin Location	Pin Type	I/O Type	Name and Functions
A25	G4	I	I1	Host Address Bus [25:0]. This is a word address
A24	G8	I	I1	
A23	F8	I	I1	
A22	D8	I	I1	
A21	G7	I	I1	
A20	F7	I	I1	
A19	E7	I	I1	
A18	D7	I	I1	
A17	A8	I	I1	
A16	B8	I	I1	
A15	C8	I	I1	
A14	A3	I	I1	
A13	C3	I	I1	
A12	B7	I	I1	
A11	A7	I	I1	
A10	D6	I	I1	
A9	C6	I	I1	
A8	A6	I	I1	
A7	A2	I	I1	
A6	B2	I	I1	
A5	D2	I	I1	
A4	E2	I	I1	
A3	B1	I	I1	
A2	D1	I	I1	
A1	F1	I	I1	
A0	H1	I	I1	
DQ15	F6	I/O	IO1	Bi-directional Host Data Bus [15:0]
DQ14	G6	I/O	IO1	
DQ13	H5	I/O	IO1	
DQ12	H4	I/O	IO1	
DQ11	J5	I/O	IO1	
DQ10	K3	I/O	IO1	
DQ9	K2	I/O	IO1	
DQ8	J2	I/O	IO1	
DQ7	H6	I/O	IO1	
DQ6	E6	I/O	IO1	
DQ5	H3	I/O	IO1	
DQ4	G3	I/O	IO1	
DQ3	F3	I/O	IO1	
DQ2	E3	I/O	IO1	
DQ1	D3	I/O	IO1	
DQ0	G2	I/O	IO1	

TABLE 2-1: Pin Descriptions (Continued) (3 of 3)

Symbol	Pin Location	Pin Type	I/O Type	Name and Functions
Debug Interface				
SCICLK	J7	I (PD)	I_PD1	Serial Interface Clock Input
DNU	G5	-	-	Do not use. Reserved
DNU	K8	-	-	Do not use. Reserved
SCIDI	H8	I (PU)	I_PU1	Serial Interface Data Input
DNU	J8	O	O1	Do not use. Reserved
SCIDO	K6	O	O1	Serial Interface Data Output
DNU	E4, F5	-	-	Do not use. Reserved
Misc.				
VREG	C5	Power	PWR1	Internal voltage regulator output. An external ceramic capacitor (4.7µF) must be connected between this pin and system ground.
Power and Ground				
VDDQ	C2	Power	PWR1	Power for Host Bus Interface (1.8V/3.0V)
VDDP	C7, H2	Power	PWR1	Power for PSRAM (1.8V)
VDDN	H7	Power	PWR1	Power for NAND Flash (3.0V)
VDD	D4	Power	PWR1	Power for core logic (3.0V)
VSSIO	B3, B6, J3, J6	Ground	PWR1	GND for IO
VSS	D5, E5, F4	Ground	PWR1	GND for core logic

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TABLE 2-2: Input/Output (I/O) Buffer Types

I/O Buffer Type	Description
I1	Input buffer[1]
I_PU1	Input buffer with internal pull-up
I_PD1	Input buffer with internal pull-down
O1	Output buffer
IO1	I/O buffer
OZ1	Output buffer with tri-state
PWR1	Power or Ground pad

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1. Any pin configured as input without internal pull-up or pull-down resistor must not be left unconnected.

3.0 DEVICE ELEMENTS

The All-in-OneMemory contains a boot NOR flash, 32 bit microcontroller, embedded flash file system (FFS), cache controller, ATA controller, PSRAM, and NAND flash all integrated in a LBGA package. This device has five different memory areas: NOR, High-speed Pseudo-NOR (High-speed PNOR), Pseudo-NOR (PNOR), RAM, and memory-mapped ATA (mATA). The host memory bus can write data to, and read data from, these five different memory areas. The default configuration has 3 chip enables with High-speed PNOR, PNOR, and RAM sharing one chip enable. Refer to Figure 1-1 for the All-in-OneMemory block diagram.

All-in-OneMemory interfaces with the host system through a standard PSRAM bus interface, supporting both asynchronous read/write and synchronous read/write operations. The NOR area is directly mapped to the NOR flash and is available for boot access immediately after power-up initialization. Similarly, the RAM area is directly mapped to a partition of the internal PSRAM.

In the High-speed PNOR and PNOR areas, a two-way set associative cache controller moves pages between NAND flash and high-speed SRAM for the High-speed PNOR, or PSRAM for the PNOR area. This built-in cache controller supports both static and dynamic paging modes.

In the mATA area, the All-in-OneMemory converts standard ATA protocols into flash media data and control signals and performs Flash File System operations to translate the host logical address to NAND physical address.

The components that contribute to the All-in-OneMemory operations are described in Sections 3.1 - 3.16.

3.1 Microcontroller Unit (MCU)

The 32-bit Microcontroller Unit manages internal operations of the All-in-OneMemory by translating host commands into data and control signals required for internal memory operations.

3.2 Host Interface

For Write operations, the host interface receives control signals and data from the host bus and directs them to the host-selected memory area. For Read operations, the host interface receives control signals from the host bus and drives data from the host-selected memory area to the host bus.

3.3 Boot NOR

The boot NOR flash is used to store the boot code and any time-critical code and data. The boot NOR area is available for host access immediately after power-up initialization, and supports a minimum page size of 2 KWord.

3.4 Embedded Flash File System (FFS)

The embedded Flash File System (FFS) is an integral part of the All-in-OneMemory flash memory, handling all data transfers to and from the NAND flash. The controller-embedded flash memory stores the firmware and FFS, and allows for quicker firmware upgrades, if required.

The FFS performs the following tasks:

- Translates host side operations into flash memory Read and Write operations
- Increases longevity by providing wear-leveling to evenly distribute Write actions across the entire NAND memory
- Performs NAND flash bad-block management
- Keeps track of FFS data structure
- Manages system security for selected protection zones

3.5 Cache Controller

The built-in cache controller manages access to the High-speed PNOR and PNOR areas. The cache controller uses a two-way set associative caching scheme to improve cache hit rate. The cache controller supports both static and dynamic paging modes with 1K Word page size. The cache coherence operations are complete managed by the cache controller without any host intervention. However, the host may issue page or flush cache commands through the device control interface, if required.

3.6 RAM Controller

The RAM controller is the interface to the high-speed SRAM and the PSRAM memories.

3.7 High-speed SRAM

A 2 KWord cache zone, Zone H, serves the High-speed PNOR area. The 2 KWord high-speed SRAM is used as cache for the Zone H cache zone.

3.8 PSRAM

The PSRAM is divided into two partitions whose size is configurable by the host. One partition is the cache for the PNOR area cache zones which is served by four size-configurable cache zones—Zone 0 through Zone 3. The other partition is available to the host as system RAM.

3.9 ATA Controller

The ATA controller supports standard ATA protocols, and receives ATA commands from the host interface. This controller moves data from the host interface to the ATA buffer for ATA Write commands, and from the buffer to the host interface for ATA Read commands.

3.10 ATA Buffer

A key contributor to the mATA area performance is the SRAM ATA buffer. This 512 Word buffer optimizes data transfers to and from the NAND flash media, beginning transfer when the buffer contains 256 Words.

3.11 NAND Flash Interface

The multi-tasking NAND flash interface enables fast, sustained write performance by allowing multiple Read, Program, and Erase operations to several flash media chips or planes.

3.12 Error Correction Code (ECC)

The hardware Error Correction Code (ECC) module utilizes an advanced ECC algorithm which corrects random bit errors for both SLC and MLC NAND flash.

3.13 NAND Flash

The NAND flash is used as the non-volatile storage media for High-speed PNOR, PNOR, and mATA areas. The size of each area is configurable by the host.

3.14 Direct Memory Access (DMA)

SST88VP1107 uses internal DMA engine for instant data transfer between the NAND flash and the High-speed SRAM, PSRAM, or ATA buffer. This implementation eliminates the microcontroller overhead associated with the traditional firmware-based approach and results in increased data transfer rates.

3.15 Power Management Unit (PMU)

The Power Management Unit (PMU) handles the power consumption of All-in-OneMemory. The PMU dramatically reduces power consumption by automatically putting the circuitry that is not being used in the operation into standby mode.

3.16 Serial Communication Interface (SCI)

For additional manufacturing flexibility, the SCI bus can be used for device configuration and error reporting. This bus consists of 3 active signals: SCICLK, SCIDI, and SCIDO. SST strongly recommends providing access to the device SCI interface at the system level during development and manufacturing.

4.0 SYSTEM INTERFACE

Figure 4-1 is a simplified interface diagram that shows how the All-in-OneMemory is connected to the host through a standard PSRAM bus interface.

For a complete list of interface signals, and a detailed description of their functions, please see Table 2-1.

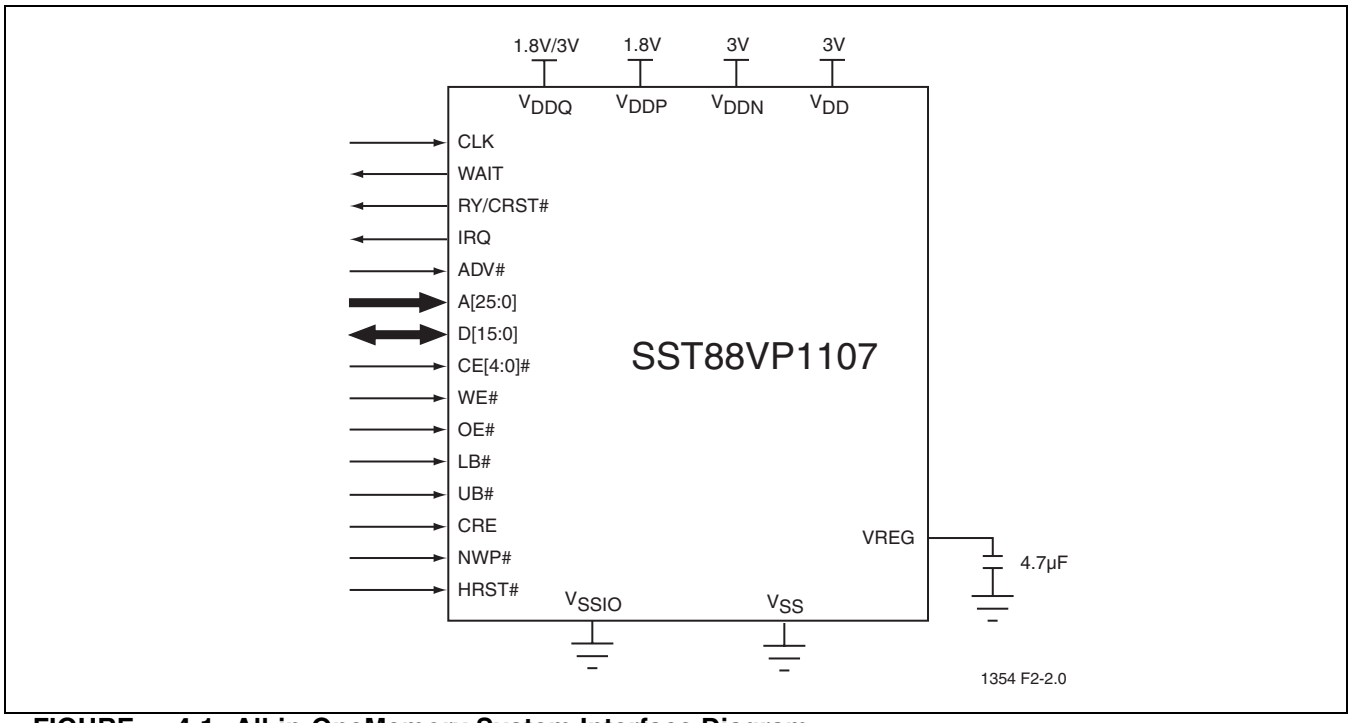
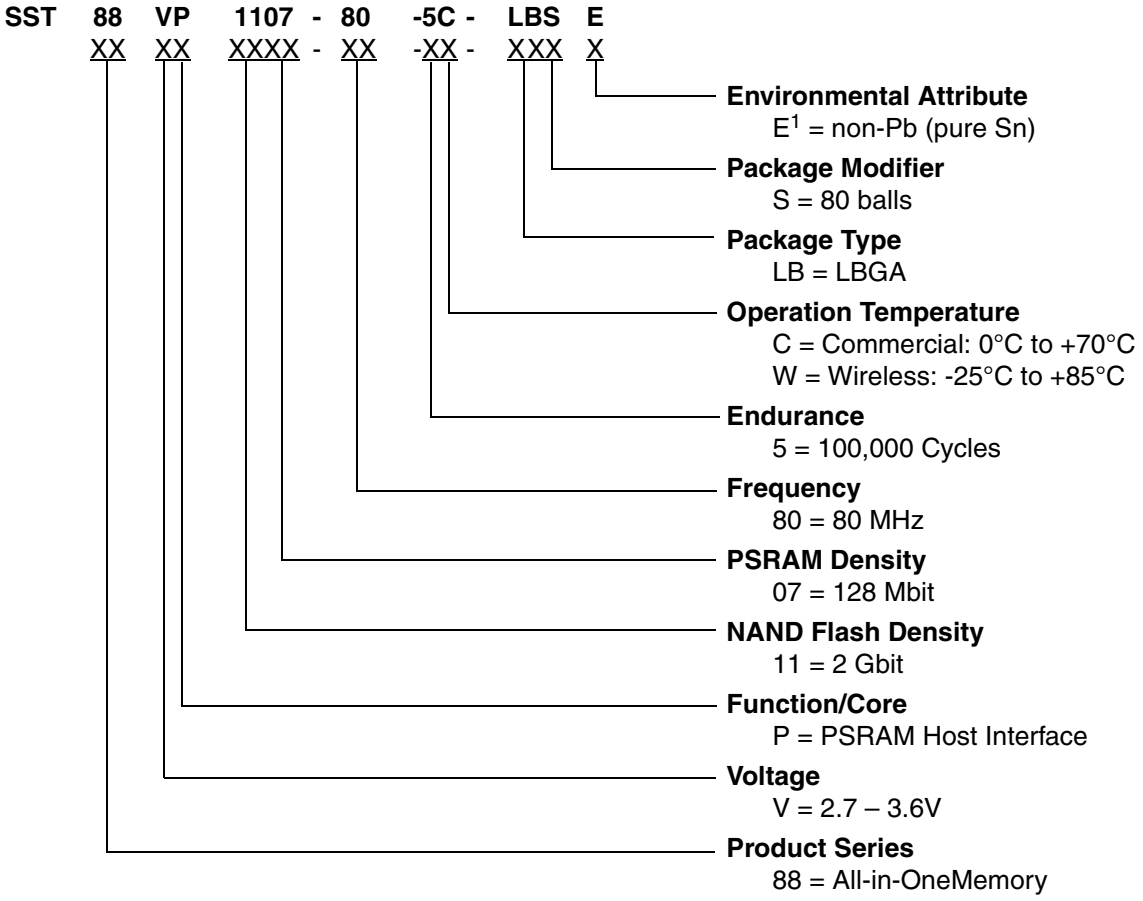


FIGURE 4-1: All-in-OneMemory System Interface Diagram

5.0 PRODUCT ORDERING INFORMATION



1 Environmental suffix “E” denotes non-Pb solder.
SST non-Pb solder devices are “RoHS Compliant”.

5.1 Valid Combinations

Valid combinations for SST88VP1107

SST88VP1107-80-5C-LBSE

SST88VP1107-80-5W-LBSE

Note: Valid combinations are those products in mass production or will be in mass production. Consult your SST sales representative to confirm availability of valid combinations and to determine availability of new combinations.

6.0 PACKAGE DIAGRAMS

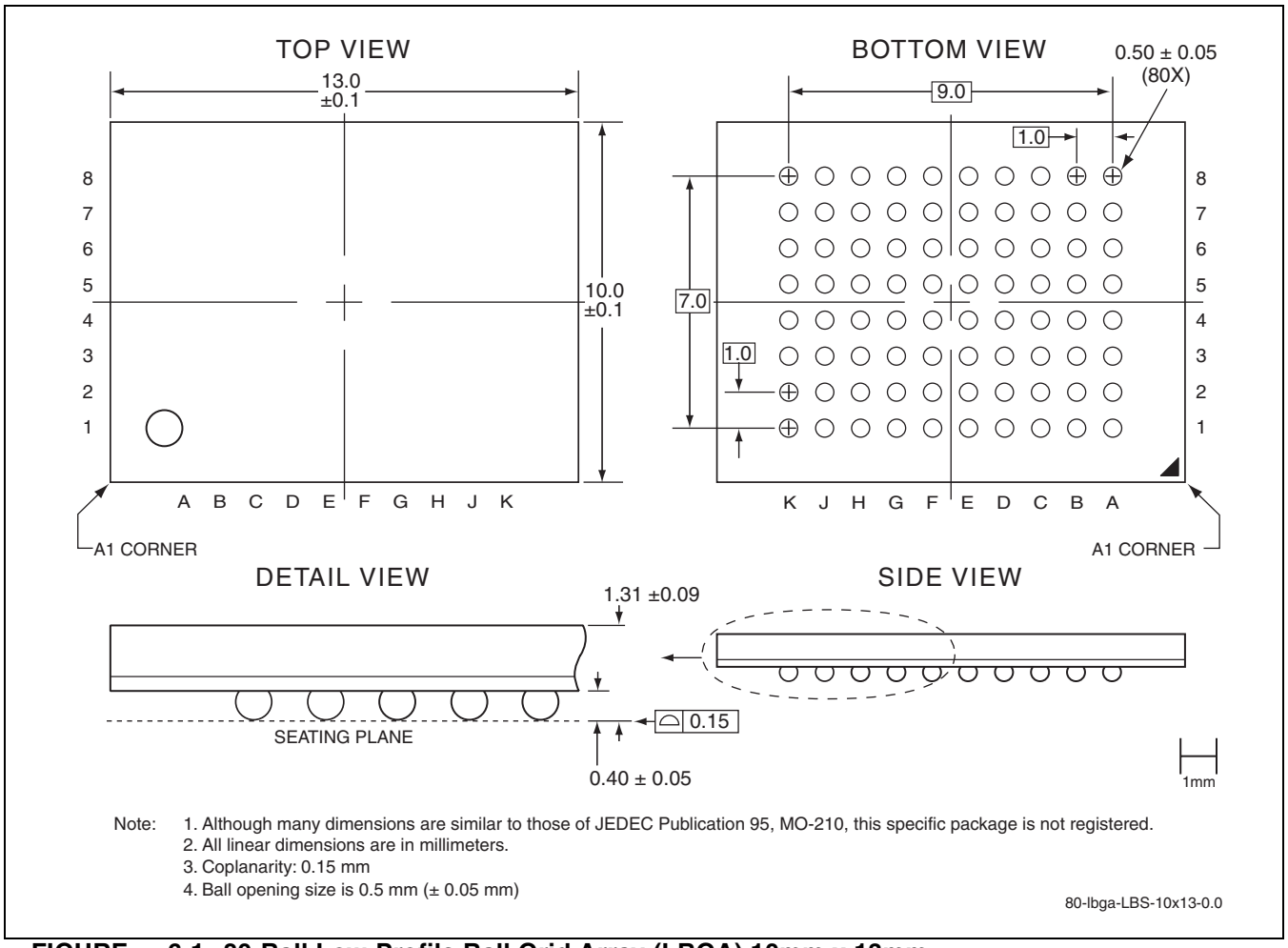


FIGURE 6-1: 80-Ball Low-Profile Ball Grid Array (LBGA) 10mm x 13mm
SST Package Code: LBS

TABLE 6-1: Revision History

Number	Description	Date
00	• Initial Release of Fact Sheet	Jul 2007