TEMIC Semiconductors

TSS901E

Intelligent and Flexible IEEE 1355 Communication Controller for Space

Description and Applications

The TSS901E provides an interface between a Data-Strobe link - according to the IEEE Std 1355-1995 specification carrying a simple interprocessor communication protocol - and a data processing node consisting of a CPU and a communication and data memory.

The TSS901E offers hardware supported execution of the major parts of the interprocessor communication protocol: data transfer between two nodes of a multi-processor system is performed with minimal host CPU intervention. The TSS901E can execute simple commands to provide basic features for system control functions; a provision of fault tolerant features exists as well.

Although the TSS901E initial exploitation is for use in multi-processor systems where the high speed links standardisation is an important issue and where reliability is a requirement, it could be used in applications such as heterogeneous systems or modules without any communication feature like special image compression chips, some signal processors, application specific programmable logic or mass memory.

The TSS901E may also be used in single board systems where standardised high speed interfaces are needed and systems containing "non-intelligent" modules such as A/D-converter or sensor interfaces which can be assembled with the TSS901E thanks to the "control by link" feature.

Features

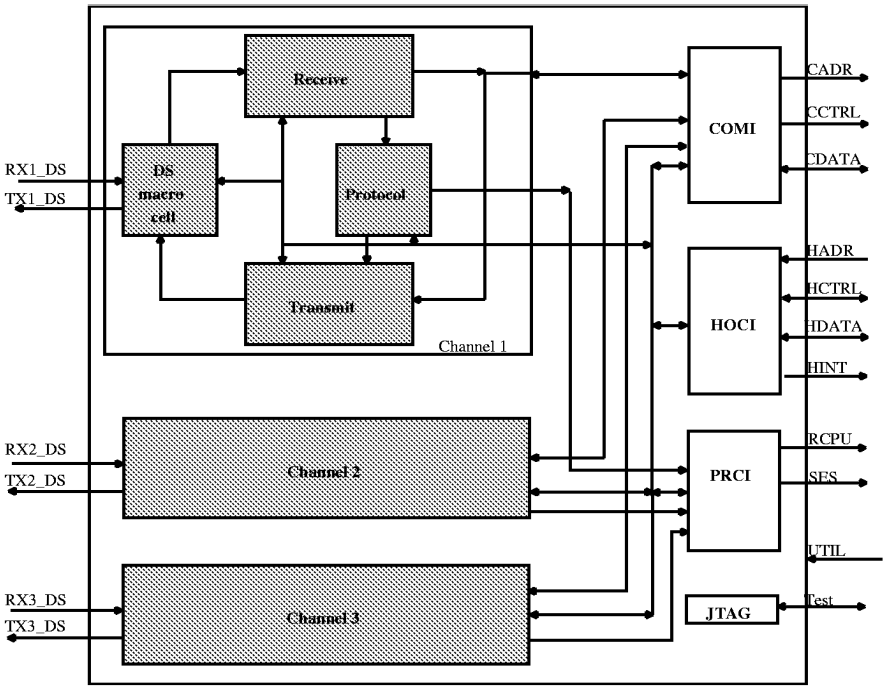
- 3 identical bidirectional link channels allowing full duplex communication under selectable transmit rate from 1.25 up to 200 Mbit/s in each direction
- a COmmunication Memory Interface (COMI) provides autonomous accesses to a communication memory which are controlled by an arbitration unit, allowing two TSS901E to share one Dual Port Ram without external arbitration
- the scalable databus width (8/16/32 bit) allows flexible integration with any CPU type
- little or big endian mode is configurable
- a HOst Control Interface (HOCI) gives read/write accesses to the TSS901E configuration registers and to the DS-link channels for the controlling CPU
- device control via one of the three links allows its use in systems without a local controller
- link disconnect detection and parity check at token (data and control) level; possible checksum generation for packet level check
- power saving mode relying on automatic transmit rate reduction
- a user's manual of the TSS901E (also called SMCS332) is available at:
  http://www.omimo.be/companies/dasa_000.htm

1. Introduction

The TSS901E provides an interface between a Data-Strobe link according to the IEEE Std 1355-1995 specification carrying the simple interprocessor communication protocol[1] and a data processing node consisting of a CPU and communication and data memory. The TSS901E provides HW supported execution of the major parts of the simple interprocessor communication protocol, particularly:

- transfer of data between two modes of a multi-processor system with minimal host CPU intervention,
- execution of simple commands to provide basic features for system control functions,
- provision of fault tolerant features.

However, with disabling of features such as the protocol handling or with reduction of the transmit rate (TSS901E automatically reduces transmit rate for sending null tokens) also low power usage is supported.



Target applications are heterogeneous multi-processor systems supported by scalable interfaces including the little/ big endian swapping. The TSS901E connects modules with different processors (e.g. 21020F, ERC32, TSC695E and others). Any kind of network topology could be realized through the high speed point-to-point IEEE1355-links (see chapter Applications).

1. Rastetter P. et.al., Simple Interprocessor Communication Protocol Specification, DIPSAPII-DAS-31-01, Issue 3, 08.10.96, also available on the same web site as the users guide.

1.1 Interfaces

The TSS901E consists of the following blocks (See TSS901E block diagram):

- **bidirectional link channels**, all comprising the DS-link macro cell (DSM), receive and transmit sections (each including FIFOs) and a protocol processing unit (PPU). Each channel allows full duplex communication up to 200 Mbit/s in each direction. With protocol command execution a higher level of communication is supported. Link disconnect detection and parity check at token level are performed. A checksum generation for a check at packet level can be enabled.

  The transmit rate is selectable between 1.25 and 200 Mbit/s; an additional power saving mode can be enabled, where the transmit rate is automatically reduced to 10 Mbit/s when only Null tokens are being transmitted over the link. The default transmit rate is 10 Mbit/s. For special applications the data transmit rate can be programmed to values even below 10 Mbit/s; the lowest possible (to be within the IEEE-1355 specification) transmit rate is 1.25 Mbit/s (the next values are 2.5 and 5 Mbit/s).

- **Communication Memory Interface (COMI)** performs autonomous accesses to the communication memory of the module to store data received via the links or to read data to be transmitted via the links. The COMI consists of individual memory address generators for the receive and transmit direction of every DS link channel. The access to the memory is controlled via an arbitration unit providing a fair arbitration scheme. Two TSS901E can share one DPRAM without external arbitration.

  The data bus width is scalable (8/16/32 bit) to allow flexible integration with any CPU type.

  Operation in little or big endian mode is configurable through internal registers.

  The COMI address bus is 16 bit wide allowing direct access of up to 64K words of the DPRAM. Two chip select signals are provided to allow splitting of the 64k address space in two memory banks.

- **Host Control Interface (HOCI)** gives read and write access to the TSS901E configuration registers and to the DS-link channels for the controlling CPU. Viewed from the CPU, the interface behaves like a peripheral that generates acknowledges to synchronize the data transfers and which is located somewhere in the CPU's address space.

  Packets can be transmitted or received directly via the HOCI. In this case the Communication Memory (DPRAM) is not strictly needed. However, in this case the packet size should be limited to avoid frequent CPU interaction.

  The data bus width is scalable (8/16/32 bit) to allow flexible integration with any CPU type. The byte alignment can be configured for little or big endian mode through an external pin.

  Additionally the HOCI contains the interrupt signalling capability of the TSS901E by providing an interrupt output, the interrupt status register and interrupt mask register to the local CPU.

  A special pin is provided to select between control of the TSS901E by HOCI or by link. If control by link is enabled, the host data bus functions as a 32-bit general purpose interface (GPIO).

- **Protocol Command Interface (PRCI)** that collects the decoded commands from all PPUs and forwards them to external circuitry via 5 special pins.

- **JTAG Test Interface** that represents the boundary scan testing provisions specified by IEEE Standard 1149.1 of the Joint Testing Action Group (JTAG). The TSS901E' test access port and on-chip circuitry is fully compliant with the IEEE 1149.1 specification. The test access port enables boundary scan testing of circuitry connected to the TSS901E I/O pins.

1.2 Operation Modes

According to the different protocol formats expected for the operation of the TSS901E, two major operation modes are implemented into the TSS901E. The operation modes are chosen individually for each link channel by setting the respective configuration registers via the HOCI or via the link.

- **Transparent Mode (default after reset):** This mode allows complete transparent data transfer between two nodes without performing any interpretation of the databytes and without generating any acknowledges. It is completely up to the host CPU to interpret the received data and to generate acknowledges if required.

  The TSS901E accepts EOP1 and EOP2 control tokens as packet delimiters and generates autonomously EOP1/ EOP2 (as configured) markers after each end of a transmission packet.

  This mode also includes as a special submode:

  - **Wormhole routing:** This mode allows hardware routing of packets by the TSS901E.

- **Simple Interprocessor Communication (SIC) Protocol Mode:** This mode executes the simple interprocessor communication protocol as described in the protocol specification[1]. The following capabilities of the protocol are implemented into the TSS901E:

  - interpretation of the first 4 data tokens as the header bytes of the protocol
  - autonomous execution of the simple control commands as described in the protocol specification[1]
  - autonomous acknowledgement of received packets if configured

  In transmit direction no interpretation of the data is performed. This means that for transmit packets, the four header bytes must be generated by the host CPU and must be available as the first data read from the communication memory. EOP1/EOP2 control tokens are automatically inserted by the TSS901E when one configured transfer from the communication memory has finished.

1.3 TSS901E Control by Link

A feature of the TSS901E is the possibility to control the TSS901E not only via HOCI but via one of the three links. This allows to use the TSS901E in systems without a local controller (Controller, FPGA etc.). Since the HOCI is no longer used in this operation mode, it is instead available as a set of general purpose I/O (GPIO) lines.

1.4 Wormhole Routing

The TSS901E introduces a wormhole routing function similar to the routing implemented in the ST-Microelectronics C104 routing switch. Each of the three links and the TSS901E itself can be assigned an eight bit address. When routing is enabled in the TSS901E, the first byte of a packet will be interpreted as the address destination byte, analysed and removed from the packet (header deletion). If this address matches one of the two other link addresses or the TSS901E address assigned previously, the packet will be automatically forwarded to this link or the FIFO of the TSS901E. If the header byte does not match a link address, the packet will be written to the internal FIFO as well and an error interrupt (maskable) will be raised.

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1. Rastetter P. et.al., Simple Interprocessor Communication Protocol Specification, DIPSAPII-DAS-31-01, Issue 3, 08.10.96, also available on the same web site as the users guide.

1.5 PPU Functional Description

Since the Protocol Processing Unit (PPU) determines a major part of the TSS901E functionality, the principal blocks of the PPU and their function are described here. This functionality is provided for every DS link channel of the TSS901E.

- **Protocol Execution Unit:** This unit serves as the main controller of the PPU block. It receives the tokens from the DS macrocell and interprets (in protocol mode) the four header data characters received after an EOP1/ EOP2 control character. If the address field matches the link channel address and the command field contains a valid command then forwarding of data into the receive FIFO is enabled. If the command field contains a "simple control command" then the execution request is forwarded to the command execution unit.

  The protocol execution unit also enables forwarding of header data characters to the acknowledge generator and provides an error signal in case of address mismatch, wrong commands or disabled safety critical "simple control commands".

  The protocol execution unit is disabled in "transparent" or “wormhole routing” operation mode.

- **Receive, Transmit, Acknowledge:** The transmit and receive FIFOs decouple the DS link related operations from the TSS901E related operations in all modes and such allows to keep the speed of the different units even when the source or sink of data is temporarily blocked.

  In the protocol mode a further FIFO (acknowledge FIFO) is used to decouple sending of acknowledges from receiving new data when the transmit path is currently occupied by a running packet transmission.

- **Command Execution Unit:** This unit performs activating resp. deactivating of the CPU reset and the specific external signals and provides the capability to reset one or all links inside the TSS901E, all actions requested by the decoded commands from the protocol execution unit.

  The unit contains a register controlling the enable/disable state of safety critical commands which is set into the 'enable' state upon command request and which is reset after a safety critical command has been executed.

  The CPU reset and the specific external signals are forwarded to the Protocol Command Interface (PRCI).

1.6 Fault Tolerance

The IEEE Std 1355-1995 specifies low level checks as link disconnect detection and parity check at token level. The TSS901E provides, through the Protocol Processing Unit, features to reset a link or all links inside the TSS901E, to reset the local CPU or to send special signals to the CPU commanded via the links.

Additionally it is possible to enable a checksum coder/decoder to have fault detection capabilities at packet level.

1.7 Applications

The TSS901E is a very high speed, scalable link-interface chip with fault tolerance features. The initial exploitation is for use in multi-processor systems where the standardisation or the high speed of the links is an important issue and where reliability is a requirement. Further application examples are heterogeneous systems or modules without any communication features as special image compression chips, certain signal processors (TSC21020F, ERC32, ...), application specific programmable logic or mass memory.

The TSS901E could also be used for single board systems where standardised high speed interfaces are needed. Even "non-intelligent" modules such as A/D-converter or sensor interfaces can be assembled with the TSS901E because of the "control by link" feature. The complete control of the TSS901E can be done via link from a central controller-node.

2. Register Set

This chapter describes the TSS901E registers which can be read or written by the HOCI or via the link (in case the "control by link" is enabled) to control TSS901E operations. All TSS901E control operations are performed by writes or reads of the respective registers. Most of the control operations are obvious from the content of the registers.

General Conventions:

- bit 0 (D0) = least significant bit,
- bit 7 (D7) = most significant bit (or bit 15 resp. bit 31)
- D x:0 means data bit x until bit 0.

2.1 Access by HOCI: HOCI data transfer

Big/Little endian selection of the HOCI is done using a special pin (HOSTBIGE) of the TSS901E. By connecting this pin to either Vcc or GND the HOCI is configured to be in little or big endian mode as follows:

When Signal HOSTBIGE = '0' (GND), the HOCI data port is in little endian mode.
When Signal HOSTBIGE = '1' (Vcc), the HOCI data port is in big endian mode.

Little endian mode selected:

- **8 bit data port (default after reset)**
  - register byte 0 is connected with pin HDATA0 - HDATA7
- **16 bit data port**
  - register byte 0 is connected with pin HDATA0 - HDATA7
  - register byte 1 is connected with pin HDATA8 - HDATA15
- **32 bit data port**
  - register byte 0 is connected with pin HDATA0 - HDATA7
  - register byte 1 is connected with pin HDATA8 - HDATA15
  - register byte 2 is connected with pin HDATA16 - HDATA23
  - register byte 3 is connected with pin HDATA24 - HDATA31

Big endian mode selected:

- **8 bit data port (default after reset)**
  - register byte 0 is connected with pin HDATA24 - HDATA31

- **16 bit data port**
  - register byte 0 is connected with pin HDATA24 - HDATA31
  - register byte 1 is connected with pin HDATA16 - HDATA23

- **32 bit data port**
  - register byte 0 is connected with pin HDATA24 - HDATA31
  - register byte 1 is connected with pin HDATA16 - HDATA23
  - register byte 2 is connected with pin HDATA8 - HDATA15
  - register byte 3 is connected with pin HDATA0 - HDATA7

The registers of the TSS901E are 1, 2 or 4 Bytes wide. That means, if the HOCI data port is in 8 bit mode, 4 read or write accesses are necessary to access a 4 Byte register (e. g. the interrupt mask register). In 16/32 bit mode the data bits 31 - 8 are '0' if an 8 bit register is read.

2.2 Register Address Map

The addresses of the TSS901E registers are directly mapped with pins HADR7 - 0. The tables below shows the addresses of all the TSS901E registers depending on the HOCI port width.

2.2.1 TSS901E status and control registers

Port Width / Address (hex)			Register	Function	Reset Value (hex)	Access
32	16	8				
00	00	00	SICR	TSS901E Interface Control Register	00	r / w
01	01	01	TRS_CTRL	Transmit-Speed-Base Register	0A	r / w
02	02	02	ROUTE_CTRL	Routing Enable / Status Register	00	r
03	03	03		reserved	00	
04	04 06	04 05 06 07	ISR	Interrupt Status Register	04010040	ro
08	08 0A	08 09 0A 0B	IMR	Interrupt Mask Register	00000000	r / w
0C	0C	0C	COMI_CS0R	COMI Chip Select 0 upper address boundary Register	FF	r / w
0D	0D	0D		reserved	00	
0E	0E	0E	COMI_ACR	COMI Arbitration Control Register	08	r / w
0F	0F	0F	PRCIR	PRCI Register	00	r / w

2.2.2 TSS901E channel 1 status and control registers

Port Width / Address (hex)			Register	Function	Reset Value (hex)	Access
32	16	8				
10	10	10	CH1_DSM_MODR	channel 1 DSM mode Register	03	r / w
11	11	11	CH1_DSM_CMDR	channel 1 DSM command Register	00	r / w
12	12	12	CH1_DSM_STAR	channel 1 DSM status Register	00	r / w
13	13	13	CH1_DSM_TSTR	channel 1 DSM test Register	00	r / w
14	14	14	CH1_ADDR	channel 1 address Register	00	r / w
15	15	15	CH1_RT_ADDR	channel 1 Route Address Register	00	r / w
16	16	16	CH1_PR_STAR	channel 1 Protocol Status Register	04	r / w
17	17	17		reserved	00	---
18	18	18	CH1_CNTRL1	channel 1 control Register 1	00	r / w
19	19	19	CH1_CNTRL2	channel 1 control Register 2	00	r / w
1A	1A	1A	CH1_HTID	channel 1 Header Transaction ID byte	00	ro
1B	1B	1B	CH1_HCNTRL	channel 1 Header control byte	00	ro
1C	1C	1C	CH1_ESR1	channel 1 detailed error source register 1	00	r / w
1D	1D	1D	CH1_ESR2	channel 1 detailed error source register 2	00	r / w
1E	1E	1E		reserved	00	---
1F	1F	1F	CH1_COMICFG	channel 1 COMI configuration register	00	r / w
20	20	20 21	CH1_TX_SAR	channel 1 transmit Start Address Register	0000	r / w
22	22	22 23	CH1_TX_EAR	channel 1 transmit End Address Register	0000	r / w
24	24	24 25	CH1_TX_CAR	channel 1 transmit Current Address Register	0000	ro
26	26	26	CH1_TX_FIFO	channel 1 transmit FIFO	--	wo
27	27	27	CH1_TX_EOPB	channel 1 transmit EOP Bit Register	--	wo
28	28	28 29	CH1_RX_SAR	channel 1 receive Start Address Register	0000	r / w
2A	2A	2A 2B	CH1_RX_EAR	channel 1 receive End Address Register	0000	r / w
2C	2C	2C 2D	CH1_RX_CAR	channel 1 receive Current Address Register	0000	ro
2E	2E	2E	CH1_RX_FIFO	channel 1 receive FIFO	xxxxxxxx	ro
2F	2F	2F	CH1_STAR	channel 1 Status Register	01	ro

2.2.3 TSS901E channel 2 status and control registers

Port Width / Address (hex)			Register	Function	Reset Value (hex)	Access
32	16	8				
30	30	30	CH2_DSM_MODR	channel 2 DSM mode Register	03	r / w
31	31	31	CH2_DSM_CMDR	channel 2 DSM command Register	00	r / w
32	32	32	CH2_DSM_STAR	channel 2 DSM status Register	00	r / w
33	33	33	CH2_DSM_TSTR	channel 2 DSM test Register	00	r / w
34	34	34	CH2_ADDR	channel 2 address Register	00	r / w
35	35	35	CH2_RT_ADDR	channel 2 Route Address Register	00	r / w
36	36	36	CH2_PR_STAR	channel 2 Protocol Status Register	04	r / w
37	37	37		reserved	00	
38	38	38	CH2_CNTRL1	channel 2 control Register 1	00	r / w
39	39	39	CH2_CNTRL2	channel 2 control Register 2	00	r / w
3A	3A	3A	CH2_HTID	channel 2 Header Transaction ID byte	00	ro
3B	3B	3B	CH2_HCNTRL	channel 2 Header control byte	00	ro
3C	3C	3C	CH2_ESR1	channel 2 detailed error source register 1	00	r / w
3D	3D	3D	CH2_ESR2	channel 2 detailed error source register 2	00	r / w
3E	3E	3E		reserved	00	
3F	3F	3F	CH2_COMICFG	channel 2 COMI configuration register	00	r / w
40	40	40 41	CH2_TX_SAR	channel 2 transmit Start Address Register	00	r / w
42	42	42 43	CH2_TX_EAR	channel 2 transmit End Address Register	00	r / w
44	44	44 45	CH2_TX_CAR	channel 2 transmit Current Address Register	00	ro
46	46	46	CH2_TX_FIFO	channel 2 transmit FIFO	00	wo
47	47	47	CH2_TX_EOPB	channel 2 transmit EOP Bit Register	00	wo
48	48	48 49	CH2_RX_SAR	channel 2 receive Start Address Register	00	r / w
4A	4A	4A 4B	CH2_RX_EAR	channel 2 receive End Address Register	00	r / w
4C	4C	4C 4D	CH2_RX_CAR	channel 2 receive Current Address Register	00	ro
4E	4E	4E	CH2_RX_FIFO	channel 2 receive FIFO	xxxxxxxx	ro
4F	4F	4F	CH2_STAR	channel 2 Status Register	01	ro

2.2.4 TSS901E channel 3 status and control registers

Port Width / Address (hex)			Register	Function	Reset Value (hex)	Access
32	16	8				
50	50	50	CH3_DSM_MODR	channel 3 DSM mode Register	03	r / w
51	51	51	CH3_DSM_CMDR	channel 3 DSM command Register	00	r / w
52	52	52	CH3_DSM_STAR	channel 3 DSM status Register	00	r / w
53	53	53	CH3_DSM_TSTR	channel 3 DSM test Register	00	r / w
54	54	54	CH3_ADDR	channel 3 address Register	00	r / w
55	55	55	CH3_RT_ADDR	channel 3 Route address Register	00	r / w
56	56	56	CH3__PR_STAR	channel 3 Protocol Status Register	04	r / w
57	57	57		reserved	00	
58	58	58	CH3_CNTRL1	channel 3 control Register 1	00	r / w
59	59	59	CH3_CNTRL2	channel 3 control Register 2	00	r / w
5A	5A	5A	CH3_HTID	channel 3 Header Transaction ID byte	00	ro
5B	5B	5B	CH3_HCNTRL	channel 3 Header control byte	00	ro
5C	5C	5C	CH3_ESR1	channel 3 detailed error source register 1	00	r / w
5D	5D	5D	CH3_ESR2	channel 3 detailed error source register 2	00	r / w

Port Width / Address (hex)			Register	Function	Reset Value (hex)	Access
32	16	8				
5E	5E	5E		reserved	00	
5F	5F	5F	CH3_COMICFG	channel 3 COMI configuration register	00	r / w
60	60	60 61	CH3_TX_SAR	channel 3 transmit Start Address Register	00	r / w
62	62	62 63	CH3_TX_EAR	channel 3 transmit End Address Register	00	r / w
64	64	64 65	CH3_TX_CAR	channel 3 transmit Current Address Register	00	ro
66	66	66	CH3_TX_FIFO	channel 3 transmit FIFO	00	wo
67	67	67	CH3_TX_EOPB	channel 3 transmit EOP Bit Register	00	wo
68	68	68 69	CH3_RX_SAR	channel 3 receive Start Address Register	00	r / w
6A	6A	6A 6B	CH3_RX_EAR	channel 3 receive End Address Register	00	r / w
6C	6C	6C 6D	CH3_RX_CAR	channel 3 receive Current Address Register	00	ro
6E	6E	6E	CH3_RX_FIFO	channel 3 receive FIFO	xxxxxxxx	ro
6F	6F	6F	CH3_STAR	channel 3 Status Register	01	ro

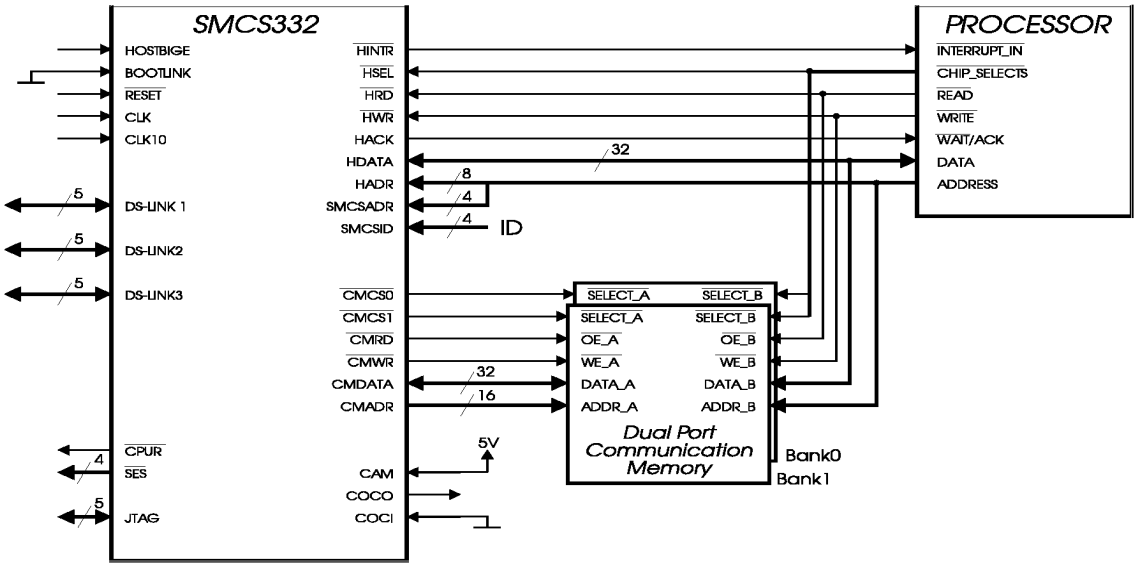
2.2.5 TSS901E GPIO control registers

These registers are only enabled when the TSS901E is configured for "control by link" using the 'BOOTLINK' pin.

Port Width / Address (hex)			Register	Function	Reset Value (hex)	Access
32	16	8				
		70	GPIO_DIR0	GPIO direction register 0	00	r / w
		71	GPIO_DIR1	GPIO direction register 1	00	r / w
		72	GPIO_DIR2	GPIO direction register 2	00	r / w
		73	GPIO_DIR3	GPIO direction register 3	00	r / w
		74	GPIO_DATA0	GPIO data register 0	00	r / w
		75	GPIO_DATA1	GPIO data register 1	00	r / w
		76	GPIO_DATA2	GPIO data register 2	00	r / w
		77	GPIO_DATA3	GPIO data register 3	00	r / w

3. Signal Description

The Figure below shows the TSS901E (also called SMCS332) embedded in a typical module environment:



This section describes the pins of the TSS901E. Groups of pins represent busses where the highest number is the MSB.

O = Output; I = Input; Z = High Impedance; (*) = active low signal
O/Z = if using a configuration with two TSS901Es these signals can directly be connected together (WIROR)

Signal Name	Type	Function	max. output current [mA]	load [pF]
HSEL*	I	Select host interface		
HRD*	I	host interface read strobe		
HWR*	I	host interface write strobe		
HADR(7:0)	I	TSS901E register address lines. This address lines will be used to access (address) the TSS901E registers.		
HDATA(31:0)	IO/Z	TSS901E data	3	50
HACK	O/Z	host acknowledge. TSS901E deasserts this output to add wait states to a TSS901E access. After TSS901E is ready this output will be asserted.	3	50
HINTR*	O/Z	host interrupt request line	3	50
TSS901EADR(3:0)	I	TSS901E Address. The binary value of this lines will be compared with the value of the TSS901E ID lines.		
TSS901EID(3:0)	I	TSS901E ID lines: offers possibility to use sixteen TSS901E within one HSEL*		
HOSTBIGE	I	1: host I/F Big Endian 0: host I/F Little Endian		
BOOTLINK	I	1: control by link 0: control by host		
CMCS(1:0)*	O/Z	Communication memory select lines. These pins are asserted as chip selects for the corresponding banks of the communication memory.	8	25

Signal Name	Type	Function	max. output current [mA]	load [pF]
CMRD*	O/Z	Communication memory read strobe. This pin is asserted when the TSS901E reads data from memory.	8	25
CMWR*	O/Z	Communication memory write strobe. This pin is asserted when the TSS901E writes to data memory.	8	25
CMADR(15:0)	O/Z	Communication memory address. The TSS901E outputs an address on these pins.	8	25
CMDATA(31:0)	IOZ	Communication memory data. The TSS901E inputs and outputs data from and to com. memory on these pins.	3	50
COCI	I	Communication interface 'occupied' input signal	3	50
COCO	O/Z	Communication interface 'occupied' output signal		
CAM	I	Communication interface arbitration master input signal 1: master 0: slave		
CPUR*	O/Z	CPU Reset Signal	3	50
SES(3:0)*	O/Z	Specific External Signals	3	50
LDI1	I	Link Data Input channel 1		
LSI1	I	Link Strobe Input channel 1		
LDO1	O/Z	Link Data Output channel 1	12	25
LSO1	O/Z	Link Strobe Output channel 1	12	25
LEN1	O/Z	Link Enable Out (for external drivers)	3	50
LDI2	I	Link Data Input channel 2		
LSI2	I	Link Strobe Input channel 2		
LDO2	O/Z	Link Data Output channel 2	12	25
LSO2	O/Z	Link Strobe Output channel 2	12	25
LEN2	O/Z	Link Enable Out (for external drivers)	3	50
LDI3	I	Link Data Input channel 3		
LSI3	I	Link Strobe Input channel 3		
LDO3	O/Z	Link Data Output channel 3	12	25
LSO3	O/Z	Link Strobe Output channel 3	12	25
LEN3	O/Z	Link Enable Out (for external drivers)	3	50
TRST*	I	Test Reset. Resets the test state machine.		
TCK	I	Test Clock. Provides an asynchronous clock for JTAG boundary scan.		
TMS	I	Test Mode Select. Used to control the test state machine.		
TDI	I	Test Data Input. Provides serial data for the boundary scan logic.		
TDO	O/Z	Test Data Output. Serial scan output of the boundary scan path.	3	50
RESET*	I	TSS901E Reset. Sets the TSS901E to a known state. This input must be asserted (low) at power-up. The minimum width of RESET low is 5 cycles of CLK10 in parallel with CLK running.		
CLK	I	External clock input to TSS901E (max. 25 Mhz). Must be derived from RAM access time.		
CLK10	I	External clock input to TSS901E DS-links (application specific, nominal 10 Mhz). Used to generate to transmission speed and link disconnect timeout.		
PLLOUT	O	Output of internal PLL. Used to connect a network of external RC devices.		
VCC		Power Supply		
GND		Ground		

4. Electrical Specifications

Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Supply Voltage	V_{CC}	-0.5 to +7	V
I/O Voltage		-0.5 to VCC + 0.5	V
Operating Temperature Range (Ambient)	T_A	-55 to +125	C
Junction Temperature	T_J	$T_J < T_A$ +20	C
Storage Temperature Range	T_{stg}	-65 to +150	C

Stresses above those listed may cause permanent damage to the device.

DC Electrical Characteristics

Specified at V_{CC} = + 5 V 10% (TSS901E will only work with 5V $_{CC}$)

Parameter	Symbol	Min.	Max.	Unit	Conditions
Operating Voltage	V_{CC}	4.5	5.5	V	
Input HIGH Voltage	V_{IH}	2.0		V	
Input LOW Voltage	V_{IL}		0.8	V	
Output HIGH Voltage	V_{OH}	2.4		V	max. output current
Output LOW Voltage	V_{OL}		0.4	V	max. output current
Output Short circuit current	I_{OS}		160 130	mA mA	V_{OUT} = VCC V_{OUT} = GND

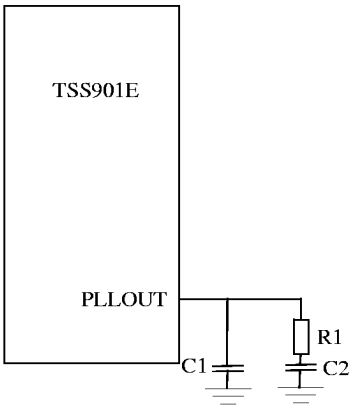
Although specified for TTL outputs, all TSS901E outputs are CMOS compatible and will drive to VCC and GND assuming no dc loads.

Max. power consumption figures (at 5.5V, 125 C) are:

Operation Mode	Power consumption [mA]
not clocked	5
TSS901E in RESET	45
TSS901E in IDLE	70
Maximum	190

4.1 PLL Filter

The pin PLLOUT should be connected as shown below:



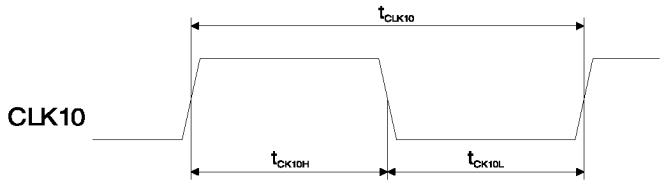
R1 = 249Ω 5%, 1/4W

C1 = 1nF, 5%, 200V

C2 = 15nF, 5%, 200V

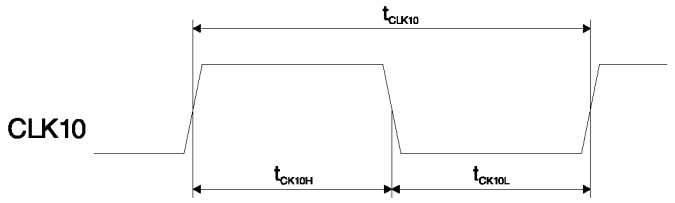
5. Timing Parameters

5.1 Clock Signals



Description	Symbol	Min.	Max.	Unit
CLK period [1]	t_{CLK}	40		ns
CLK width high	t_{CLKH}	17		ns
CLK width low	t_{CLKL}	17		ns

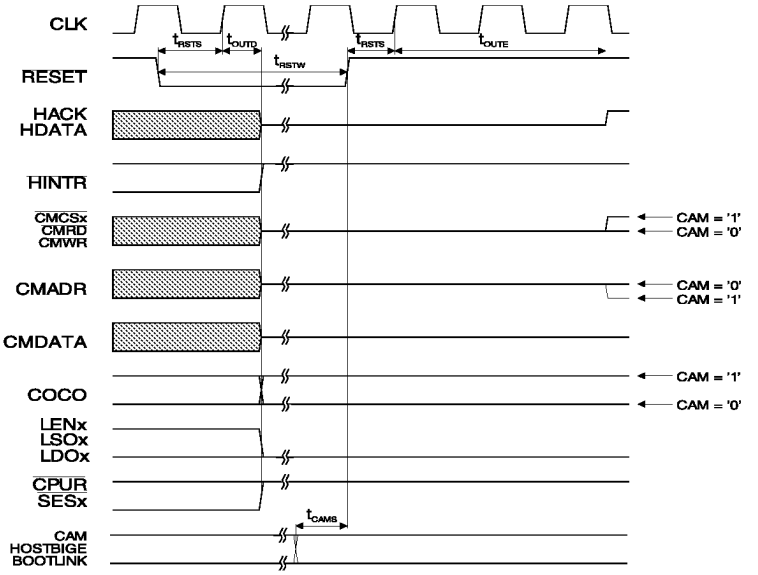
[1] *Max. 25 MHz*



Description	Symbol	Min.	Max.	Unit
CLK10 period [1]	t_{CLK10}	100	100	ns
CLK10 width high	t_{CLK10H}	40		ns
CLK10 width low	t_{CLK10L}	40		ns

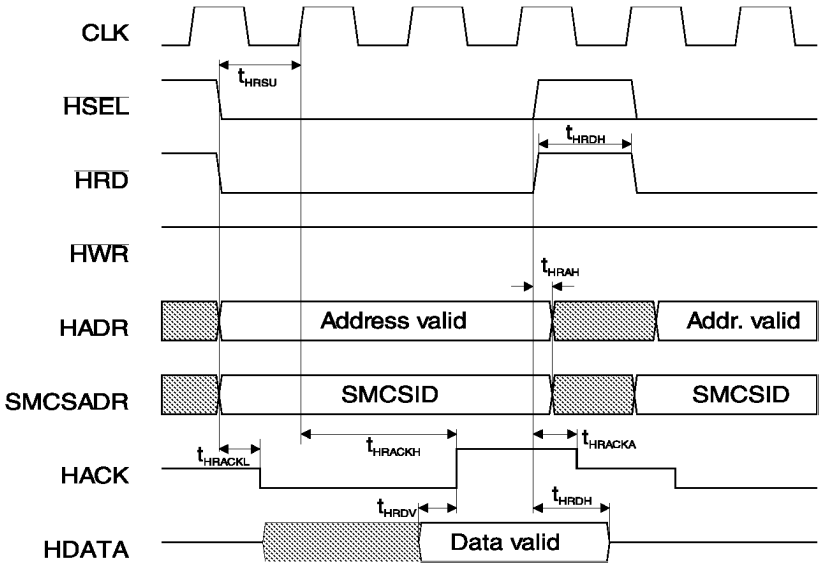
[1] *Typically 10 MHz*

5.2 Reset



Description	Symbol	Min.	Max.	Unit
RESET setup before CLK high	t_{RSTS}	5		ns
RESET low pulse width	t_{RSTW}	2 * t_{CLK}		ns
Output disable after CLK high	t_{OUTD}		42	ns
Output enable after CLK high	t_{OUTE}		2 * t_{CLK} + 26	ns
CAM, HOSTBIGE, BOOTLINK setup before RESET high	t_{CAMS}	1		

5.3 Host Read



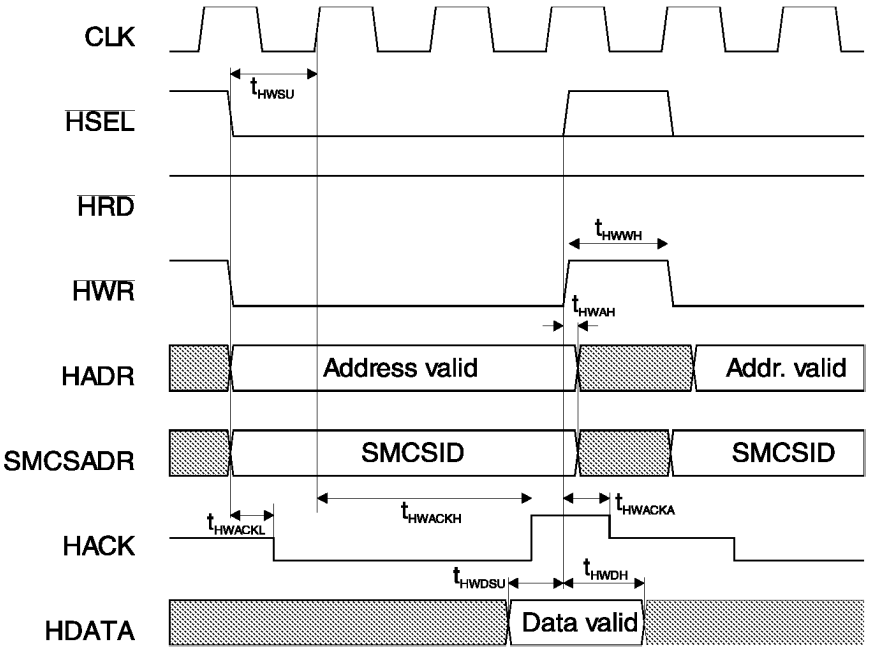
Description	Symbol	Min.	Max.	Unit
HSEL*, HRD* and TSS901EADR and HADR setup before CLK high	t_{HRSU}	5		ns
HADR, TSS901EADR hold after HSEL*, HRD* high	t_{HRAH}	0		ns
HRD* pulse width high	t_{HRDH}	5		ns
HACK low after HRD*, HSEL* active and TSS901EADR valid [1]	t_{HRACKL}		16	ns
HACK high after CLK high	t_{HRACKH}	$1 * t_{CLK} + 5$	$3 * t_{CLK} + 23$	ns
HACK disable after HRD*, HSEL* inactive or TSS901EADR invalid [2]	t_{HRACKA}		12	ns
HDATA valid before HACK high	t_{HRDV}	0		ns
HDATA hold after HRD*, HSEL* inactive or TSS901EADR invalid [2]	t_{HRDH}	5	19	ns

Notes

[1] *Signal HACK active when HRD* low* ***and*** *HSEL* low* ***and*** *TSS901EADR = TSS901EID*

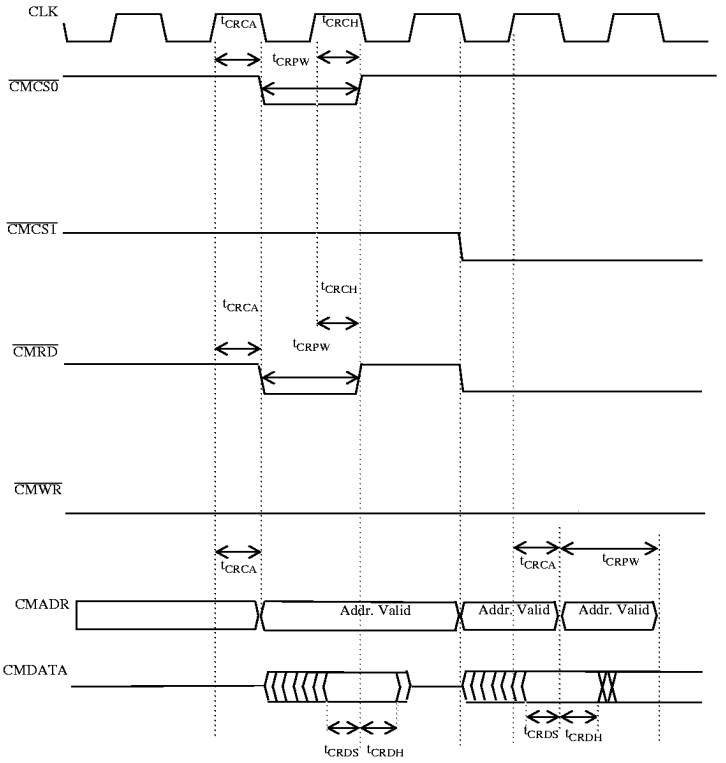
[2] *Signal HACK disable when HRD* high* ***or*** *HSEL* high* ***or*** *TSS901EADR ≠ TSS901EID*

5.4 Host Write



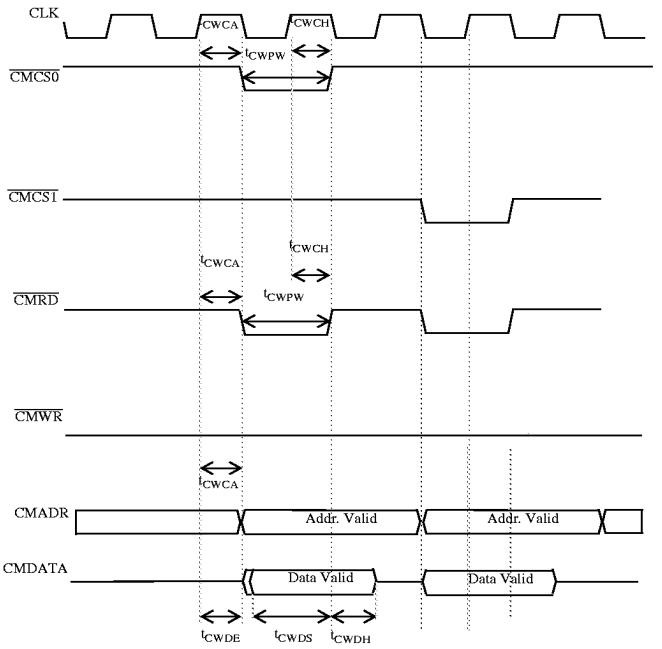
Description	Symb.	Min.	Max.	Unit
HSEL*, HWR* and TSS901EADR and HADR setup before CLK high	t_{HWSU}	5		ns
HADR, TSS901EADR hold after HSEL*, HWR* high	t_{HWAH}	0		ns
HWR* pulse width high	t_{HWWH}	$1 * t_{CLK} + 5$		ns
HACK low after HWR*, HSEL* active and TSS901EADR valid [1]	t_{HWACKL}		16	ns
HACK high after HSEL* and HWR* and TSS901EADR = TSS901EID	t_{HWACKH}	$1 * t_{CLK} + 5$	$2.5 * t_{CLK} + 24$	ns
HACK disable after HWR* or HSEL* inactive or TSS901EADR invalid [2]	t_{HWACKA}		12	ns
HDATA setup before HSEL* or HWR* high or TSS901EADR ≠ TSS901EID	t_{HWDSU}	5		ns
HDATA hold after HWR* or HSEL* inactive or TSS901EADR invalid [2]	t_{HWDH}	0		ns

5.5 COMI Read



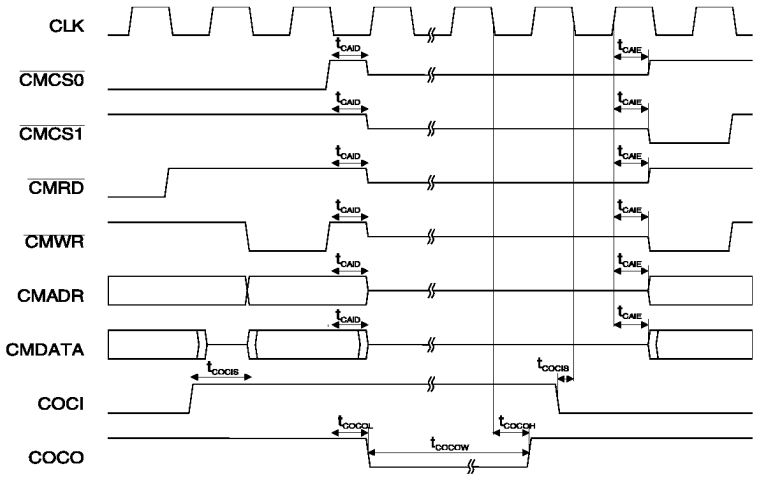
Description	Symbol	Min.	Max.	Unit
CMCS0*, CMCS1* and CMRD* low and CMADR valid after CLK high	t_{CRCA}		18	ns
CMCS0*, CMCS1* or CMRD* high after CLK high	t_{CRCH}		18	ns
CMCS0*, CMCS1*, CMRD*, CMADR pulse width	t_{CRPW}	t_{CLK} - 1		ns
CMDATA setup before CMCS0* or CMCS1* or CMRD* high or new address on CMADR	t_{CRDS}	4		ns
CMDATA hold after CMCS0* or CMCS1* or CMRD* high or new address on CMADR	t_{CRDH}	0		ns

5.6 COMI Write



Description	Symbol	Min.	Max.	Unit
CMCS0*, CMCS1* and CMWR* low and CMADR valid after CLK high	t_{CWCA}		18	ns
CMCS0*, CMCS1* or CMWR* high after CLK high	t_{CWCH}		18	ns
CMCS0*, CMCS1*, CMWR* pulse width	t_{CWPW}	t_{CLK} - 1		ns
CMDATA valid after CLK high	t_{CWDE}		15	
CMDATA valid before CMCS0* or CMCS1* or CMWR* high	t_{CWDS}	25		ns
CMDATA hold after CMCS0* or CMCS1* or CMWR* high	t_{CWDH}		$t_{CLK}/2$ + 18	ns

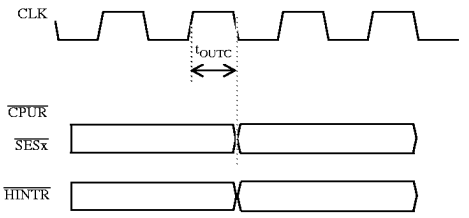
5.7 COMI Arbitration



Description	Symbol	Min.	Max.	Unit
COM Interface disable after CLK low	t_{CAID}		23	ns
COM Interface enable after CLK high	t_{CAIE}		22	ns
COCI setup before CLK low	t_{COCIS}	2		ns
COCO low after CLK low	t_{COCOL}		11	ns
COCO high after CLK high	t_{COCOH}		11	ns
COCO pulse width [3)]	t_{COCOW}		N - 1 t_{CLK}	ns

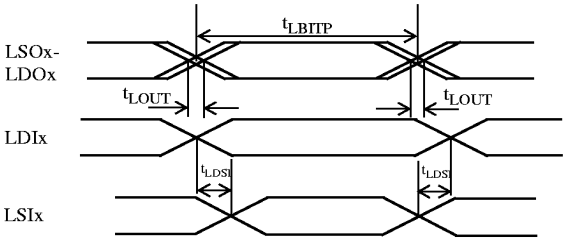
[3)] *N = content of COMI_ACR*

5.8 CPUR, SES, Interrupt



Description	Symbol	Min.	Max.	Unit
CPUR*, SESx*, HINTR* delay after CLK high	t_{OUTC}		22	ns

5.9 Links



Description	Symbol	Min.	Max.	Unit
Bit Period	t_{LBITP}	4		ns
LDOx, LSOx output skew	t_{LOUTS}		0.5	ns
Data/Strobe edge separation	t_{LDSI}		4	ns

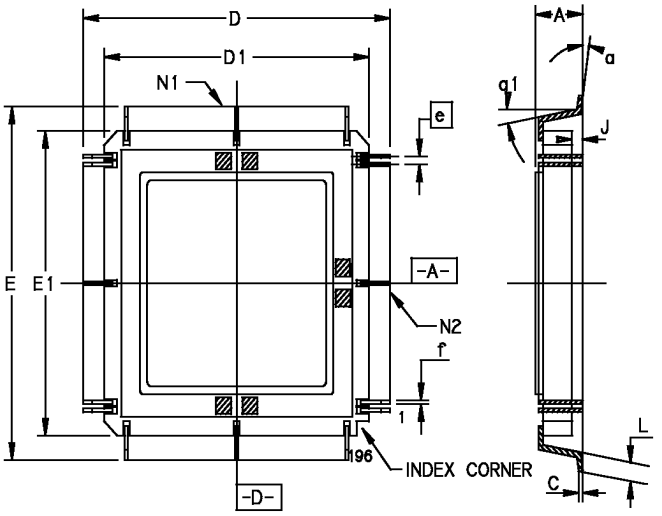
5.10 Test Port (JTAG)

Description	Symbol	Min.	Max.	Unit
TCK period	t_{TCK}	100		ns
TCK width high	t_{TCKH}	40		ns
TCK width low	t_{TCKL}	40		ns
TMS, TDI setup before TCK high	t_{TIS}	8		ns
TMS, TDI hold after TCK high	t_{TIH}	8		ns
TDO delay after TCK low	t_{TDO}		17	ns
TRST* pulse width	t_{TRST}	2 * t_{TCK}		ns
TSS901E Inputs setup before TCK high	t_{SYSS}	8		ns
TSS901E Inputs hold after TCK high	t_{SYSM}	8		ns
TSS901E Outputs delay after TCK low	t_{SYSO}		27	ns

Note: *The BSDL file is printed in the Annex of this document.*

6. Mechanical Data

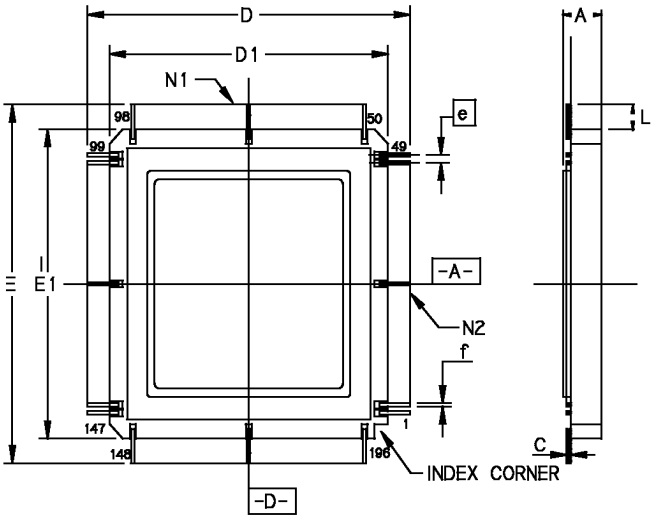
6.1 Package Dimensions



	Min	Max	Min	Max
A	-	2.95	-	.116
C	0.20 TYP		.008 TYP	
D	-	39.75	-	1.565
D1	-	34.54	-	1.360
E	-	39.75	-	1.565
E1	-	34.54	-	1.360
e	0.635 BSC		.025 BSC	
f	0.28 REF		.011 REF	
J	0.15	0.30	.006	.012
L	0.61	1.01	.024	.040
N1	49		49	
N2	49		49	
	a=4°±4°		a1=5°±5°	

Code: FX Date: 17-11-95

MQFPL 196



	mm		inch	
	Min	Max	Min	Max
A	-	2.65	-	.104
C	0.15 TYP		.006 TYP	
D	-	45.94	-	1.809
D1	-	34.54	-	1.360
E	-	45.94	-	1.809
E1	-	34.54	-	1.360
e	0.635 BSC		.025 BSC	
f	0.20 REF		.008 REF	
L	5.30	5.70	.212	.228
N1	49		49	
N2	49		49	

Code: K9 Date: 07-04-97

MQFPF 196

6.2 Pin Assignment

Pin Number	Name	Pin Number	Name	Pin Number	Name
1	VCC	67	HDATA18	133	CMDATA8
2	GND	68	HDATA19	134	VCC
3	GND	69	HDATA20	135	GND
4	CLK	70	HDATA21	136	CMDATA9
5	RESET*	71	HDATA22	137	CMDATA10
6	CLK10	72	HDATA23	138	CMDATA11
7	HOSTBIGE	73	VCC	139	CMDATA12
8	TCK	74	GND	140	CMDATA13
9	TMS	75	HDATA24	141	CMDATA14
10	TDI	76	HDATA25	142	VCC
11	TRST*	77	HDATA26	143	GND
12	TDO	78	VCC	144	CMDATA15
13	VCC	79	GND	145	CMDATA16
14	GND	80	HDATA27	146	CMDATA17
15	HSEL*	81	HDATA28	147	CMDATA18
16	HRD*	82	HDATA29	148	CMDATA19
17	HWR*	83	VCC	149	CMDATA20
18	HACK	84	GND	150	VCC
19	HINTR*	85	HDATA30	151	GND
20	VCC	86	HDATA31	152	CMDATA21
21	GND	87	CPUR*	153	CMDATA22
22	HADR0	88	SES0*	154	CMDATA23
23	HADR1	89	SES1*	155	VCC
24	HADR2	90	SES2*	156	GND
25	HADR3	91	SES3*	157	CMDATA24
26	HADR4	92	CAM	158	CMDATA25
27	HADR5	93	COCI	159	CMDATA26
28	HADR6	94	COCO	160	VCC
29	HADR7	95	CMCS0*	161	GND
30	VCC	96	CMCS1*	162	CMDATA27
31	GND	97	VCC	163	CMDATA28
32	BOOTLINK	98	GND	164	CMDATA29
33	TSS901EADR0	99	CMRD*	165	CMDATA30
34	TSS901EADR1	100	CMWR*	166	CMDATA31
35	TSS901EADR2	101	CMADR0	167	NC
36	TSS901EADR3	102	CMADR1	168	NC
37	TSS901EID0	103	CMADR2	169	NC
38	TSS901EID1	104	CMADR3	170	NC
39	TSS901EID2	105	CMADR4	171	NC
40	TSS901EID3	106	VCC	172	VCC
41	VCC	107	GND	173	GND
42	GND	108	CMADR5	174	GND
43	HDATA0	109	CMADR6	175	LEN1
44	HDATA1	110	CMADR7	176	LDI1
45	HDATA2	111	CMADR8	177	LSI1
46	HDATA3	112	CMADR9	178	LDO1
47	HDATA4	113	CMADR10	179	LSO1
48	HDATA5	114	CMADR11	180	LDI2
49	HDATA6	115	VCC	181	LSI2
50	VCC	116	GND	182	LEN2
51	GND	117	CMADR12	183	VCC
52	HDATA7	118	CMADR13	184	VCC
53	HDATA8	119	CMADR14	185	VCC
54	HDATA9	120	CMADR15	186	LDO2
55	HDATA10	121	CMDATA0	187	LSO2
56	HDATA11	122	CMDATA1	188	LDI3
57	VCC	123	CMDATA2	189	LSI3
58	GND	124	VCC	190	LDO3
59	HDATA12	125	GND	191	LSO3
60	HDATA13	126	CMDATA3	192	LEN3

Pin Number	Name	Pin Number	Name	Pin Number	Name
61	HDATA14	127	CMDATA4	193	GND
62	HDATA15	128	CMDATA5	194	GND
63	HDATA16	129	VCC	195	VCC
64	HDATA17	130	GND	196	PLLOUT
65	VCC	131	CMDATA6		
66	GND	132	CMDATA7		

7. Ordering Information