μPD424256
262,144 x 4-Bit
Dynamic CMOS RAM

Description

The μPD424256 is a fast-page dynamic RAM organized as 262,144 words by 4 bits and designed to operate from a single +5-volt power supply. Advanced polycide technology using trench capacitors minimizes silicon area and provides high storage cell capacity, high performance, and high reliability. A single-transistor dynamic storage cell and advanced CMOS circuitry throughout ensure minimum power dissipation, while an on-chip circuit generates the negative-voltage substrate bias automatically and transparently.

The three-state I/O pins are controlled by $\overline{CAS}$ independent of $\overline{RAS}$. After a valid read or read-modify-write cycle, data is held on the outputs by maintaining $\overline{CAS}$ low. The data outputs are returned to high impedance by returning $\overline{CAS}$ high. Fast-page read and write cycles can be executed by cycling $\overline{CAS}$.

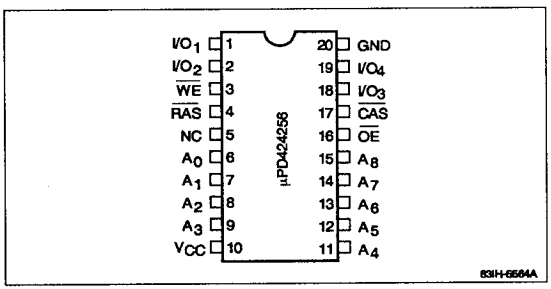
Refreshing may be accomplished by means of a $\overline{CAS}$ before $\overline{RAS}$ cycle whereby the refresh addresses are internally generated. Refreshing may also be accomplished by means of $\overline{RAS}$-only refresh cycles or by normal read or write cycles on the 512 address combinations of A_0 through A_8 during an 8-ms refresh period (64 ms for -L versions).

Features

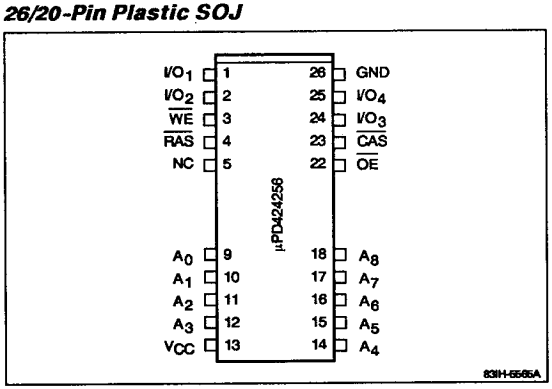
- 262,144-word by 4-bit organization
- Single +5-volt power supply
- Fast-page option
- Low power available in -L version
- $\overline{CAS}$ before $\overline{RAS}$ internal refreshing
- Multiplexed address inputs
- On-chip substrate bias generator
- Nonlatched, three-state I/O
- TTL-compatible inputs and outputs
- High-density 20-pin DIP, 26/20-pin SOJ, 20-pin ZIP, or 24/20-pin TSOP plastic packaging

Pin Configurations

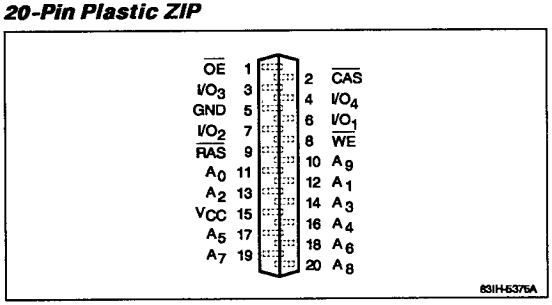
20-Pin Plastic DIP



26/20-Pin Plastic SOJ



20-Pin Plastic ZIP



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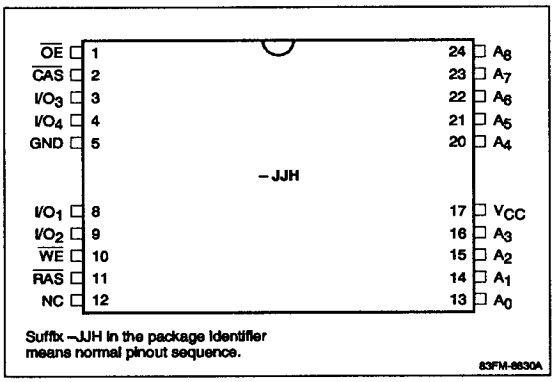
Pin Configurations (cont)

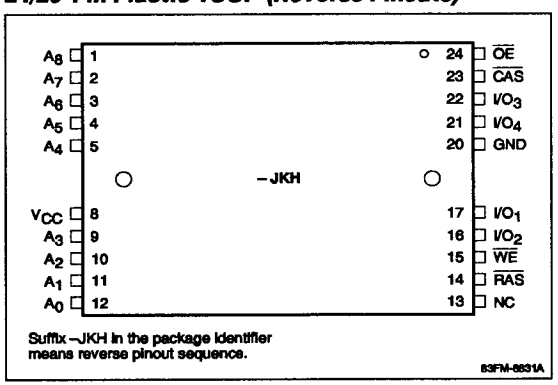
24/20-Pin Plastic TSOP (Normal Pinouts)



Suffix –JJH in the package identifier means normal pinout sequence.

83FM-8630A

24/20-Pin Plastic TSOP (Reverse Pinouts)



Suffix –JKH in the package identifier means reverse pinout sequence.

83FM-8631A

Pin Identification

Name	Function
A_0 - A_8	Address inputs
I/O_1 - I/O_4	Data inputs and outputs
$\overline{CAS}$	Column address strobe
$\overline{OE}$	Output enable
$\overline{RAS}$	Row address strobe
$\overline{WE}$	Write enable
GND	Ground
V_{CC}	+5-volt power supply
NC	No connection

Absolute Maximum Ratings

Voltage on any pin relative to GND	−1.0 to +7.0 V
Operating temperature, T_{OPR}	0 to +70°C
Storage temperature, T_{STG}	−55 to +125°C
Short-circuit output current, I_{OS}	50 mA
Power dissipation, P_D	1.0 W

Exposure to Absolute Maximum Ratings for extended periods may affect device reliability; exceeding the ratings could cause permanent damage. The device should be operated within the limits specified under DC and AC Characteristics.

Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Input voltage, high	V_{IH}	2.4		V_{CC} + 1.0	V
Input voltage, low	V_{IL}	−1.0		0.8	V
Supply voltage	V_{CC}	4.5	5.0	5.5	V
Ambient temperature	T_A	0		70	°C

Capacitance

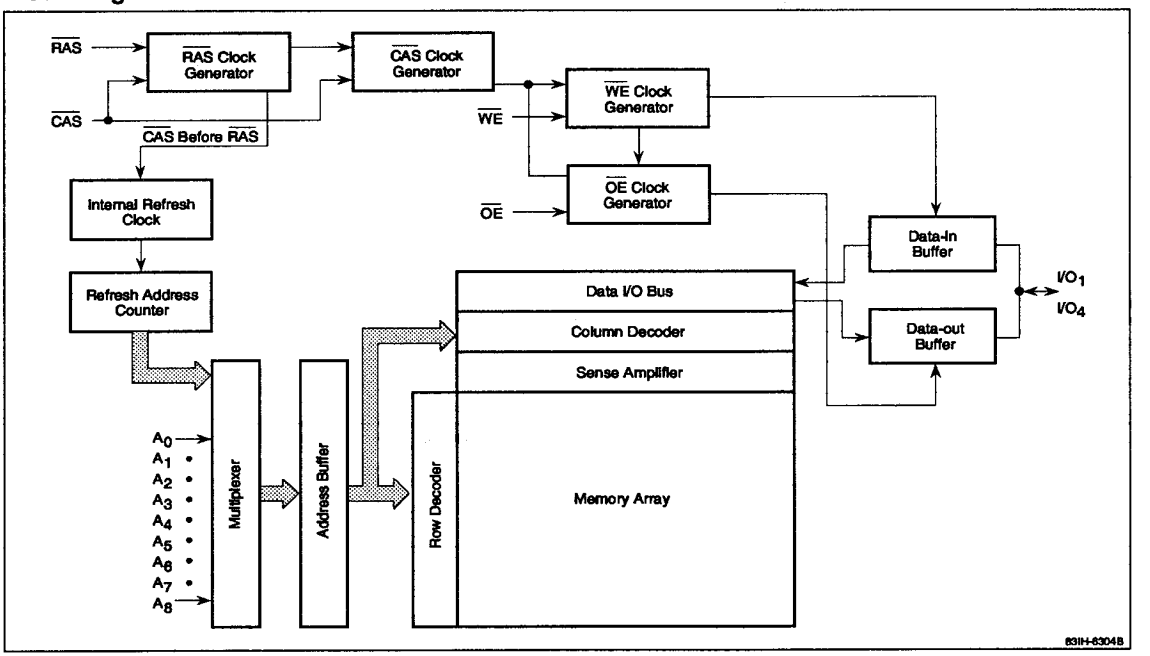
T_A = 25°C; f = 1 MHz

Parameter	Symbol	Max	Unit	Pins Under Test
Input capacitance	C_{I1}	5	pF	Address
	C_{I2}	7	pF	$\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, $\overline{OE}$
Input/output capacitance	C_{IO}	7	pF	I/O

Ordering Information

Part Number	$\overline{RAS}$ Access Time (max)	R/W Cycle Time (max)	Fast-Page Cycle (max)	Refresh Period	Standby Current (min)	Package
μPD424256C-60	60 ns	120 ns	40 ns	8 ms	1 mA	20-pin plastic DIP
C-70	70 ns	130 ns	45 ns			
C-80	80 ns	160 ns	50 ns			
C-10	100 ns	190 ns	60 ns			
μPD424256C-60L	60 ns	120 ns	40 ns	64 ms	200 μA	
C-70L	70 ns	130 ns	45 ns			
C-80L	80 ns	160 ns	50 ns			
C-10L	100 ns	190 ns	60 ns			
μPD424256LA-60	60 ns	120 ns	40 ns	8 ms	1 mA	26/20-pin plastic SOJ
LA-70	70 ns	130 ns	45 ns			
LA-80	80 ns	160 ns	50 ns			
LA-10	100 ns	190 ns	60 ns			
μPD424256LA-60L	60 ns	120 ns	40 ns	64 ms	200 μA	
LA-70L	70 ns	130 ns	45 ns			
LA-80L	80 ns	160 ns	50 ns			
LA-10L	100 ns	190 ns	60 ns			
μPD424256V-60	60 ns	120 ns	40 ns	8 ms	1 mA	20-pin plastic ZIP
V-70	70 ns	130 ns	45 ns			
V-80	80 ns	160 ns	50 ns			
V-10	100 ns	190 ns	60 ns			
μPD424256V-60L	60 ns	120 ns	40 ns	64 ms	200 μA	
V-70L	70 ns	130 ns	45 ns			
V-80L	80 ns	160 ns	50 ns			
V-10L	100 ns	190 ns	60 ns			
μPD424256GX-60	60 ns	120 ns	40 ns	8 ms	1 mA	24/20-pin plastic TSOP (normal leads)
GX-70	70 ns	130 ns	45 ns			
GX-80	80 ns	160 ns	50 ns			
GX-10	100 ns	190 ns	60 ns			
μPD424256GX-60L	60 ns	120 ns	40 ns	64 ms	200 μA	
GX-70L	70 ns	130 ns	45 ns			
GX-80L	80 ns	160 ns	50 ns			
GX-10L	100 ns	190 ns	60 ns			
μPD424256GXM-60	60 ns	120 ns	40 ns	8 ms	1 mA	24/20-pin plastic TSOP (reverse bent leads)
GXM-70	70 ns	130 ns	45 ns			
GXM-80	80 ns	160 ns	50 ns			
GXM-10	100 ns	190 ns	60 ns			
μPD424256GXM-60L	60 ns	120 ns	40 ns	64 ms	200 μA	
GXM-70L	70 ns	130 ns	45 ns			
GXM-80L	80 ns	160 ns	50 ns			
GXM-10L	100 ns	190 ns	60 ns			

Block Diagram



DC Characteristics

T_A = 0 to +70°C; V_{CC} = +5.0 V ±10%

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Standby current	I_{CC2}			2.0	mA	$\overline{RAS}$ = $\overline{CAS}$ = V_{IH}
				1.0	mA	$\overline{RAS}$ = $\overline{CAS}$ ≥ V_{CC} – 0.2 V
Input leakage current	$I_{I(L)}$	–10		10	μA	V_{IN} = 0 to 5.5 V; all other pins not under test = 0 V
Output leakage current	$I_{O(L)}$	–10		10	μA	D_{OUT} disabled; V_{OUT} = 0 to 5.5 V
Output voltage, low	V_{OL}			0.4	V	I_{OL} = 4.2 mA
Output voltage, high	V_{OH}	2.4			V	I_{OH} = –5 mA

AC Characteristics

T_A = 0 to +70 °C; V_{CC} = +5.0V ±10%

Parameter	Symbol	-60 Min	-60 Max	-70 Min	-70 Max	-80 Min	-80 Max	-10 Min	-10 Max	Unit	Test Conditions
Operating current, average	I_{CC1}		90		80		70		60	mA	$\overline{RAS}$ and $\overline{CAS}$ cycling; t_{RC} = t_{RC} min; (Note 5)
Operating current, $\overline{RAS}$-only refresh cycle, average	I_{CC3}		90		80		70		60	mA	$\overline{RAS}$ cycling; $\overline{CAS}$ = V_{IH}; t_{RC} = t_{RC} min; (Note 5)
Operating current, fast-page cycle, average	I_{CC4}		80		70		60		50	mA	$\overline{RAS}$ = V_{IL}; $\overline{CAS}$ cycling; t_{PC} = t_{PC} min; (Note 5)
Operating current, $\overline{CAS}$ before $\overline{RAS}$ refresh cycle, average	I_{CC5}		90		80		70		60	mA	$\overline{RAS}$ cycling; $\overline{CAS}$ = V_{IL}; t_{RC} = t_{RC} min; (Note 5)
Access time from column address	t_{AA}		30		35		45		50	ns	(Notes 7, 10, 13)
Access time from $\overline{CAS}$ precharge (rising edge)	t_{ACP}		35		40		45		55	ns	(Notes 7, 13)
Column address hold time referenced to $\overline{RAS}$	t_{AR}	N/A		N/A		60		70		ns	
Column address setup time	t_{ASC}	0		0		0	20	0	20	ns	(Note 13)
Row address setup time	t_{ASR}	0		0		0		0		ns	
Column address to $\overline{WE}$ delay time	t_{AWD}	50		55		70		80		ns	(Note 18)
Access time from $\overline{CAS}$ (falling edge)	t_{CAC}		20		20		20		25	ns	(Notes 7, 9, 10, 13)
Column address hold time	t_{CAH}	15		17		20		20		ns	
$\overline{CAS}$ pulse width	t_{CAS}	20	10,000	20	10,000	20	10,000	25	10,000	ns	
$\overline{CAS}$ hold time for $\overline{CAS}$ before $\overline{RAS}$ refresh cycle	t_{CHR}	15		15		15		20		ns	
$\overline{CAS}$ precharge time, fast-page cycle	t_{CP}	10		10	15	10	20	10	25	ns	(Note 13)
$\overline{CAS}$ precharge time, nonpage cycle	t_{CPN}	10		10		10		10		ns	
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	10		10		10		10		ns	(Note 14)
$\overline{CAS}$ hold time	t_{CSH}	60		70		80		100		ns	
$\overline{CAS}$ setup time for $\overline{CAS}$ before $\overline{RAS}$ refresh cycle	t_{CSR}	10		10		10		10		ns	
$\overline{CAS}$ to $\overline{WE}$ delay	t_{CWD}	40		40		45		55		ns	(Note 18)
Write command to $\overline{CAS}$ lead time	t_{CWL}	15		15		20		20		ns	
Data-in hold time	t_{DH}	15		15		20		20		ns	(Note 17)

AC Characteristics (cont)

		-60		-70		-80		-10			
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Test Conditions**
Data-in hold time referenced to $\overline{RAS}$	t_{DHR}	N/A		N/A		60		70		ns	
Data-in setup time	t_{DS}	0		0		0		0		ns	(Note 17)
Access time from $\overline{OE}$	t_{OEA}		20		20		20		25	ns	
$\overline{OE}$ data delay time	t_{OED}	15		15		20		25		ns	
$\overline{OE}$ command hold time	t_{OEH}	0		0		0		0		ns	
$\overline{OE}$ to $\overline{RAS}$ inactive setup time	t_{OES}	0		0		0		0		ns	
Output turnoff delay from $\overline{OE}$	t_{OEZ}	0	15	0	15	0	20	0	25	ns	(Note 11)
Output buffer turnoff delay	t_{OFF}	0	15	0	15	0	20	0	25	ns	(Note 11)
Fast-page cycle time	t_{PC}	40		45		50		60		ns	(Note 6)
Fast-page read-write cycle time	t_{PRWC}	85		90		105		125		ns	
Access time from $\overline{RAS}$	t_{RAC}		60		70		80		100	ns	(Notes 7, 8)
$\overline{RAS}$ to column address delay time	t_{RAD}	15	30	15	35	17	35	17	50	ns	(Note 10)
Row address hold time	t_{RAH}	10		10		12		12		ns	
Column address lead time referenced to $\overline{RAS}$ (rising edge)	t_{RAL}	30		35		45		50		ns	
$\overline{RAS}$ pulse width	t_{RAS}	60	10,000	70	10,000	80	10,000	100	10,000	ns	
$\overline{RAS}$ pulse width, fast-page cycle	t_{RASP}	60	100,000	70	100,000	80	100,000	100	100,000	ns	
Random read or write cycle time	t_{RC}	120		130		160		190		ns	(Note 6)
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	20	40	20	50	25	60	25	75	ns	(Note 12)
Read command hold time referenced to $\overline{CAS}$	t_{RCH}	0		0		0		0		ns	(Note 15)
Read command setup time	t_{RCS}	0		0		0		0		ns	
Refresh period	t_{REF}		8		8		8		8	ms	Addresses A_0 - A_8; 64 ms for -L versions
$\overline{RAS}$ precharge time	t_{RP}	50		50		70		80		ns	
$\overline{RAS}$ precharge $\overline{CAS}$ hold time	t_{RPC}	10		10		10		10		ns	
Read command hold time referenced to $\overline{RAS}$	t_{RRH}	10		10		10		10		ns	(Note 15)
$\overline{RAS}$ hold time	t_{RSH}	20		20		20		25		ns	
Read-write cycle time	t_{RWC}	165		175		215		255		ns	(Note 6)
$\overline{RAS}$ to $\overline{WE}$ delay	t_{RWD}	80		90		105		130		ns	(Note 18)

AC Characteristics (cont)

Parameter	Symbol	-60 Min	-60 Max	-70 Min	-70 Max	-80 Min	-80 Max	-10 Min	-10 Max	Unit	Test Conditions
Write command to $\overline{RAS}$ lead time	t_{RWL}	20		20		25		30		ns	
Rise and fall transition time	t_T	3	50	3	50	3	50	3	50	ns	(Note 4)
Write command hold time	t_{WCH}	15		15		15		20		ns	
Write command hold time referenced to $\overline{RAS}$	t_{WCR}	N/A		N/A		55		70		ns	
Write command setup time	t_{WCS}	0		0		0		0		ns	(Note 18)
Write command pulse width	t_{WP}	15		15		15		20		ns	(Note 16)

Notes:

(1) All voltages are referenced to GND.

(2) An initial pause of 100 μs is required after power-up, followed by any eight $\overline{RAS}$ cycles, before proper device operation is achieved.

(3) Ac measurements assume t_T = 5 ns.

(4) V_{IH} (min) and V_{IL} (max) are reference levels for measuring the timing of input signals. Transition times are measured between V_{IH} and V_{IL}.

(5) I_{CC1}, I_{CC3}, I_{CC4}, and I_{CC5} depend on output loading and cycle rates. Specified values are obtained with the output open. I_{CC3} is measured assuming that all column address inputs are held at either a high level or a low level during $\overline{RAS}$-only refresh cycles. I_{CC4} is measured assuming that all column address inputs are switched only once during each fast-page cycle.

(6) The minimum specifications are used only to indicate the cycle time at which proper operation over the full temperature range (T_A = 0 to +70°C) is assured.

(7) Load = 2 TTL (−1 mA, +4 mA) loads and 100 pF.

(8) Assumes that $t_{RCD} \leq t_{RCD}$ (max) and $t_{RAD} \leq t_{RAD}$ (max). If t_{RCD} or t_{RAD} is greater than the maximum recommended value in this table, t_{RAC} increases by the amount that t_{RCD} or t_{RAD} exceeds the value shown.

(9) Assumes that $t_{RCD} \geq t_{RCD}$ (max) and $t_{RAD} \leq t_{RAD}$ (max).

(10) If $t_{RAD} \geq t_{RAD}$ (max), then the access time is defined by t_{AA}.

(11) t_{OFF} (max) and t_{OEZ} (max) define the time at which the outputs achieve the open-circuit condition and are not referenced to V_{OH} or V_{OL}.

(12) Operation with the t_{RCD} (max) limit assures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a reference point only; if t_{RCD} is greater than t_{RCD} (max), access time is controlled exclusively by t_{CAC}.

(13) For fast-page read operation, the definition of access time is as follows:

$\overline{CAS}$ and Column Address Input Conditions	Access Time Definition
$t_{CP} \leq t_{CP}$ (max), $t_{ASC} \geq t_{CP}$	t_{ACP}
$t_{CP} \leq _{CP}$ (max), $t_{ASC} \leq t_{CP}$	t_{AA}
$t_{CP} \geq _{CP}$ (max), $t_{ASC} \leq t_{ASC}$ (max)	t_{AA}
$t_{CP} \geq _{CP}$ (max), $t_{ASC} \geq t_{ASC}$ (max)	t_{CAC}

(14) The t_{CRP} requirement should be applicable for $\overline{RAS}$/$\overline{CAS}$ cycles preceded by any cycle.

(15) Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.

(16) Parameter t_{WP} is applicable for a delayed write cycle such as a read-write/read-modify-write cycle. For early write cycles, both t_{WCS} and t_{WCH} must be met.

(17) These parameters are referenced to the falling edge of $\overline{CAS}$ for early write cycles and to the falling edge of $\overline{WE}$ for delayed write or read-modify-write cycles.

(18) t_{WCS}, t_{RWD}, t_{CWD}, and t_{AWD} are restrictive operating parameters in read-write/read-modify-write cycles only. If $t_{WCS} \geq t_{WCS}$ (min), the cycle is an early write cycle and the data I/O pins will remain open-circuit throughout the entire cycle. If $t_{CWD} \geq t_{CWD}$ (min), $t_{RWD} \geq t_{RWD}$ (min), and $t_{AWD} \geq t_{AWD}$ (min), then the cycle is a read-write cycle and the data I/O pins will contain data read from the selected cells. If neither of the above conditions is met, the condition of the data I/O pins (at access time and until $\overline{CAS}$ returns to V_{IH}) is indeterminate.

Low Power Battery Backup (-L Versions Only)

The μPD424256-L is capable of low power battery backup during times of reduced system power, when the input buffers and all nonessential internal circuits are turned off. For the input buffers to be turned off and the amount of leakage current flowing through them reduced, the μPD424256-L must be in standby and all control lines within 0.2 V of either V_{CC} or GND, as appropriate. When $\overline{RAS}$ and $\overline{CAS}$ are both within 0.2 V of V_{CC}, the internal circuits are inactive and power requirements reduced even further. Standby current can drop as low as 200 μA.

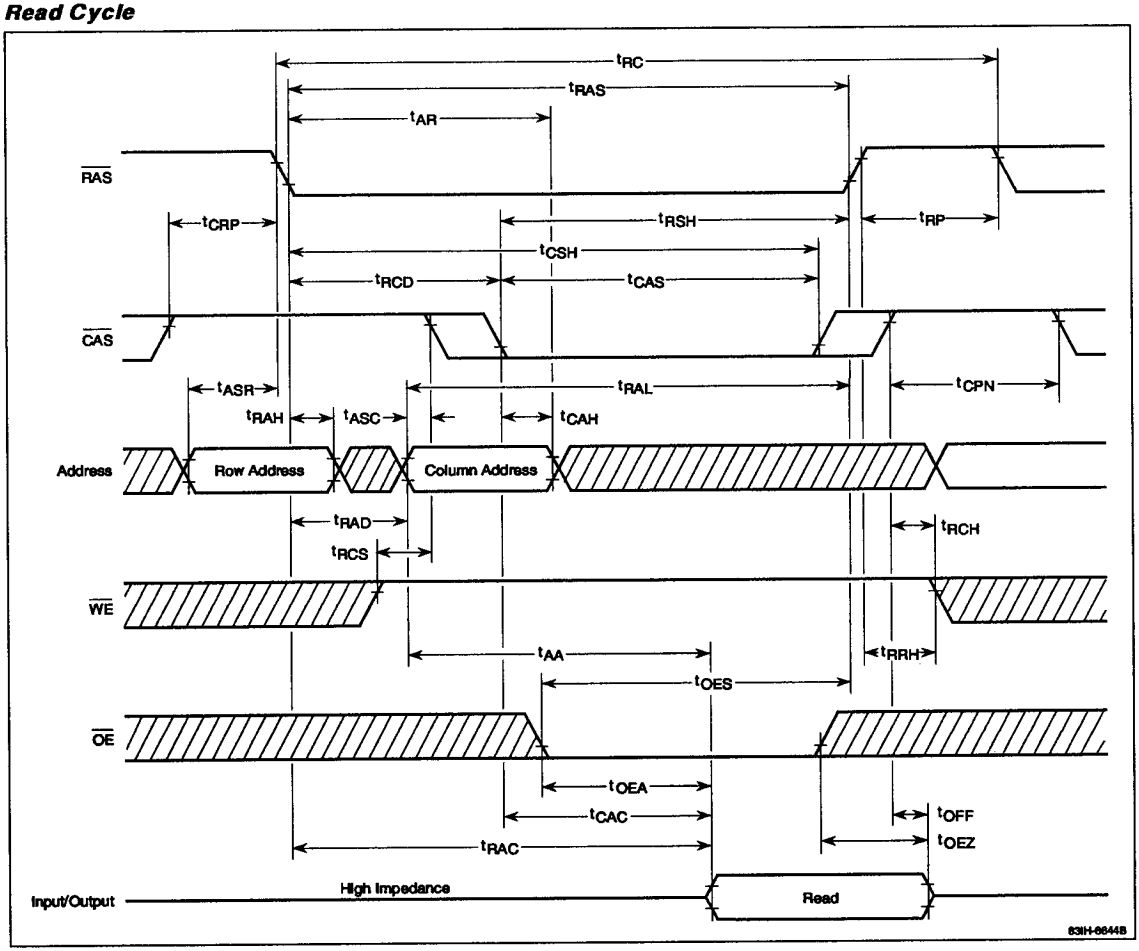
$\overline{CAS}$ before $\overline{RAS}$ refresh cycles are executed at a minimum rate to ensure that all 512 rows are refreshed only once every 64 ms. The time that $\overline{RAS}$ is low (t_{RAS}) and the μPD424256-L active needs to be as short as possible, typically less than 300 ns, to minimize power usage during refresh operation. The following table shows the conditions under which the lowest average standby current can be obtained.

Battery Backup Current

Symbol	Max	Unit	$\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle	Standby Conditions
I_{CC6}	200	μA	$t_{RAS} \leq 300$ ns	$\overline{RAS} = \overline{CAS} \geq V_{CC} - 0.2$ V; $\overline{OE} \geq V_{CC} - 0.2$ V; $\overline{WE}$ = Addresses $\geq V_{CC} - 0.2$ V or ≤ 0.2 V; I/O $\geq V_{CC} - 0.2$ V or ≤ 0.2 V or high-Z
I_{CC6}	300	μA	$t_{RAS} \geq 300$ ns and ≤ 1 μs	

Timing Waveforms

Read Cycle



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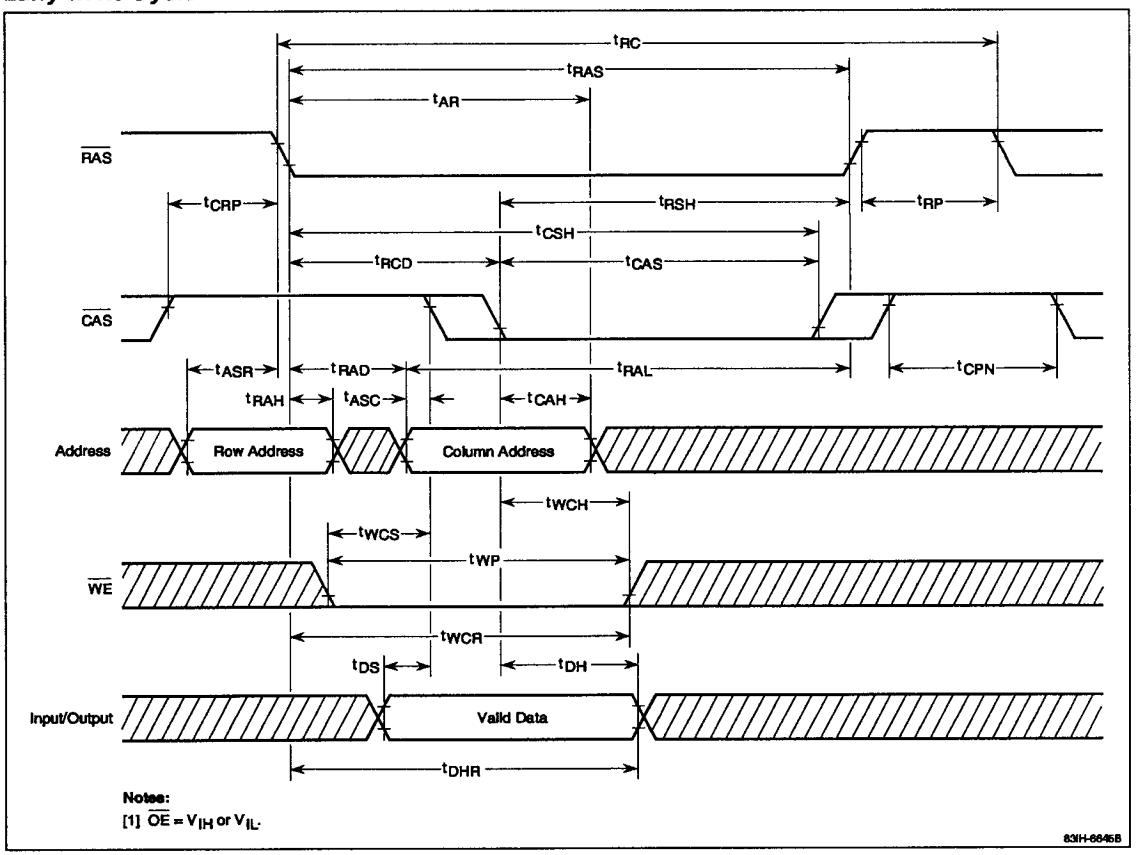
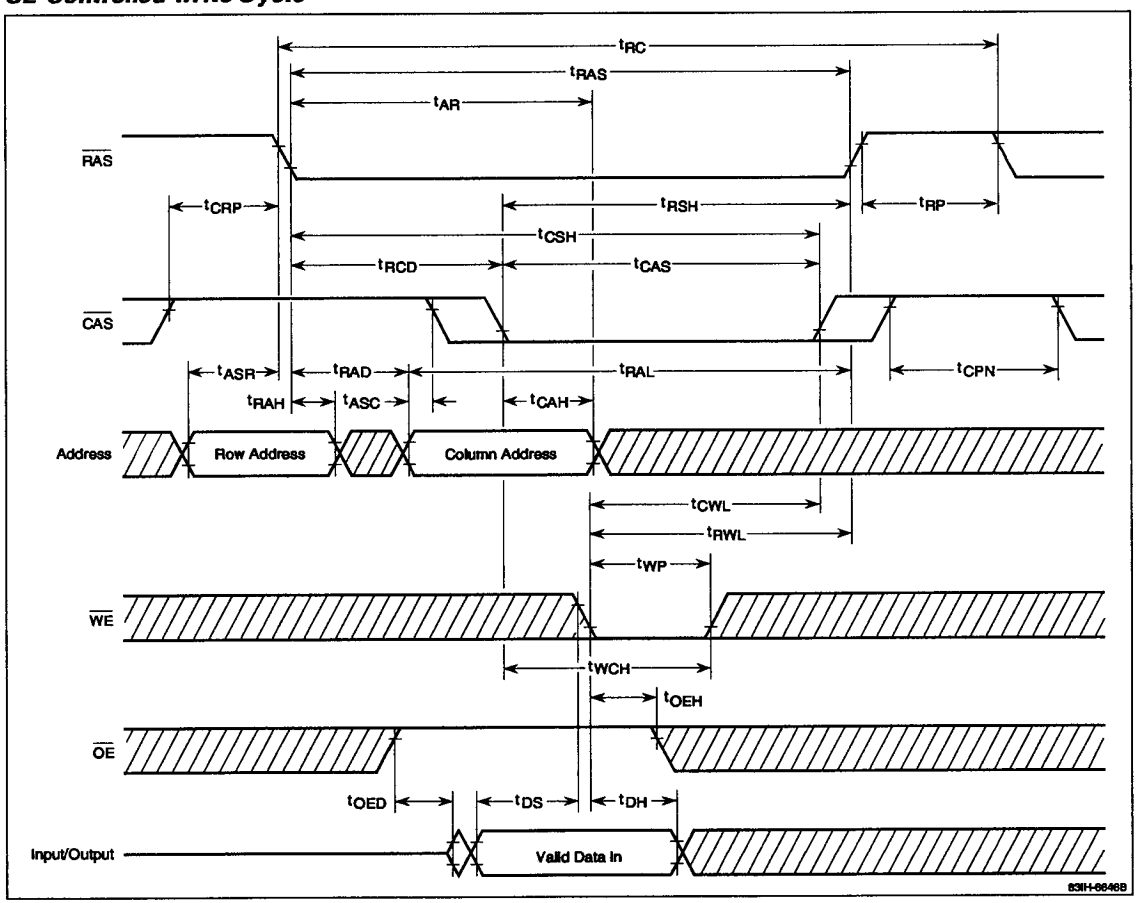
Timing Waveforms (cont)

Early Write Cycle



Timing Waveforms (cont)

$\overline{OE}$-Controlled Write Cycle



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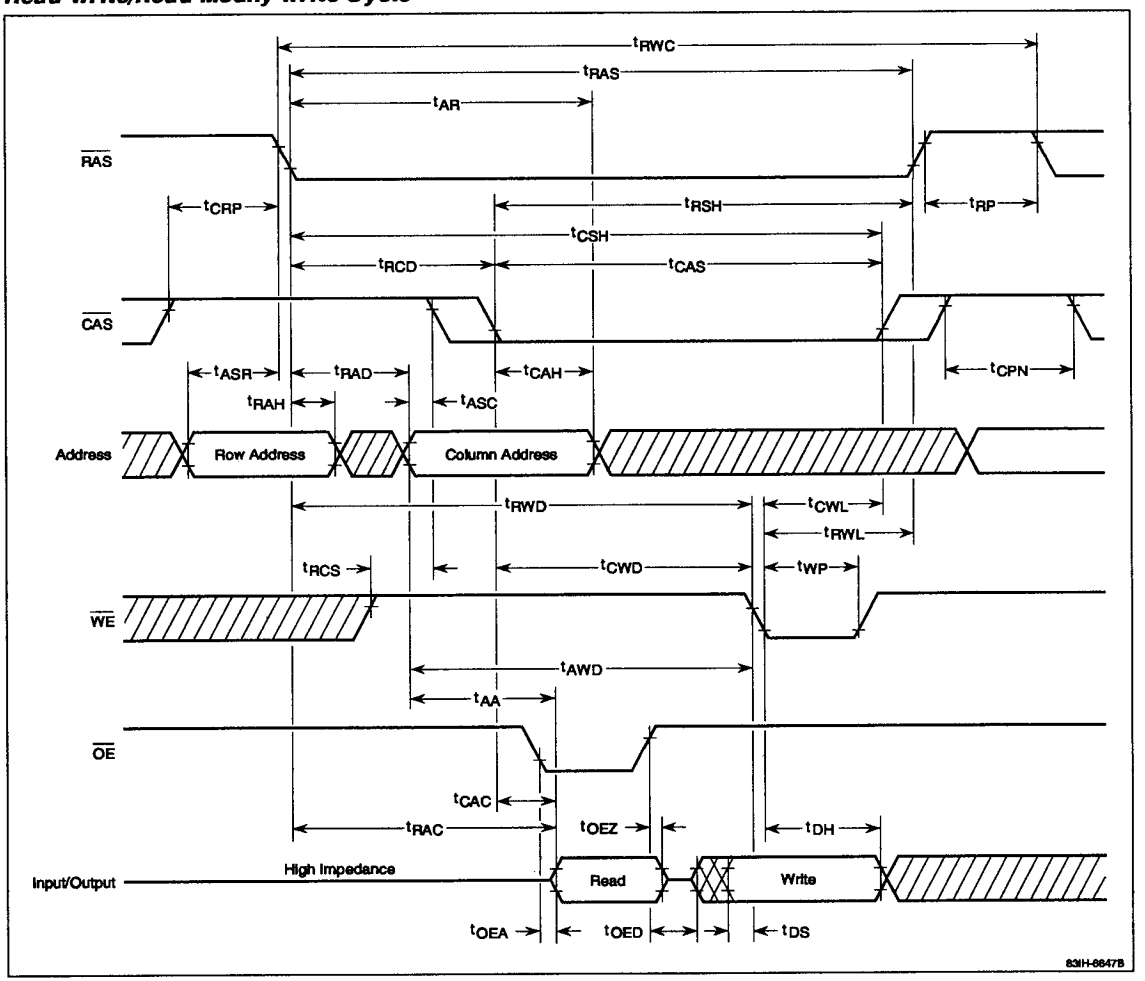
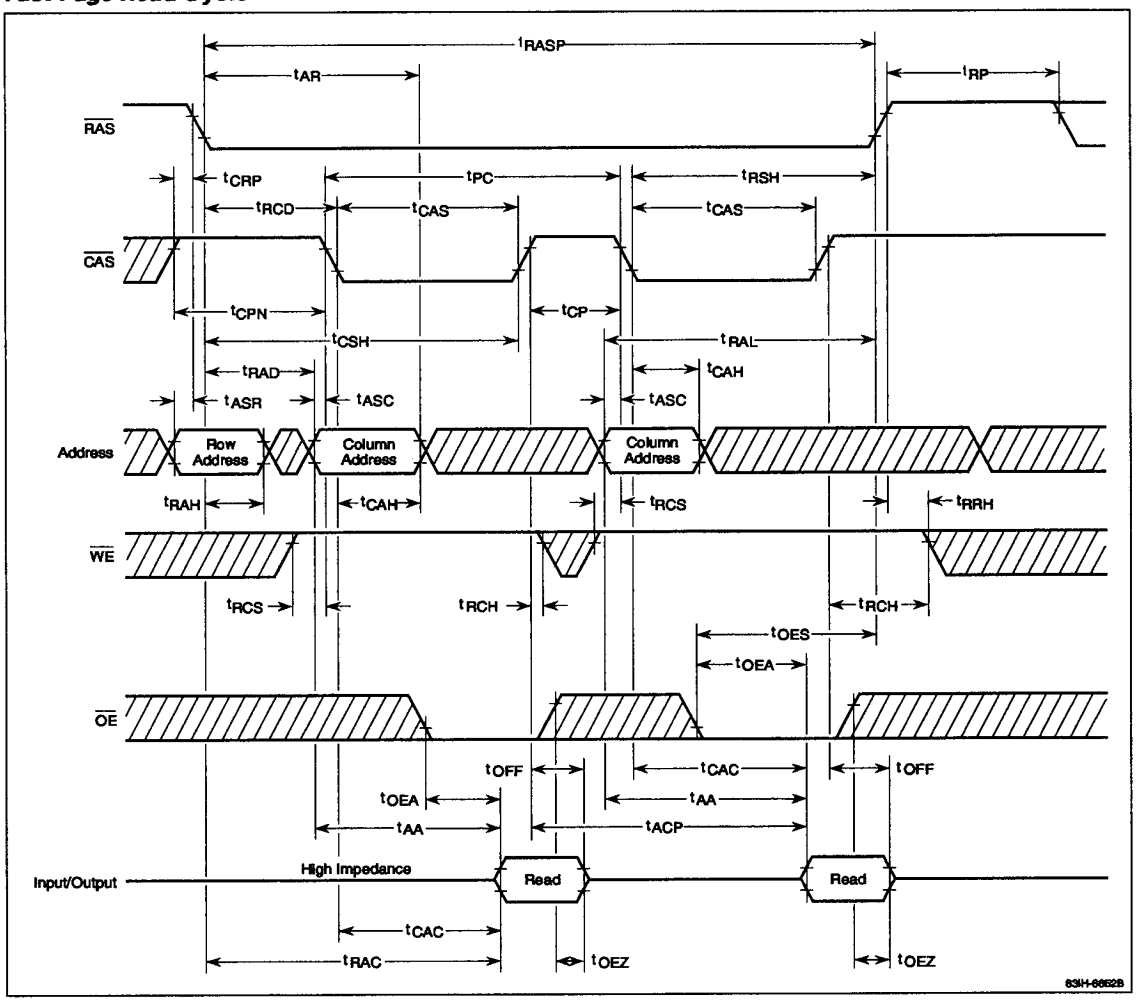
Timing Waveforms (cont)

Read-Write/Read-Modify-Write Cycle



Timing Waveforms (cont)

Fast-Page Read Cycle



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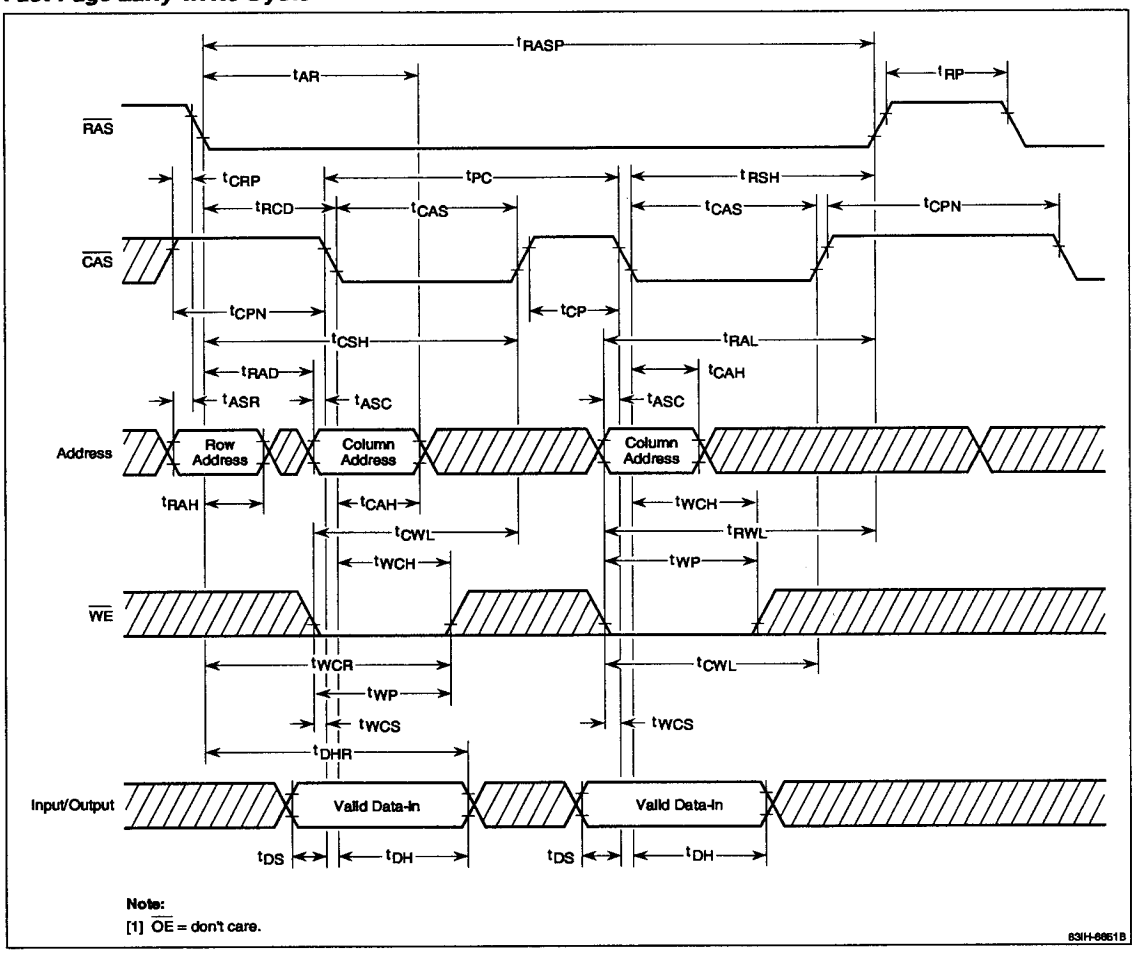
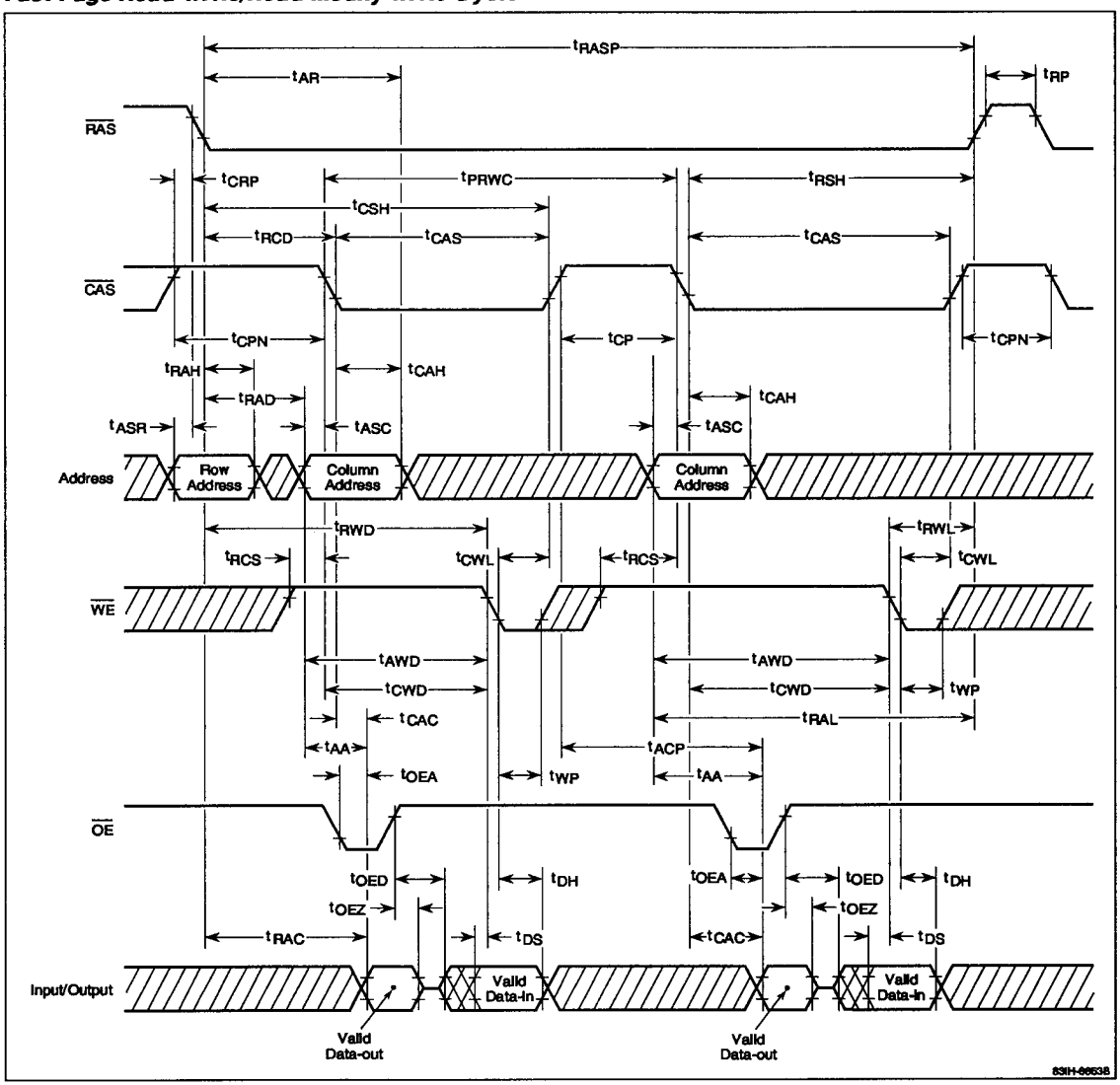
Timing Waveforms (cont)

Fast-Page Early Write Cycle



Timing Waveforms (cont)

Fast-Page Read-Write/Read-Modify-Write Cycle



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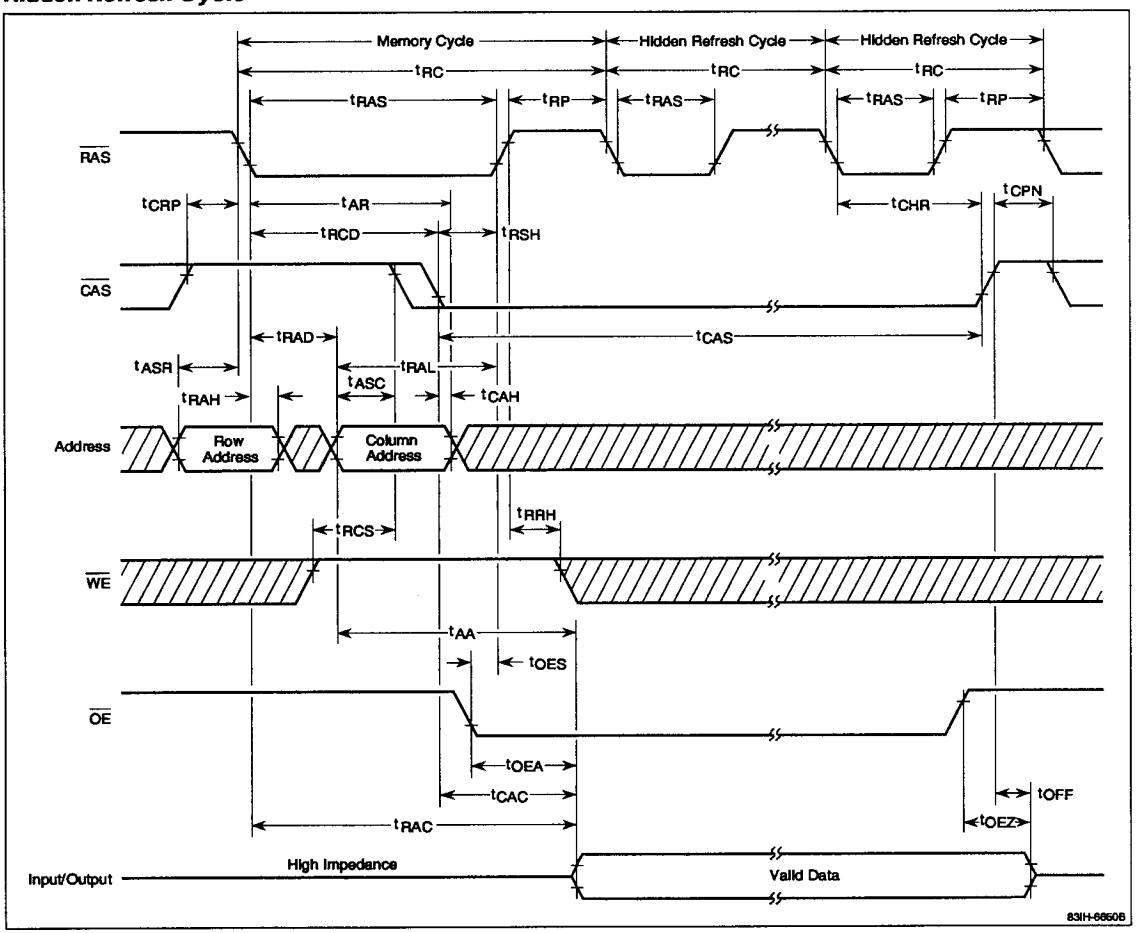
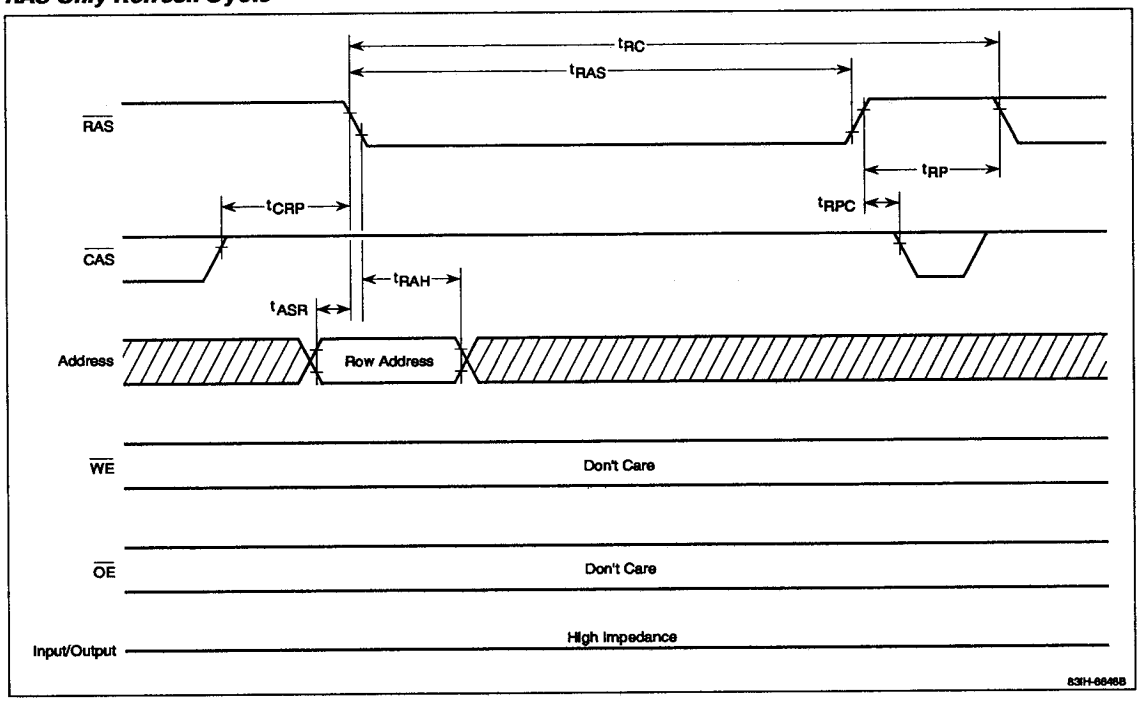
Timing Waveforms (cont)

Hidden Refresh Cycle



Timing Waveforms (cont)

$\overline{RAS}$-Only Refresh Cycle



Timing Waveforms (cont)

$\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle