

Document Title**1M x 8bit 2.7 ~ 3.6V Super low Power FCMOS Slow SRAM**Revision History

| <u>Revision No</u> | <u>History</u> | <u>Draft Date</u> | <u>Remark</u> |
|--------------------|---|-------------------|---------------|
| 00 | Initial Draft | Jan.19.2002 | Preliminary |
| 01 | DC Electrical Characteristics - ICC changed 4mA -> 3mA - ICC1 changed 20mA at 55ns / 15mA at 70ns / 2mA at 1us - ISB1 LL-Part changed 30uA -> 20uA Absolute Maximum Ratings - VCC changed -0.3 to 4.6V -> -0.3 to 4.0V AC Test Conditions - Output Load changed 5pF -> 30p Data Retention Electric Characteristic - ICCDR LL-Part changed 20uA -> 10uA | Nov.06.2002 | Final |

DESCRIPTION

The HY62KF08802B is a high speed, super low power and 8Mbit full CMOS SRAM organized as 1M words by 8bits. The HY62KF08802B uses high performance full CMOS process technology and is designed for high speed and low power circuit technology. It is particularly well-suited for the high density low power system application. This device has a data retention mode that guarantees data to remain valid at a minimum power supply voltage of 1.2V.

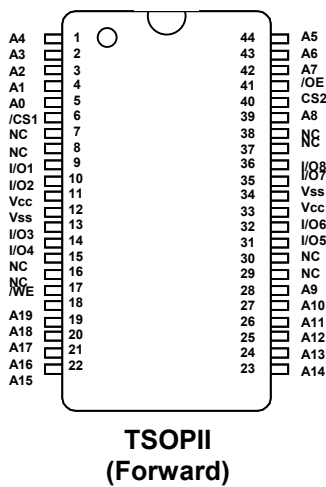
FEATURES

- Fully static operation and Tri-state output
- TTL compatible inputs and outputs
- Battery backup
 - . 1.2V(min) data retention
- Standard pin configuration
 - . 44pin 400mil TSOP-II(Forward)

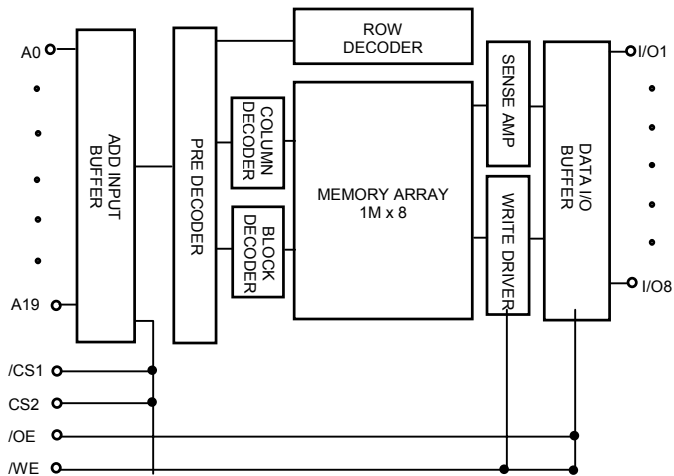
| Product No. | Voltage (V) | Speed (ns) | Operation Current/Icc(mA) | Standby Current(uA) | | Temperature (°C) |
|----------------|-------------|------------|---------------------------|---------------------|----|------------------|
| | | | | SL | LL | |
| HY62KF08802B-I | 2.7~3.6 | 55/70 | 3 | 12 | 20 | -40~85 |

Note 1. I : Industrial
 2. Current value is max.

PIN CONNECTION



BLOCK DIAGRAM



PIN DESCRIPTION

| Pin Name | Pin Function | Pin Name | Pin Function |
|-----------|---------------------|----------|------------------|
| /CS1, CS2 | Chip Select | A0~A19 | Address Inputs |
| /WE | Write Enable | Vcc | Power (2.7~3.6V) |
| /OE | Output Enable | Vss | Ground |
| I/O1~I/O8 | Data Inputs/Outputs | NC | No Connection |

ORDERING INFORMATION

| Part No. | Speed | Power | Temp' | Package |
|--------------------|-------|---------|-------|---------|
| HY62KF08802B-SD(I) | 55/70 | SL-part | I | TSOP-II |
| HY62KF08802B-DD(I) | 55/70 | LL-part | I | TSOP-II |

Note 1. I : Industrial

ABSOLUTE MAXIMUM RATINGS (1)

| Symbol | Parameter | Rating | Unit | Remark |
|------------------------------------|-----------------------------------|-------------------------------|--------|----------------|
| V _{IN} , V _{OUT} | Input/Output Voltage | -0.3 to V _{CC} +0.3V | V | |
| V _{CC} | Power Supply | -0.3 to 4.0 | V | |
| T _A | Operating Temperature | -40 to 85 | °C | HY62KF08802B-I |
| T _{STG} | Storage Temperature | -55 to 150 | °C | |
| P _D | Power Dissipation | 1.0 | W | |
| T _{SD} | Ball Soldering Temperature & Time | 260 • 10 | °C•sec | |

Note

- Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is stress rating only and the functional operation of the device under these or any other conditions above those indicated in the operation of this specification is not implied. Exposure to the absolute maximum rating conditions for extended period may affect reliability.

TRUTH TABLE

| /CS1 | CS2 | /WE | /OE | Mode | I/O Pin (/I/O1~/I/O8) | Power |
|------|-----|-----|-----|-----------------|-----------------------|---------|
| H | X | X | X | Deselected | High-Z | Standby |
| X | L | X | X | Deselected | High-Z | |
| L | H | H | H | Output Disabled | High-Z | Active |
| L | H | H | L | Read | DOUT | Active |
| L | H | L | X | Write | DIN | Active |

Note:

- H=V_{IH}, L=V_{IL}, X=don't care (V_{IL} or V_{IH})

RECOMMENDED DC OPERATING CONDITION

| Symbol | Parameter | Min. | Typ | Max. | Unit |
|--------|--------------------|-------------------|------------|---------|------|
| Vcc | Supply Voltage | 2.7 | 3.0 or 3.3 | 3.6 | V |
| Vss | Ground | 0 | 0 | 0 | V |
| VIH | Input High Voltage | 2.2 | - | Vcc+0.3 | V |
| VIL | Input Low Voltage | -0.3 ¹ | - | 0.6 | V |

Note : 1. Undershoot : VIL = -1.5V for pulse width less than 30ns
 2. Undershoot is sampled, not 100% tested.

DC ELECTRICAL CHARACTERISTICS

TA = -40°C to 85°C

| Sym | Parameter | Test Condition | Min | Typ ¹ | Max | Unit |
|------|--------------------------------|---|------|------------------|-----|------|
| ILI | Input Leakage Current | $V_{SS} \leq V_{IN} \leq V_{CC}$ | -1 | - | 1 | uA |
| ILO | Output Leakage Current | $V_{SS} \leq V_{OUT} \leq V_{CC}$, /CS1 = VIH or CS2 = VIL or /OE = VIH or /WE = VIL | -1 | - | 1 | uA |
| Icc | Operating Power Supply Current | /CS1 = VIL, CS2 = VIH VIN = VIH or VIL, I/O = 0mA | | | 3 | mA |
| ICC1 | Average Operating Current | /CS1 = VIL, CS2 = VIH VIN = VIH or VIL, Cycle Time = Min, 100% Duty, I/O = 0mA | 55ns | | 20 | mA |
| | | | 70ns | | 15 | mA |
| | | /CS1 \leq 0.2V, CS2 \geq Vcc-0.2V VIN \leq 0.2V or VIN \geq Vcc-0.2V, Cycle Time = 1us, 100% Duty, I/O = 0mA | | | 2 | mA |
| ISB | Standby Current (TTL Input) | /CS1 = VIH, CS2 = VIL VIN = VIH or VIL | | | 300 | uA |
| ISB1 | Standby Current (CMOS Input) | /CS1 \geq Vcc - 0.2V, CS2 \leq Vss + 0.2V, VIN \geq Vcc - 0.2V or VIN \leq Vss + 0.2V | SL | 0.2 | 12 | uA |
| | | | LL | 0.2 | 20 | uA |
| VOL | Output Low | IOL = 2.1mA | - | - | 0.4 | V |
| VOH | Output High | IOH = -1.0mA | 2.4 | - | - | V |

Note

1. Typical values are at Vcc = 3.0V TA = 25°C
2. Typical values are not 100% tested

CAPACITANCE

(Temp = 25°C, f= 1.0MHz)

| Symbol | Parameter | Condition | Max. | Unit |
|--------|---|------------|------|------|
| CIN | Input Capacitance (Add, /CS1,CS2, /WE, /OE) | VIN = 0V | 10 | pF |
| COU | Output Capacitance (I/O) | V/I/O = 0V | 10 | pF |

Note : These parameters are sampled and not 100% tested

AC CHARACTERISTICS

TA = -40°C to 85°C, unless otherwise specified

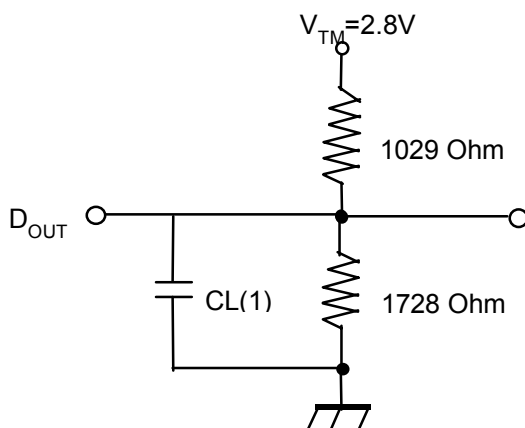
| # | Symbol | Parameter | 55ns | | 70ns | | Unit |
|-------------|--------|--------------------------------------|------|------|------|------|------|
| | | | Min. | Max. | Min. | Max. | |
| READ CYCLE | | | | | | | |
| 1 | tRC | Read Cycle Time | 55 | - | 70 | - | ns |
| 2 | tAA | Address Access Time | - | 55 | - | 70 | ns |
| 3 | tACS | Chip Select Access Time | - | 55 | - | 70 | ns |
| 4 | tOE | Output Enable to Output Valid | - | 30 | - | 35 | ns |
| 5 | tCLZ | Chip Select to Output in Low Z | 10 | - | 10 | - | ns |
| 6 | tOLZ | Output Enable to Output in Low Z | 5 | - | 5 | - | ns |
| 7 | tCHZ | Chip Deselection to Output in High Z | 0 | 20 | 0 | 25 | ns |
| 8 | tOHZ | Out Disable to Output in High Z | 0 | 20 | 0 | 25 | ns |
| 9 | tOH | Output Hold from Address Change | 10 | - | 10 | - | ns |
| WRITE CYCLE | | | | | | | |
| 10 | tWC | Write Cycle Time | 55 | - | 70 | - | ns |
| 11 | tCW | Chip Selection to End of Write | 50 | - | 60 | - | ns |
| 12 | tAW | Address Valid to End of Write | 50 | - | 60 | - | ns |
| 13 | tAS | Address Set-up Time | 0 | - | 0 | - | ns |
| 14 | tWP | Write Pulse Width | 45 | - | 50 | - | ns |
| 15 | tWR | Write Recovery Time | 0 | - | 0 | - | ns |
| 16 | tWHZ | Write to Output in High Z | 0 | 20 | 0 | 20 | ns |
| 17 | tDW | Data to Write Time Overlap | 25 | - | 30 | - | ns |
| 18 | tDH | Data Hold from Write Time | 0 | - | 0 | - | ns |
| 19 | tOW | Output Active from End of Write | 5 | - | 5 | - | ns |

AC TEST CONDITIONS

TA = -40°C to 85°C, unless otherwise specified

| Parameter | | Value |
|---|-----------------------------------|-----------------------|
| Input Pulse Level | | 0.4V to 2.2V |
| Input Rise and Fall Time | | 5ns |
| Input and Output Timing Reference Level | | 1.5V |
| Output Load | tCLZ, tOLZ, tCHZ, tOHZ, tWHZ, tOW | CL = 30pF + 1TTL Load |
| | Others | CL = 30pF + 1TTL Load |

AC TEST LOADS

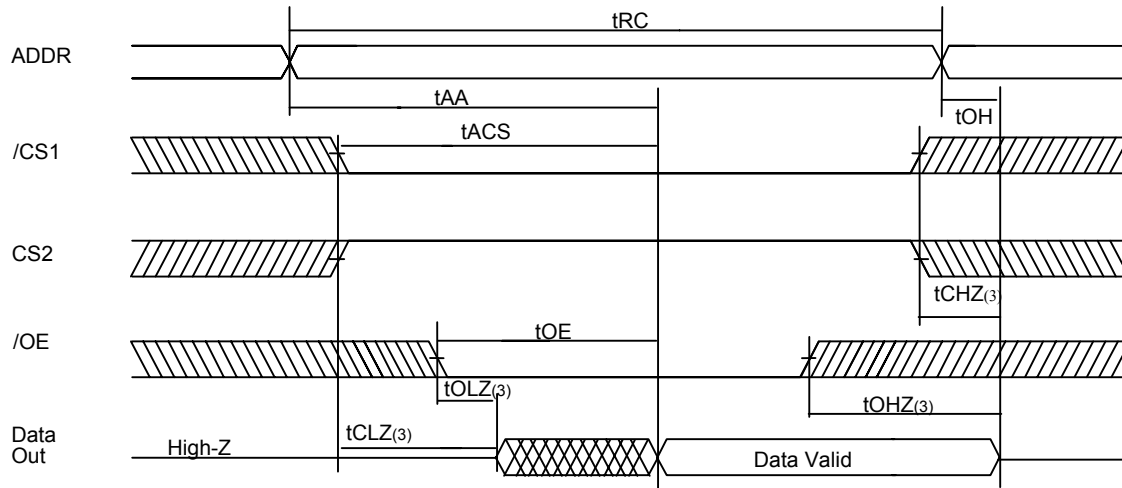


Note

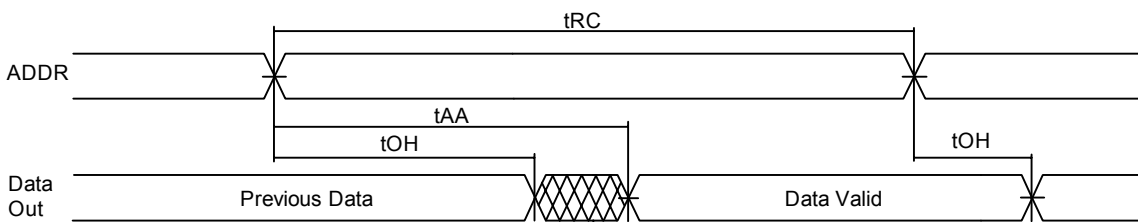
1. Including jig and scope capacitance

TIMING DIAGRAM

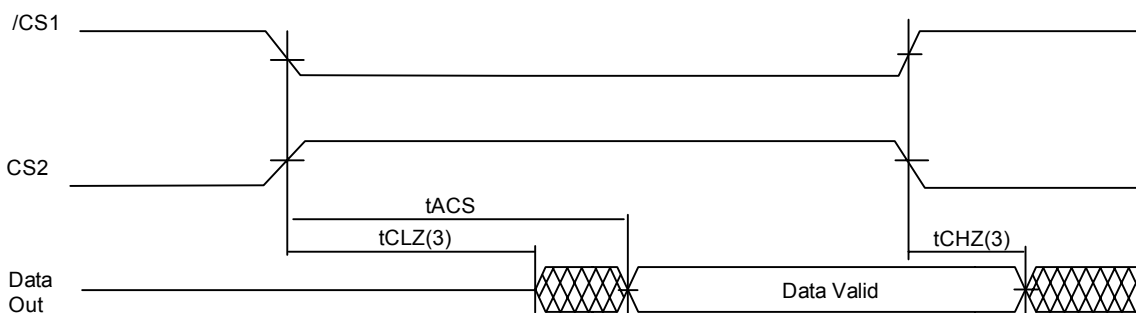
READ CYCLE 1 (Note 1,4)



READ CYCLE 2 (Note 1,2,4)



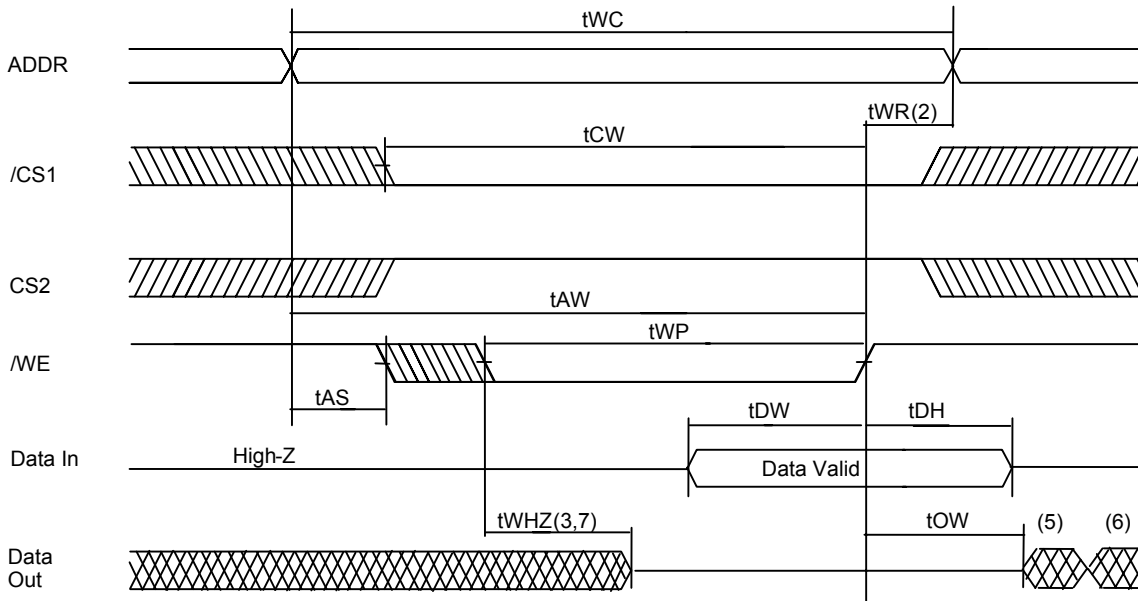
READ CYCLE 3 (Note 1,2,4)



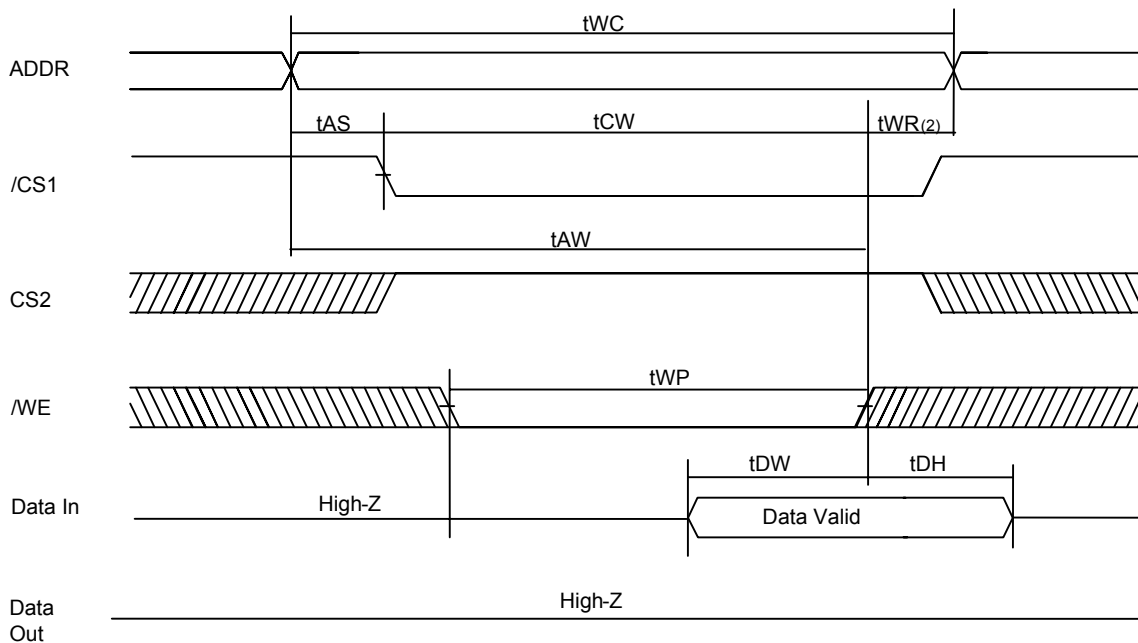
Notes:

1. Read Cycle occurs whenever a high on the /WE and /OE is low, while /CS1 and CS2 are in active status.
2. /OE = V_{IL}
3. tCHZ and tOHZ are defined as the time at which the outputs achieve the open circuit conditions and are not referenced to output voltage levels.
4. /CS1 in high for the standby, low for active
CS2 in low for the standby, high for active.

WRITE CYCLE 1 (1,4,8) (/WE Controlled)



WRITE CYCLE 2 (Note 1,4,8) (/CS1, CS2 Controlled)



Notes:

1. A write occurs during the overlap of a low /WE, a low /CS1, a high CS2.
2. t_{WR} is measured from the earlier of /CS1 or /WE going high or CS2 going low to the end of write cycle.
3. During this period, I/O pins are in the output state so that the input signals of opposite phase to the output must not be applied.
4. If the /CS1, CS2 high transition occur simultaneously with the /WE low transition or after the /WE transition, outputs remain in a high impedance state.
5. Q(data out) is the same phase with the write data of this write cycle.
6. Q(data out) is the read data of the next address.
7. /CS1 in high for the standby, low for active. CS2 in low for the standby, high for active.

DATA RETENTION ELECTRIC CHARACTERISTIC

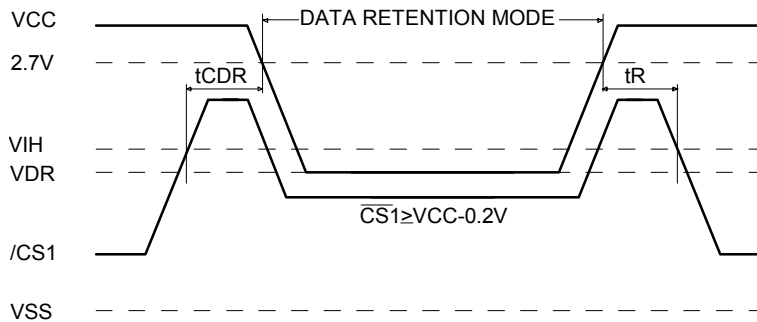
TA = -40°C to 85°C

| Symbol | Parameter | Test Condition | Min | Typ ¹ | Max | Unit | |
|--------|--------------------------------------|--|-----|------------------|-----|------|----|
| VDR | Vcc for Data Retention | $V_{CS} \geq V_{CC} - 0.2V$, $V_{IN} \geq V_{CC} - 0.2V$ or $V_{IN} \leq V_{SS} + 0.2V$ | 1.2 | - | 3.6 | V | |
| Iccdr | Data Retention Current | $V_{CC}=1.5V$, $V_{CS} \geq V_{CC} - 0.2V$ or $V_{IN} \geq V_{CC} - 0.2V$ or $V_{IN} \leq V_{SS} + 0.2V$ | SL | - | 0.1 | 6 | uA |
| | | | LL | - | 0.1 | 10 | uA |
| tCDR | Chip Deselect to Data Retention Time | See Data Retention Timing Diagram | 0 | - | - | ns | |
| tR | Operating Recovery Time | | tRC | - | - | ns | |

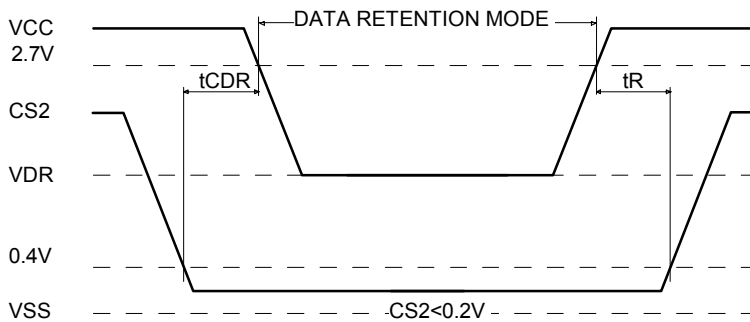
Notes:

1. Typical values are under the condition of TA = 25°C.
2. Typical value are sampled and not 100% tested

DATA RETENTION TIMING DIAGRAM 1

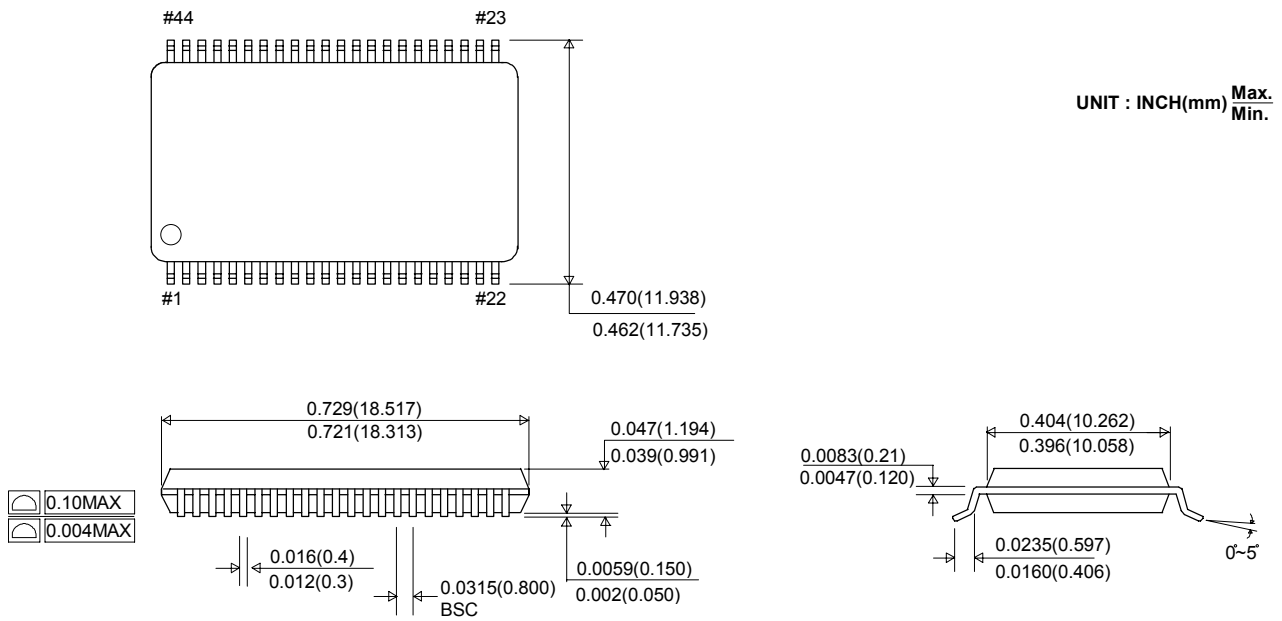


DATA RETENTION TIMING DIAGRAM 2



PACKAGE INFORMATION

44pin 400mil Thin Small Outline Package Forward (D)



MARKING INFORMATION

| Package | Marking Example | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|-------------------------------------|--|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|--|--|--|--|--|--|--|--|--|--|
| <p>TSOP-II (Forward)</p> | <table border="1" style="margin: auto;"> <tr> <td>h</td><td>y</td><td>n</td><td>i</td><td>x</td><td></td><td></td><td></td><td></td><td></td><td>y</td><td>y</td><td>w</td><td>w</td><td>p</td> </tr> <tr> <td>H</td><td>Y</td><td>6</td><td>2</td><td>K</td><td>F</td><td>8</td><td>8</td><td>0</td><td>2</td><td>B</td><td>c</td><td>s</td><td>s</td><td>t</td> </tr> <tr> <td>K</td><td>O</td><td>R</td><td>E</td><td>A</td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td> </tr> </table> | h | y | n | i | x | | | | | | y | y | w | w | p | H | Y | 6 | 2 | K | F | 8 | 8 | 0 | 2 | B | c | s | s | t | K | O | R | E | A | | | | | | | | | | |
| h | y | n | i | x | | | | | | y | y | w | w | p | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| H | Y | 6 | 2 | K | F | 8 | 8 | 0 | 2 | B | c | s | s | t | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| K | O | R | E | A | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

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| <ul style="list-style-type: none"> • hynix • yy • ww • p • HY62KF8802B • c • ss • t • KOREA | <ul style="list-style-type: none"> : hynix Logo : Year (ex : 02 = year 2002, 03 = year 2002) : Work Week (ex : 12 = ww12) : Process Code : Part Name : Power Consumption <ul style="list-style-type: none"> - D : Low Low Power - S : Super Low Power : Speed <ul style="list-style-type: none"> - 55 : 55ns - 70 : 70ns : Temperature <ul style="list-style-type: none"> - I : Industrial (-40 ~ 85 °C) : Origin Country |
| <p>Note</p> <ul style="list-style-type: none"> - Capital Letter : Fixed Item - Small Letter : Non-fixed Item (Except hynix) | |