APL6535

Two-Channel Supervisory IC

Features

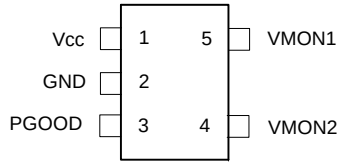
- 2.6V to 5.5V Input Voltage Range
- Low Quiescent Current : less than 50µA
- High Accuracy Detection Threshold : ±1.6%
- Adjustable Undervoltage Lockout for Each Supply
- Active high PGOOD Output
- Guaranteed PGOOD Valid to Falling V_{CC} < 1V
- VMON Glitch Immunity : 30µs
- Lead Free Available (RoHS Compliant)

Applications

- Graphics Cards
- Portable Battery-Powered Equipment
- µP Voltage Monitoring
- Set-Top Boxes
- Notebook Computer
- Multiple Supply System

Pinouts

SOT-23-5 Top View



APL6535

General Description

The APL6535 is a two channel supervisory IC designed to monitor voltage supplies in mP and digital system. This IC can supervise any positive voltage using an external resistor divider to translate to a lower voltage for comparison to the internal 0.633V reference. Once any VMON input falls below 0.633V the PGOOD output is pulled low, the hysteresis of the internal reference is 15mV. The PGOOD pin has an internal 20kW pull-up to V_{CC} making an external pull-up resistor unnecessary. Each rail's VMON point is independently adjustable with a resistor divider. The PGOOD output is guaranteed to be valid with IC bias lower than 1V. This IC is designed to reject fast line transient glitches 30ms on VMON input. The PGOOD output is an open-drain to allow ORing of multiple signals. If less than four voltages are being monitored, connect the unused VMON pins to V_{CC}. The ENABLE input pin provides for a reset of the PGOOD output when it is pulled down below 0.5V. With an internal 10mA pull-up to VCC, it can be signaled with common logic or pulled to ground with a push button switch. APL6535 come in a miniature SOT-23-5 package.

ANPEC reserves the right to make changes to improve reliability or manufacturability without notice, and advise customers to obtain the latest version of relevant information to verify before placing orders.

Ordering and Marking Information

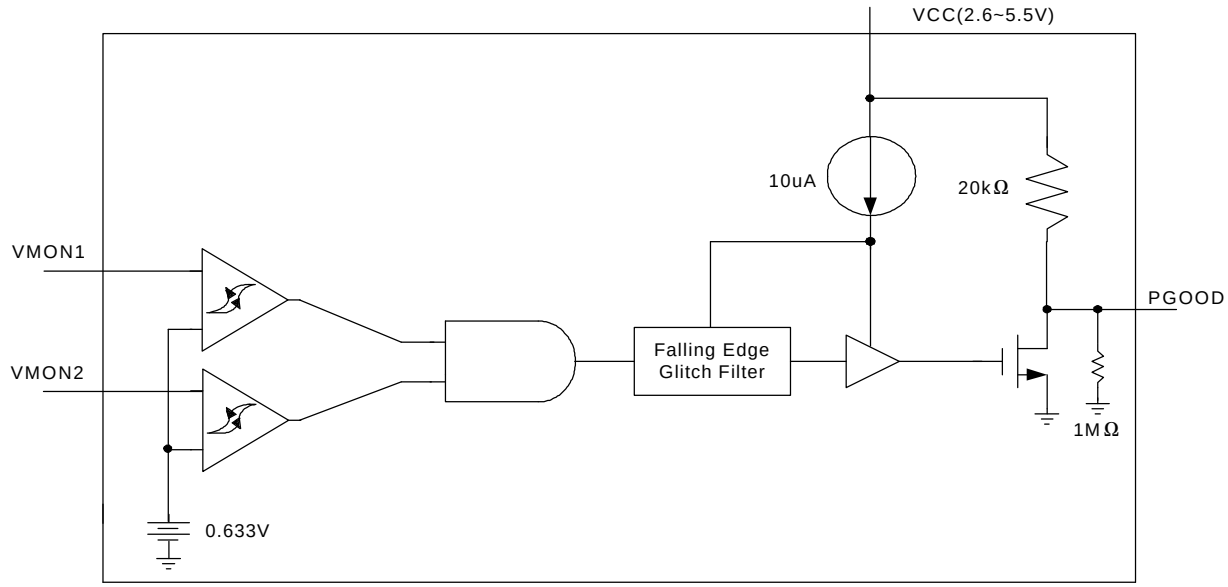
APL6535 □□-□□□ Lead Free Code Handling Code Temp. Range Package Code	Package Code B : SOT-23-5 Temp. Range I : -40 to 85 ℃ Handling Code TU : Tube TR : Tape & Reel Lead Free Code L : Lead Free Device Blank : Original Device
APL6535 : 535X	X - Date Code

Note: ANPEC lead-free products contain molding compounds/die attach materials and 100% matte in plate termination finish; which are fully compliant with RoHS and compatible with both SnPb and lead-free soldiering operations. ANPEC lead-free products meet or exceed the lead-free requirements of IPC/JEDEC J STD-020C for MSL classification at lead-free peak reflow temperature.

Pin Function Description

PIN		I/O	Description
No.	Name		
1	V_{CC}		Supply Voltage
3	PGOOD	O	PGOOD is the AND function of all the VMON inputs being satisfied. This is an open drain output and can be pulled high to the appropriate level with an external resistor. Additionally a 20kO pull up to V_{CC} is provided internally.
2	GND		Ground Connection
4, 5	VMON1 VMON2	I	These inputs provide for a programmable monitored voltage threshold referenced to an internal 0.633V reference. These inputs have a 30µs glitch filter to prevent transient upsets from being recognized by PGOOD.

Block Diagram



Absolute Maximum Ratings

Symbol	Parameter	Rating	Unit
V_{CC}	Input Voltage	6.5	V
VMON1, 2	All Input Pins	-0.3V to V_{CC}+0.3V	V
PGOOD	Output Pin	-0.3V to V_{CC}+0.3V	V
T_J	Maximum Junction Temperature	150	°C
T_{STG}	Storage Temperature	-65 to +150	°C
T_S	Soldering Temperature (10 seconds)	260	°C
ESD	Electrostatic Discharge	-3000 to 3000*[1]	V

Note:

1.Human body model: C=100pF, R=1500, 3 positives pulse plus 3 negative pulses.

Electrical Characteristics

Unless Otherwise noted these specifications apply over full temperature, V_{CC} = 3.3V, T_J=- 40 °C to 85°C
Typical values refer to T_J=25°C

Symbol	Parameter	Test condition	APL6535			Unit
			Min.	Typ.	Max.	
BIAS						
I_{CC}	Supply Current (EN enable)	VMON > V_{MON_L2H}		40	400	µA
		VMON < V_{MON_H2L}		230	2000	µA
I_{CC}	Supply Current (EN disable)	VMON > V_{MON_L2H}		50	500	µA
		VMON < V_{MON_H2L}		50	500	µA
V_{CC_L2H}	V_{CC} Power On	V_{CC} low to high		2.6		V
V_{CC_POR}	V_{CC} Power On Reset	V_{CC} high to low		2.4		V
PGOOD						
PGpd	Pull-Down Current	V_{PGOOD}=0.5V		10		mA
PGpu	Pull-Up Resistance			20		KΩ
V_{PGI}	Output Low	V_{CC} = 1V		0	100	mV
TPG del VMON	Delay From VMON Rising	Last valid input =Vth to PG release		3		µs
TPG del ENR	Delay From EN Rising	EN high to PG release		2		µs
TPG del ENF	Delay From EN Falling	EN low to PG pulling low		10		ns
VMON Input						
V_{MON_H2L}	Falling Threshold Voltage	T_J=25°C	0.623	0.633	0.643	V
V_{MON_TC}	Falling Threshold Temperature Coeff.	T_J=-40°C to 85°C		100		µV/°C
V_{VMON_HYS}	Hysteresis Voltage			15		mV
V_{VMON_RNG}	Range			10		mV
T_{FIL}	Glitch Filter Duration	VMON glitch to PGOOD low filter		30		µs

Electrical Characteristics

Unless Otherwise noted these specifications apply over full temperature, V_{CC} = 5V, T_J =- 40 °C to 85°C
Typical values refer to T_J=25°C

Symbol	Parameter	Test condition	APL6535			Unit
			Min.	Typ.	Max.	
BIAS						
I_{CC}	Supply Current (EN Enable)	VMON > $VMON_{\_L2H}$		50	500	µA
		VMON < $VMON_{\_H2L}$		230	2000	µA
I_{CC}	Supply Current (EN Disable)	VMON > $VMON_{\_L2H}$		60	600	µA
		VMON < $VMON_{\_H2L}$		60	600	µA
V_{CC_L2H}	V_{CC} Power On	V_{CC} low to high		2.6		V
V_{CC_POR}	V_{CC} Power On Reset	V_{CC} high to low		2.4		V
PGOOD						
PGpd	Pull-Down Current	V_{PGOOD}=0.5V		10		mA
PGpu	Pull-Up Resistance			20		KΩ
V_{PGI}	Output Low	V_{CC} = 1V		0	100	mV
TPG del VMON	Delay From VMON Rising	Last valid input = Vth to PG release		5		µs
TPG del ENR	Delay From EN Rising	EN high to PG release		2		µs
TPG del ENF	Delay From EN Falling	EN low to PG pulling low		10		ns
VMON Input						
$VMON_{\_H2L}$	Falling Threshold Voltage	T_J=25°C	0.623	0.633	0.643	V
$VMON_{\_TC}$	Falling Threshold Temperature Coeff.	T_J=-40°C to 85°C		100		µV/°C
$VVMON_{\_HYS}$	Hysteresis Voltage			15		mV
$VVMON_{\_RNG}$	Range			10		mV
T_{FIL}	Glitch Filter Duration	VMON glitch to PGOOD low filter		30		µs

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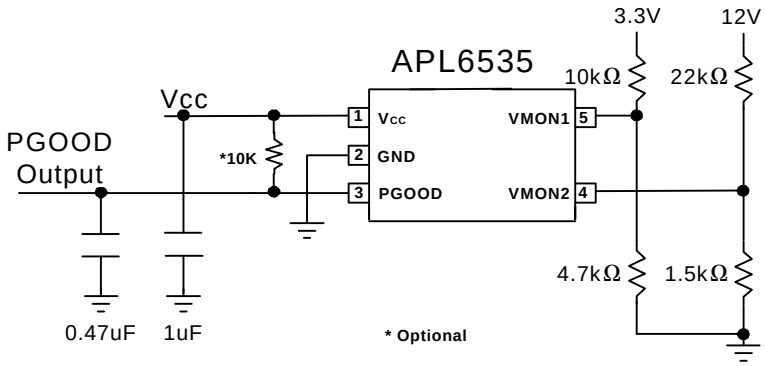
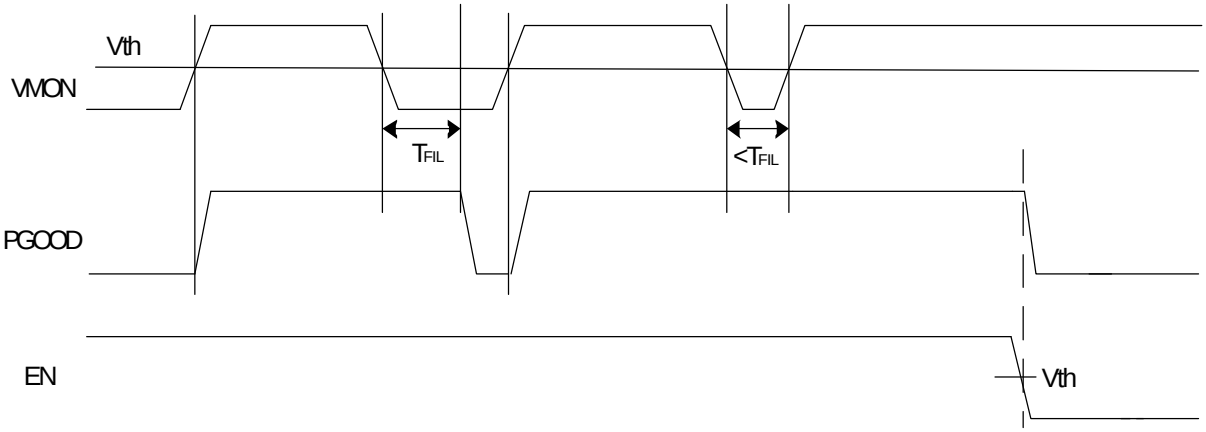
Application Circuit

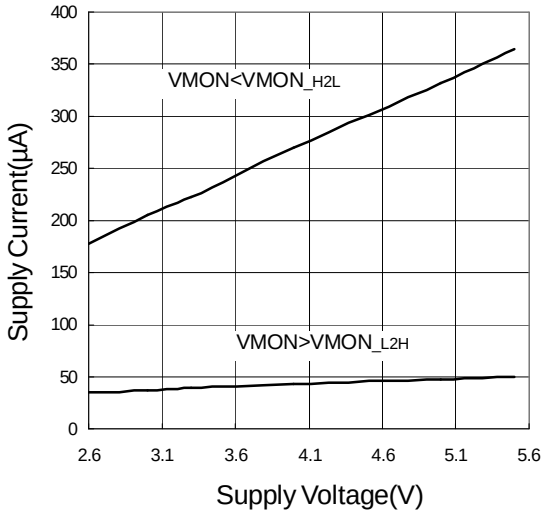


Timing Diagram

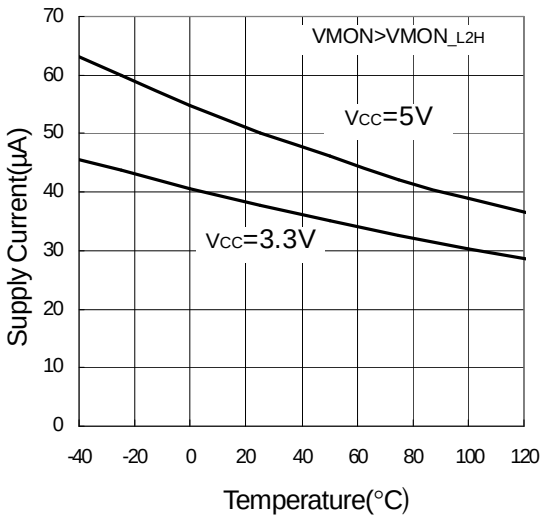


Typical Characteristics

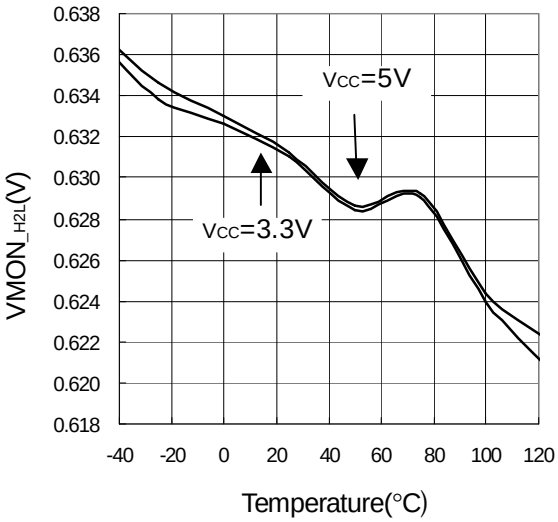
Supply Current vs. Supply Voltage



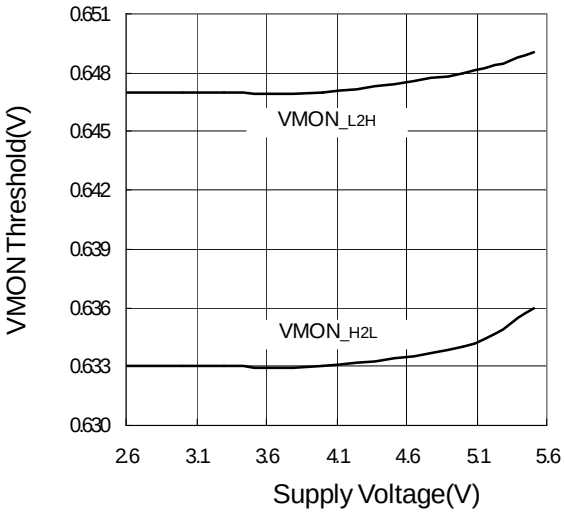
Supply Current vs. Temperature



VMON_H2L vs. Temperature

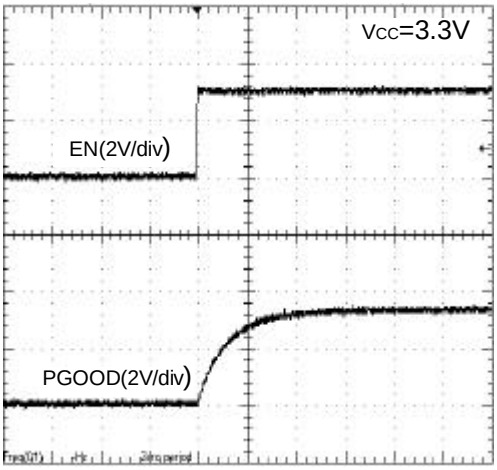


VMON Threshold vs. Supply Voltage



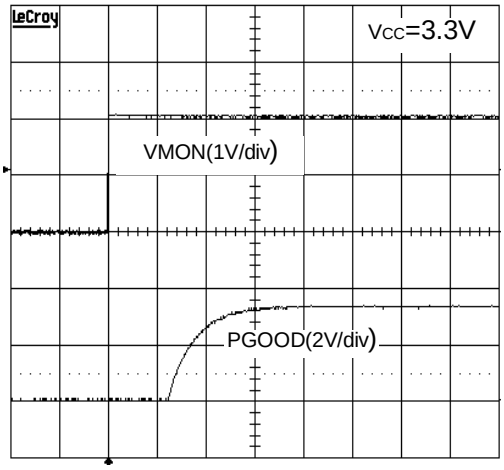
Typical Characteristics (Cont.)

EN High to PGOOD



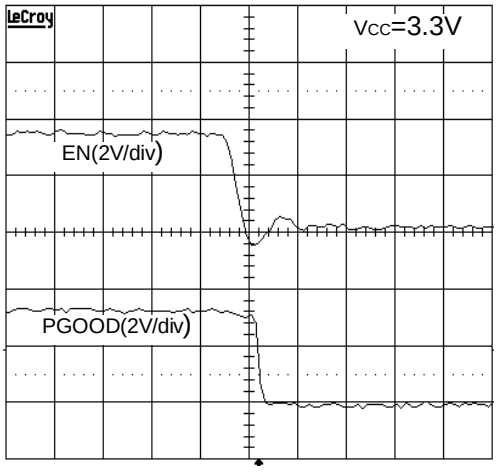
Time(1us/div)

VMON High to PGOOD



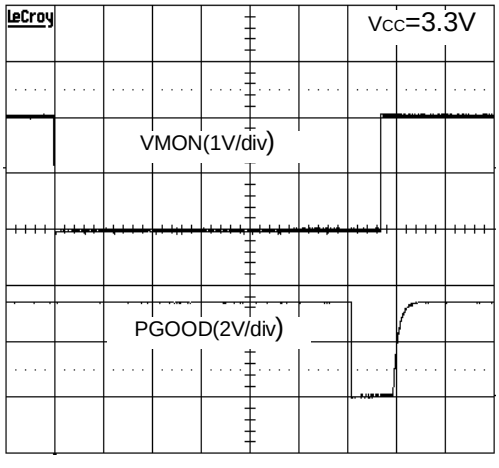
Time(4us/div)

EN Low to PGOOD



Time(10ns/div)

VMON Low to PGOOD



Time(20µs/div)

Application Information

PGOOD

The APL6535 is a four channel supervisory IC designed to monitor multiple voltages greater than 0.7V. This IC is suitable for both microprocessors or industrial system applications. Once biased to 2.6V and enabled the IC continuously monitors from one to four voltages independently through external resistor dividers comparing each VMON pin voltage to an internal 0.633V reference. The PGOOD output is an open-drain to allow ORing of the signals and interfacing to a wide range of logic levels. If less than four voltages are being monitored, connect the unused VMON pins to V_{CC}. The PGOOD pin has an internal 20kW pull-up to V_{CC} making an external pull-up resistor unnecessary.

Falling Edge Glitch Filter

Once any VMON input falls below 0.633V the PGOOD output is pulled low, the VMON inputs are designed to reject fast transients (30us).

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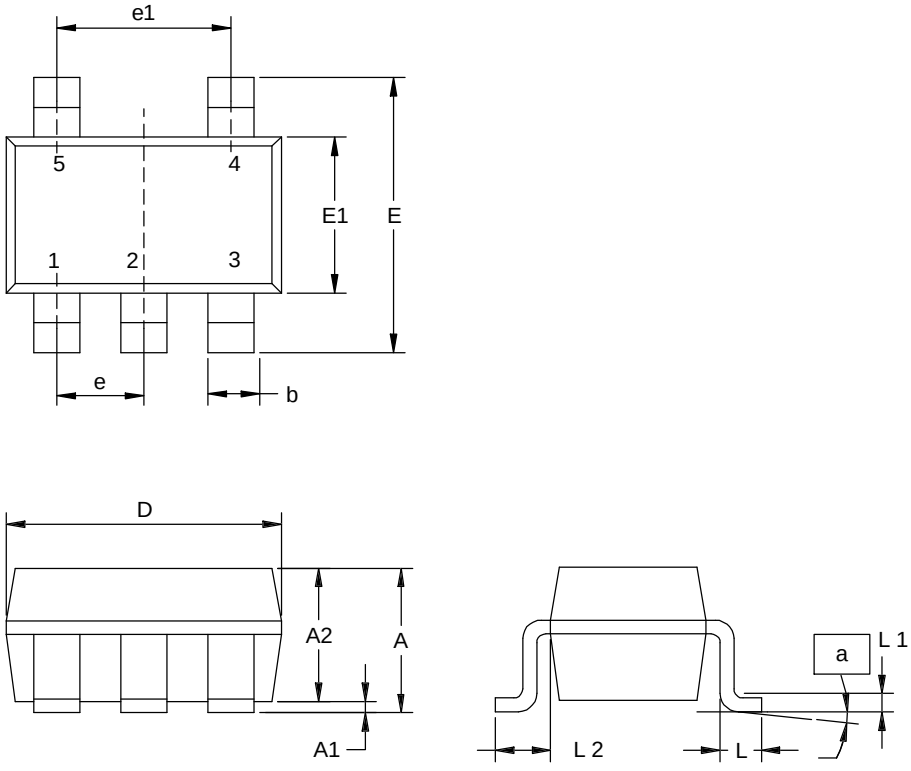
Package Information

SOT-23-5

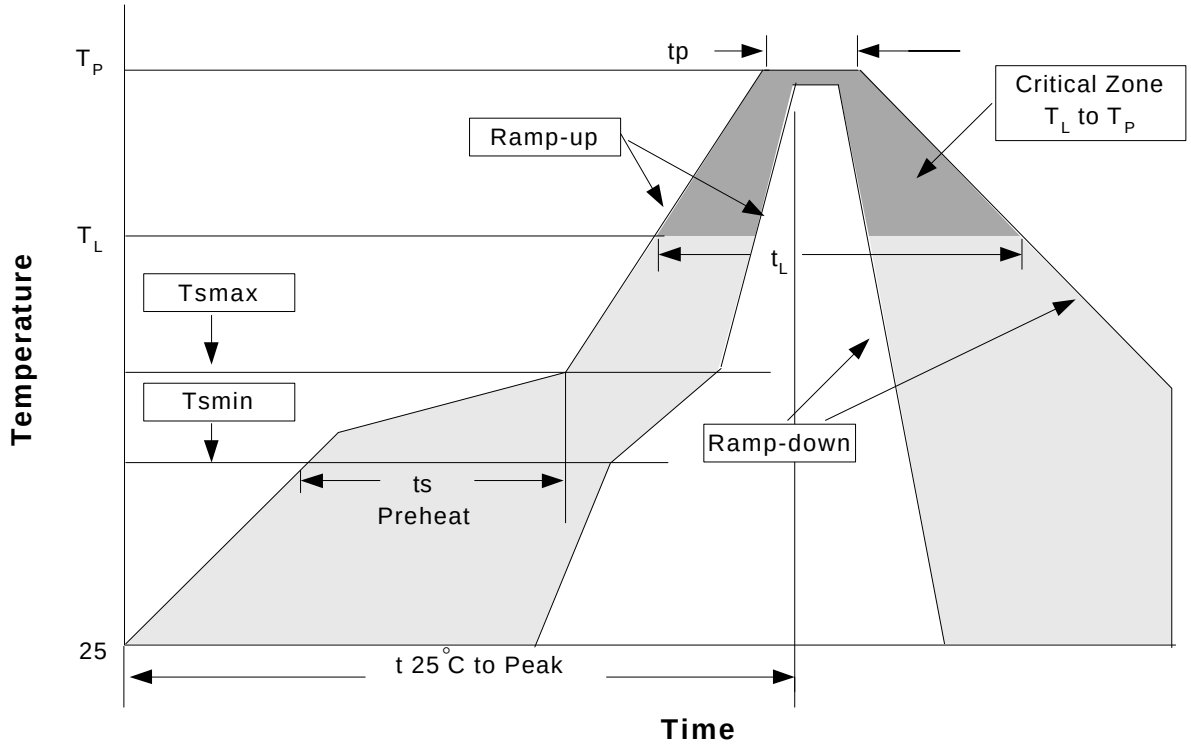


Dim	Millimeters		Inches	
	Min.	Max.	Min.	Max.
A	0.95	1.45	0.037	0.057
A1	0.05	0.15	0.002	0.006
A2	0.90	1.30	0.035	0.051
b	0.30	0.50	0.011	0.019
D	2.8	3.00	0.110	0.118
E	2.6	3.00	0.102	0.118
E1	1.5	1.70	0.059	0.067
e	0.95BSC		0.037BSC	
e1	1.90BSC		0.074BSC	
L	0.35	0.55	0.014	0.022
L1	0.20 BSC		0.008 BSC	
L2	0.5	0.7	0.020	0.028
N	5		5	
α	0°	10°	0°	10°

Physical Specifications

Terminal Material	Solder-Plated Copper (Solder Material : 90/10 or 63/37 SnPb), 100%Sn
Lead Solderability	Meets EIA Specification RSI86-91, ANSI/J-STD-002 Category 3.

Reflow Condition (IR/Convection or VPR Reflow)



Classification Reflow Profiles

Profile Feature	Sn-Pb Eutectic Assembly	Pb-Free Assembly
Average ramp-up rate (T_L to T_P)	3°C/second max.	3°C/second max.
Preheat - Temperature Min (Tsmin) - Temperature Max (Tsmax) - Time (min to max) (ts)	100°C 150°C 60-120 seconds	150°C 200°C 60-180 seconds
Time maintained above: - Temperature (T_L) - Time (t_L)	183°C 60-150 seconds	217°C 60-150 seconds
Peak/Classificatioon Temperature (Tp)	See table 1	See table 2
Time within 5°C of actual Peak Temperature (tp)	10-30 seconds	20-40 seconds
Ramp-down Rate	6°C/second max.	6°C/second max.
Time 25°C to Peak Temperature	6 minutes max.	8 minutes max.

Notes: All temperatures refer to topside of the package .Measured on the body surface.

(mm)

Classification Reflow Profiles(Cont.)

Table 1. SnPb Entectic Process – Package Peak Reflow Temperatures

Package Thickness	Volume mm^3 <350	Volume mm^3 ³350
<2.5 mm	240 +0/-5°C	225 +0/-5°C
≥2.5 mm	225 +0/-5°C	225 +0/-5°C

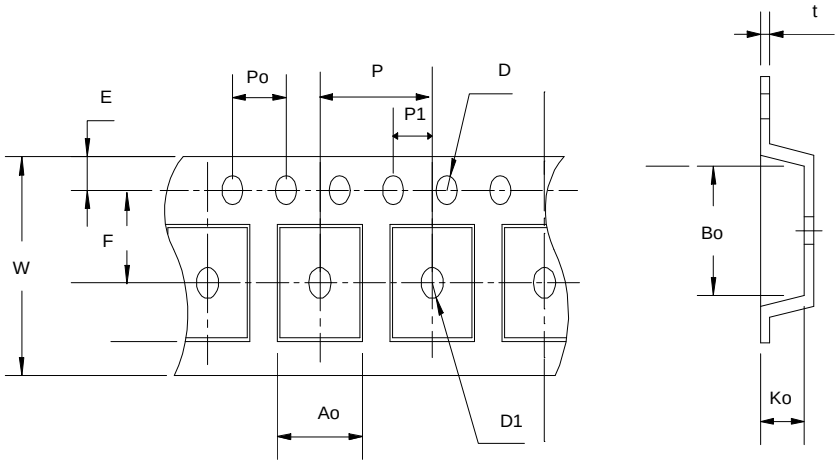
Table 2. Pb-free Process – Package Classification Reflow Temperatures

Package Thickness	Volume mm^3 <350	Volume mm^3 350-2000	Volume mm^3 >2000
<1.6 mm	260 +0°C*	260 +0°C*	260 +0°C*
1.6 mm – 2.5 mm	260 +0°C*	250 +0°C*	245 +0°C*
≥2.5 mm	250 +0°C*	245 +0°C*	245 +0°C*
*Tolerance: The device manufacturer/supplier **shall** assure process compatibility up to and including the stated classification temperature (this means Peak reflow temperature +0°C. For example 260°C+0°C) at the rated MSL level.			

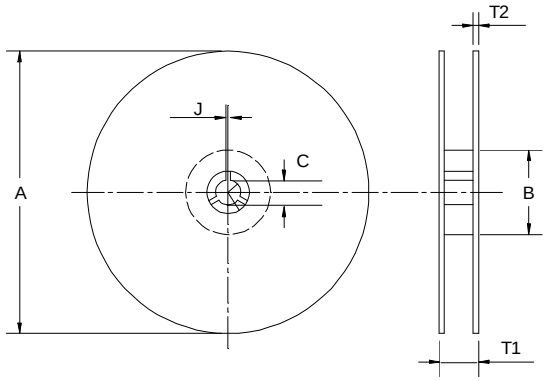
Reliability Test Program

Test item	Method	Description
SOLDERABILITY	MIL-STD-883D-2003	245°C, 5 SEC
HOLT	MIL-STD-883D-1005.7	1000 Hrs Bias @125°C
PCT	JESD-22-B,A102	168 Hrs, 100%RH, 121°C
TST	MIL-STD-883D-1011.9	-65°C~150°C, 200 Cycles
ESD	MIL-STD-883D-3015.7	VHBM > 2KV, VMM > 200V
Latch-Up	JESD 78	10ms, 1_{tr} > 100mA

Carrier Tape & Reel Dimensions



Carrier Tape & Reel Dimensions(Cont.)



Application	A	B	C	J	T1	T2	W	P	E
SOT-23-5	178±1	72 ± 1.0	13.0 + 0.2	2.5 ± 0.15	8.4 ± 2	1.5± 0.3	8.0+ 0.3 - 0.3	4 ± 0.1	1.75± 0.1
	F	D	D1	Po	P1	Ao	Bo	Ko	t
	3.5 ± 0.05	1.5 +0.1	1.5 +0.1	4.0 ± 0.1	2.0 ± 0.1	3.15 ± 0.1	3.2± 0.1	1.4± 0.1	0.2±0.03

(mm)

Cover Tape Dimensions

Application	Carrier Width	Cover Tape Width	Devices Per Reel
SOT- 23	8	5.3	3000

Customer Service

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