GOB256UV6431(A)-(67/84/100/125)Q-S

2MByte (256K x 64) CMOS Synchronous Graphic Module

General Description

The GOB256UV6431(A)-(67/84/100/125)Q-S is a high performance, 2-megabtye synchronous, graphic RAM module organized as 256K words by 64 bits, in a 144-pin, small outline dual-in-line memory module (SODIMM) package.

The module utilizes two Fujitsu MB81G83222-(015/012/010/008)PQ CMOS 256Kx32 synchronous graphic RAMs in surface mount package (QFP) on an epoxy laminated substrate. Each device is accompanied by a decoupling capacitor for improved noise immunity.

GOB256UV6431 : Parallel Presence Detect (Resistor Strapping Option)
GOB256UV6431A: A 256 Byte Serial EEPROM contains the module configuration information.

Features

- High Density: 2MByte
- Cycle Time: 8ns (125MHz), 10ns (100MHz), 12ns (84MHz), 15ns (67MHz)
- Low Power: Active 2.5W (125MHz), 2.0W (100MHz), 1.8W (84MHz), 1.5W (67MHz)
- LVTTL-compatible inputs and outputs
- Separate power and ground planes to improve noise immunity
- Single power supply of 3.3V±0.3V
- Height: 1.250 inch

ABSOLUTE MAXIMUM RATINGS

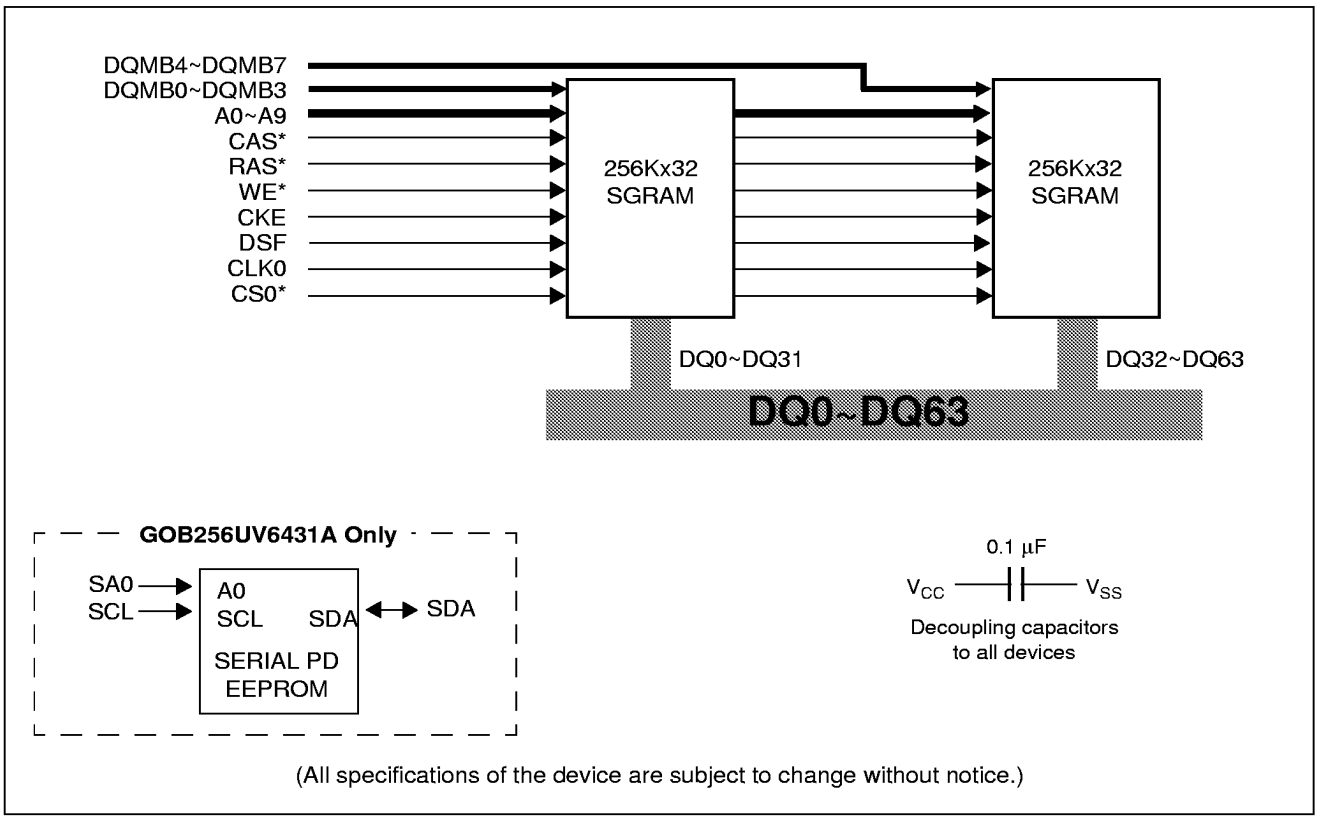
Item	Symbol	Ratings	Unit
Voltage on any pin relative to V_{SS}	V_T	-0.5 to +4.6	V
Power Dissipation	P_T	2.4	W
Operating Temperature	T_{opr}	0 to +70	°C
Storage Temperate	T_{stg}	-55 to +125	°C
Short Circuit Output Current	I_{OS}	±50	mA

RECOMMENDED DC OPERATING CONDITIONS

(T_A = 0 to +70 °C)

Symbol	Parameter	Min	Typ	Max	Unit
V_{CC}	Supply Voltage	3.0	3.3	3.6	V
V_{SS}	Ground	0	0	0	V
V_{IH}	Input High voltage	2.0	-	V_{CC}+0.5	V
V_{IL}	Input Low voltage	-0.5	-	0.8	V

Functional Diagram



(All specifications of the device are subject to change without notice.)

Notes: 1. CLK,CKE,RAS*,CAS*,WE*,DSF and Address are terminated using 10Ω series resistors.

2. Data lines (DQ29~DQ31) have resistor strapping option of 4.7KΩ.

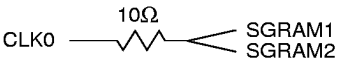
Cycle Time	DQ 31	DQ30	DQ29
8 ns	0	1	1
10 ns	0	1	0
12 ns	0	0	1
15 ns	0	0	0

0:Vss 1:Vcc

3. DQMs vs Data I/Os

DQMB0 controls DQ0 ~ DQ7
DQMB1 controls DQ8 ~ DQ15
DQMB2 controls DQ16 ~ DQ23
DQMB3 controls DQ24 ~ DQ31
DQMB4 controls DQ32 ~ DQ39
DQMB5 controls DQ40 ~ DQ47
DQMB6 controls DQ48 ~ DQ55
DQMB7 controls DQ56 ~ DQ63

4. Clock Wiring



5. GOB256UV6431A Only : A1 & A2 of the serial PD EEPROM are grounded.

Pin Name

A0~A8	Row Addresses	SA0	Decode Input
A0~A7	Column Addresses	CS0*	Chip Selects
A9	Bank Select Address	WE*	Write Enable
DQ0~DQ63	Data Inputs/Outputs	SCL	Serial Clock
CLK0	Clock Inputs	SDA	Serial Data Input/Output
CKE	Clock Enable	DSF	Define Special Function
RAS*	Row Address Strobe	V_{CC}	Power Supply
CAS*	Column Address Strobe	V_{SS}	Ground
DQMB0-DQMB7	DQ Mask Enables	NC	No Connection

Pin No.	Pin Designation	Pin No.	Pin Designation	Pin No.	Pin Designation	Pin No.	Pin Designation
1	V_{SS}	2	V_{SS}	73	NC	74	CLK0
3	DQ63	4	DQ62	75	V_{CC}	76	V_{CC}
5	DQ61	6	DQ60	77	NC	78	NC
7	DQ59	8	DQ58	79	NC	80	NC
9	DQ57	10	DQ56	81	A9	82	A8
11	V_{CC}	12	V_{CC}	83	A7	84	A6
13	DQ55	14	DQ54	85	V_{SS}	86	V_{SS}
15	DQ53	16	DQ52	87	A5	88	A4
17	DQ51	18	DQ50	89	A3	90	A2
19	DQ49	20	DQ48	91	A1	92	A0
21	V_{SS}	22	V_{SS}	93	V_{CC}	94	V_{CC}
23	DQMB7	24	DQMB6	95	DQ31	96	DQ30
25	DQMB5	26	DQMB4	97	DQ29	98	DQ28
27	V_{CC}	28	V_{CC}	99	DQ27	100	DQ26
29	DQ47	30	DQ46	101	DQ25	102	DQ24
31	DQ45	32	DQ44	103	V_{SS}	104	V_{SS}
33	DQ43	34	DQ42	105	DQ23	106	DQ22
35	DQ41	36	DQ40	107	DQ21	108	DQ20
37	V_{SS}	38	V_{SS}	109	DQ19	110	DQ18
39	DQ39	40	DQ38	111	DQ17	112	DQ16
41	DQ37	42	DQ36	113	V_{CC}	114	V_{CC}
43	DQ35	44	DQ34	115	DQMB3	116	DQMB2
45	DQ33	46	DQ32	117	DQMB1	118	DQMB0
47	V_{CC}	48	V_{CC}	119	V_{SS}	120	V_{SS}
49	NC	50	NC	121	DQ15	122	DQ14
51	NC	52	NC	123	DQ13	124	DQ12
53	NC	54	NC	125	DQ11	126	DQ10
55	V_{SS}	56	V_{SS}	127	DQ9	128	DQ8
57	DSF	58	NC	129	V_{CC}	130	V_{CC}
59	NC	60	NC	131	DQ7	132	DQ6
61	NC	62	SA0 (Note)	133	DQ5	134	DQ4
63	V_{CC}	64	V_{CC}	135	DQ3	136	DQ2
65	NC	66	CS0*	137	DQ1	138	DQ0
67	RAS*	68	CAS*	139	V_{SS}	140	V_{SS}
69	WE*	70	CKE	141	SDA (Note)	142	SCL (Note)
71	V_{SS}	72	V_{SS}	143	V_{CC}	144	V_{CC}

Note: SA0, SDA and SCL are NC for GOB256UV6431

SERIAL PD INFORMATION (GOB256UV6431A ONLY)

		Function Supported				Hex Value			
Byte#	Function Described	125 Mhz	100 Mhz	84 Mhz	67 Mhz	125 Mhz	100 Mhz	84 Mhz	67 Mhz
0	# Bytes Written into serial memory at module mfr	128 bytes				80h			
1	Total # bytes of SPD memory device	256 bytes				08h			
2	Fundamental memory type	SGRAM				05h			
3	# Row Address on this assembly	9				09h			
4	# Column Addresses on this assembly	8				08h			
5	# Module Banks on this assembly	1				01h			
6	Data Width of this assembly	64 bits				40h			
7	Data Width of this assembly (continued)					00h			
8	Voltage interface standard of this assembly	LVTTL				01h			
9	SGRAM cycle time at CL=3 (tCLK)	8ns	10ns	12ns	15ns	80h	A0h	C0h	F0h
10	SGRAM Access from Clock at CL=3 (tAC)	7.5ns	9.0ns	11ns	12ns	75h	90h	B0h	C0h
11	DIMM configuration type	Non-Parity				00h			
12	Refresh Rate/Type	S/R, Normal 15.6 ms				80h			
13	SGRAM Width Primary DRAM	x32				20h			
14	ECC SGRAM Data Width	N/A				00h			
15	Min. clock delay, Back to Back Random Column Addresses (ICCD)	1CLK				01h			
16	Burst Length Supported	1, 2, 4, 8 & Full				8Fh			
17	# Banks on each SDRAM device	2				02h			
18	CAS# Latency	1, 2, 3				07h			
19	CS# Latency	0				01h			
20	Write Latency	0				01h			
21	SGRAM Module Attribute	Non-Buffered/Registered				00h			
22	SGRAM Device Attribute	Vcc, B/R, S/W, P/A, A/P				0Eh			
23	Min Clock cycle Time at CL=2 (tCLK)	12ns	15ns	17.5ns	20ns	C0h	F0h	25h	50h
24	Max. Data Access Time from clock at CL=2 (tAC)	11.0ns	13.0ns	14.5ns	16ns	B0h	D0h	E5h	10h
25	Min Clock cycle Time at CL=1 (tCLK)	24ns	30ns	35ns	40ns	18h	1Eh	23h	28h
26	Max. Data Access Time from clock at CL=1 (tAC)	23ns	28ns	32ns	35ns	17h	1Ch	20h	23h
27	Min. Row Precharge Time (tRP)	24ns	30ns	36ns	45ns	18h	1Eh	24h	2Dh
28	Min. Row Active Delay (tRRD)	16ns	20ns	24ns	30ns	10h	14h	18h	1Eh
29	Min. RAS to CAS Delay (tRCD)	24ns	30ns	35ns	40ns	18h	1Eh	23h	28h
30	Min. RAS Pulse Width (tRAS)	48ns	60ns	70ns	80ns	30h	3Ch	46h	50h
31	Module Bank Density	N/A				00h			
32	Input Setup Time (tSI) for Add. & CMD	2.5ns	3ns	3.5ns	3.5ns	25h	30h	35h	35h
33	Input Hold Time (tHI) for Add. & CMD	1ns	1ns	1.5ns	1.5ns	10h	10h	15h	15h
34	Input Setup Time (tSI) for Data	2.5ns	3ns	3.5ns	3.5ns	25h	30h	35h	35h
35	Input Hold Time (tHI) for Data	1ns	1ns	1.5ns	1.5ns	10h	10h	15h	15h
36	Write Block Size	8 Columns				03h			
37-61	Superset Information					FFh			
62	SPD Revision	Rev. 1.2				12h			
63	Checksum for bytes 0-62								

SERIAL PD INFORMATION (CONTINUED)

Byte#	Function Described	Function Supported				Hex Value			
		125 Mhz	100 Mhz	84 Mhz	67 Mhz	125 Mhz	100 Mhz	84 Mhz	67 Mhz
64	Manufacturers JEDEC ID code per JEP-106E	Continuation code				7Fh			
65	Manufacturers JEDEC ID code per JEP-106E	SMART's ID				94h			
66-71	Manufacturers JEDEC ID code per JEP-106E	None				FFh			
72	Manufacturing location	Mfr Specific Data							
73	Manufacturer's Part Number	G				47h			
74	Manufacturer's Part Number	O				4Fh			
75	Manufacturer's Part Number	B				42h			
76	Manufacturer's Part Number	2				32h			
77	Manufacturer's Part Number	5				35h			
78	Manufacturer's Part Number	6				36h			
79	Manufacturer's Part Number	U				55h			
80	Manufacturer's Part Number	V				56h			
81	Manufacturer's Part Number	6				36h			
82	Manufacturer's Part Number	4				34h			
83	Manufacturer's Part Number	3				33h			
84	Manufacturer's Part Number	1				31h			
85	Manufacturer's Part Number	A				41h			
86	Manufacturer's Part Number	1	1	8	6	31h	31h	38h	36h
87	Manufacturer's Part Number	2	0	4	7	32h	30h	34h	37h
88	Manufacturer's Part Number	5	0	Q	Q	35h	30h	51h	51h
89	Manufacturer's Part Number	Q	Q	S	S	51h	51h	53h	53h
90	Manufacturer's Part Number	S	S	None	None	53h	53h	FFh	FFh
91	Revision Code	Mfr Specific Data				Mfr Specific Data			
92	Revision Code	None				FFh			
93	Manufacturing Date	DATE				DATE			
94	Manufacturing Date	DATE				DATE			
95-98	Assembly Serial Number	Serial Number				S.No.			
99	Manufacturer Specific Data	S				53h			
100	Manufacturer Specific Data	M				4Dh			
101	Manufacturer Specific Data	A				41h			
102	Manufacturer Specific Data	R				52h			
103	Manufacturer Specific Data	T				54h			
104	Manufacturer Specific Data	M				4Dh			
105	Manufacturer Specific Data	o				6Fh			
106	Manufacturer Specific Data	d				64h			
107	Manufacturer Specific Data	u				75h			
108	Manufacturer Specific Data	l				6Ch			
109	Manufacturer Specific Data	a				61h			
110	Manufacturer Specific Data	r				72h			
111	Manufacturer Specific Data	T				54h			
112	Manufacturer Specific Data	e				65h			
113	Manufacturer Specific Data	c				63h			
114	Manufacturer Specific Data	h				68h			
115	Manufacturer Specific Data	n				6Eh			
116	Manufacturer Specific Data	o				6Fh			
117	Manufacturer Specific Data	l				6Ch			
118	Manufacturer Specific Data	o				6Fh			
119	Manufacturer Specific Data	g				67h			
120	Manufacturer Specific Data	i				69h			
121	Manufacturer Specific Data	e				65h			
122	Manufacturer Specific Data	s				73h			
123	Manufacturer Specific Data	None				FFh			
124	Manufacturer Specific Data	None				FFh			
125	Manufacturer Specific Data	None				FFh			
126	Intel Spec Frequency	66MHz				66h			
127	Intel Spec Detail for 100MHz	N/A				00h			
128-255	Open for CPQ Use for Read & Write	None				FFh			

DC CHARACTERISTICS

(V_{CC} = 3.3V±0.3V, V_{SS} = 0V, T_A = 0 to +70 °)

Parameter	Symbol	Test Condition	125		100		84		67		Unit	Note
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.		
Operating Current	I_{CC1}	No Burst, t_{CK} = min. t_{RC} = min.	-	450	-	370	-	320	-	280	mA	1, 2
		No Burst, t_{CK} = min., t_{RC} = min. All Banks Active	-	690	-	560	-	490	-	420	mA	1, 2
Precharge Standby Current	I_{CC2}	CKE -V_{IL}, t_{CK} = min. All Banks Idle	-	4	-	4	-	4	-	4	mA	1, 2
		CKE = V_{IH}, t_{CK} = min. All Banks Idle	-	160	-	140	-	130	-	110	mA	1.2
Active Standby Current	I_{CC3}	CKE = V_{IL}, t_{CK} = min. Any Bank Active	-	70	-	70	-	70	-	70	mA	1, 2
		CKE = V_{IH}, t_{CK} = min. Any Bank Active	-	180	-	150	-	140	-	120	mA	1, 2
Burst Mode Current	I_{CC4}	t_{CK} = min.	-	600	-	500	-	420	-	350	mA	1, 2
Refresh Current	I_{CC5}	t_{CK} = min., t_{RC} = min., t_{RRD} = min. Auto Refresh	-	570	-	470	-	410	-	350	mA	1, 2
Self Refresh Current	I_{CC6}	CKE - V_{IL}	-	4	-	4	-	4	-	4	mA	1, 2
Input Leakage	I_{LI}	0V ≤ V_{in} ≤ V_{CC}	-10	10	-10	10	-10	10	-10	10	µA	
Output Leakage Current	I_{LO}	0V ≤ V_{out} ≤ V_{CC} D_{out} = Disable	-10	10	-10	10	-10	10	-10	10	µA	
Output High Voltage	V_{OH}	High I_{out} = -2mA	2.4	-	2.4	-	2.4	-	2.4	-	V	
Output Low Voltage	V_{OL}	Low I_{out} = 2mA	-	0.4	-	0.4	-	0.4	-	0.4	V	

†CL = CAS* Latency

Notes: 1. I_{CC} depends on output load condition when the device is selected I_{CC} (max.) is specified at the output open condition.

2. An initial pulse of 200µs is required after power-up followed by a minimum of eight Auto-Refresh-Cycles.

CAPACITANCE

(TA =+25°C, VCC = 3.3V±0.3V)

Parameter	Symbol	Max.	Unit	Note
Input Capacitance (Address, WE*, CKE, RAS*, CAS*)	C_{I1}	13	pF	1
Input Capacitance (DQMBs)	C_{I2}	9	pF	1
Input Capacitance (CS0*,CS1*)	C_{I3}	13	pF	1
Input Capacitance (CLK0, CLK1)	C_{I4}	13	pF	1
Input/Output Capacitance (DQ0~DQ63)	$C_{I/O}$	12	pF	1, 2

Notes: 1. Capacitance is measured with Boonton Meter or effective capacitance method.

2. CAS* - V_{IH} to disable D_{out}.

AC CHARACTERISTICS

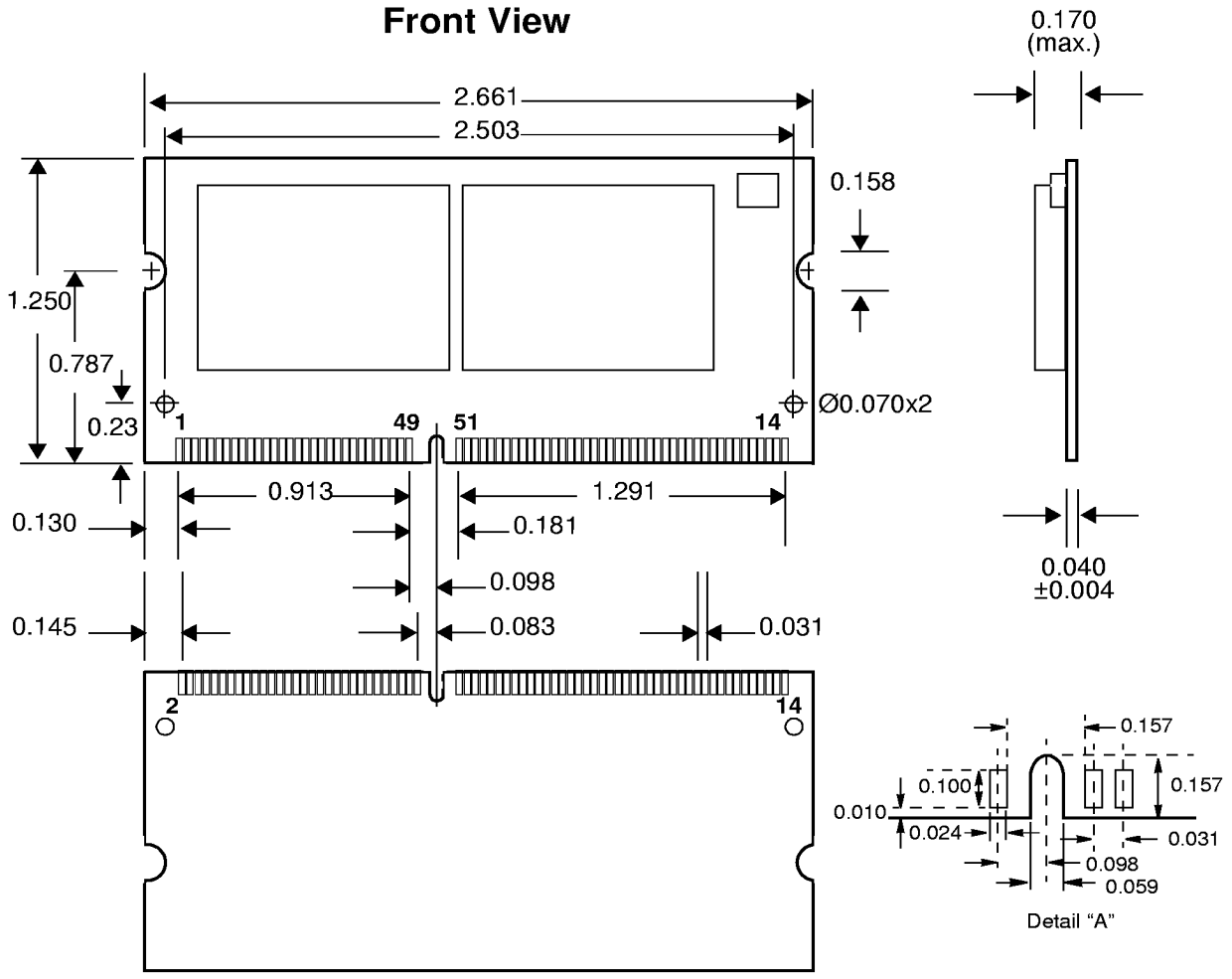
(TA = 0 to +70°C, V_{CC} = 3.3V±0.3V, V_{SS} = 0V)

Parameter		Symbol	Unit	125		100		84		67		Notes
Clock Period	CL=3	t_{CK}	ns	8	-	10	-	12	-	15	-	1, 2, 3, 6
	CL=2			12	-	15	-	17.5	-	20	-	
	CL=1			24	-	30	-	35	-	40	-	
Transition Time		t_T	ns	0.5	30	0.5	30	0.5	30	0.5	30	1, 2, 3
Clock High Time		t_{CH}	ns	3.5	-	3.5	-	4	-	5	-	1, 2, 3
Clock Low Time		t_{CL}	ns	3.5	-	3.5	-	4	-	5	-	1, 2, 3
Data Input Setup Time		t_{DS}	ns	2.5	-	3.0	-	3.5	-	3.5	-	1, 2, 3
Data Input Hold Time		t_{DH}	ns	1.0	-	1.0	-	1.5	-	1.5	-	1, 2, 3
Access Time from Clock	CL=3	t_{AC}	ns	-	7.5	-	9	-	11	-	12	1, 2, 3
	CL=2			-	11	-	13	-	14.5	-	16	
	CL=1			-	23	-	28	-	32	-	35	
Output In Low-Z		t_{LZ}	ns	2	-	3	-	3	-	3	-	1, 2, 3
Output in High-Z	CL=3	t_{HZ}	ns	3	8	4	10	4	12	4	15	1, 2, 3, 4
	CL=2				12		15		17.5		20	
	CL=1				16		20		24		30	
Output Hold Time		t_{OH}	ns	2	-	4	-	4	-	4	-	1, 2, 3
Time between Refresh		t_{REF}	ms	-	16.4	-	16.4	-	16.4	-	16.4	1, 2, 3
RAS Cycle Time		t_{RC}	ns	72	-	90	-	106	-	125	-	1, 2, 3, 5
RAS Access Time		t_{RAC}	ns	-	45	-	58	-	67	-	75	1, 2, 3
CAS Access Time		t_{CAC}	ns	-	23	-	28	-	32	-	35	1, 2, 3
RAS Precharge Time		t_{RP}	ns	24	-	30	-	36	-	45	-	1, 2, 3
RAS Active Time		t_{RAS}	ns	48	100000	60	100000	70	100000	80	100000	1, 2, 3
RAS to CAS Delay Time		t_{RCD}	ns	24	-	30	-	35	-	40	-	1, 2, 3
Write Recovery Time		t_{WR}	ns	8	-	10	-	12	-	15	-	1, 2, 3
Write to Precharge Lead Time		t_{RWL}	ns	12	-	15	-	17.5	-	20	-	1, 2, 3
RAS to RAS Delay Time		t_{RRD}	ns	16	-	20	-	24	-	30	-	1, 2, 3
Power-down Exit Time		t_{PDE}	ns	10	-	12	-	14	-	17	-	1, 2, 3
CKE to Clock Disable		l_{CKE}	cycle	1		1		1		1		
DQM to Output in High-Z		l_{DQZ}	cycle	2		2		2		2		
DQM to Input Data Delay		l_{DQD}	cycle	0		0		0		0		
Last Output to Write Command Delay		l_{OWD}	cycle	2		2		2		2		
Write Command to Input Data Delay		l_{DWD}	cycle	0		0		0		0		
Precharge to Output in High-Z Delay	CL=3	l_{ROH}	cycle	3		3		3		3		
	CL=2			2		2		2		2		
	CL=1			1		1		1		1		
Mode Register Access to Bank Active (min.)		l_{MRD}	cycle	2		2		2		2		
CAS to CAS Delay		l_{CCD}	cycle	1		1		1		1		
CAS Bank Delay		l_{CBD}	cycle	1		1		1		1		

Notes:
1. An initial pulse of at least 200ms is required after power-up followed by a minimum of eight auto refresh cycles.
2. AC characteristics assume t_T = 1ns and 50pF capacitive load. If t_T is longer than 1ms, reference level for measuring time of input signal is V_{IH} (min.) and V_{IL} (max.).
3. 1.4V is the reference level for measuring timing of input signals.
4. t_{HZ} and t_{OH} defines the time at which the outputs achieve ±200mV.
5. Actual clock output of t_{RC} will be sum clock of t_{RAS} and t_{RP}.
6. 20ns is not supported in SPD.

Physical Dimensions

144-pin (72x2) DIMM



(All dimensions are in inches with 0.005" tolerance unless otherwise specified. Drawing not to scale.)

Ordering Information

G	O	B	256	U	V	64	3	1	A	-	100	Q	-	S
(1)	(2)	(3)	(4)	(5)	(6)	(7)	(8)	(9)	(10)		(11)	(12)	(13)	

(1) **Memory Type**
S : SDRAM
G : SGRAM

(2) **Module Shape**
S : SIMM
D : DIMM
O : Small Outline DIMM

(3) **Module Pin Count**
A : 72-pin
B : 144-pin
C : 168-pin
D : 184-pin
E : 200-pin

(4) **Word Depth**
1 : 1M
2 : 2M
4 : 4M
8 : 8M
256 : 256K
512 : 512K

(5) **Buffer Type**
B : Buffered
U : Unbuffered

(6) **Operating Voltage & Power Consumption**
V : 3.3V & LVTTL & Standard Power
L : 3.3V & LVTTL & Low Power
S : 3.3V & SSTL & Standard Power

(7) **Data Width**
(ex. 64=x64, 72=x72 etc.)

(8) **Device Configuration**
4 : x4
8 : x8
1 : x16
3 : x32

(9) **Refresh**
1 : 1kR
2 : 2kR

(10) **Module Revision / Applied "Standard"** *1
Blank : Rev. 0
A : Rev. 1
B : Rev. 2 (etc.)

*1 When DRAM device or PCB is revised, the revision is changed

(11) **Clock Frequency**
67 : 67Mhz
84 : 84Mhz
100 : 100Mhz
125 : 125Mhz

(12) **Package of Component**
J : SOJ
T : TSOP
Q : QFP

(13) **Assembly & Test Site**
S : Smart Modular Technologies