

DESCRIPTION

The HYM532256A is a 256K x 32-bit Fast page mode CMOS DRAM module consisting of eight HY534256A in 20/26 pin SOJ on a 72 pin glass-epoxy printed circuit board. 0.22 μ F decoupling capacitor is mounted for each DRAM. The HYM532256AM/ALM are Tin-Lead plated and HYM532256AMG/ALMG are Gold plated socket type Single In-line Memory Modules suitable for easy interchange and addition of 1M byte memory.

FEATURES

- Low power dissipation
 - Max. battery back-up 17.6mW (L-part)
 - Max. CMOS standby 8.8mW (L-part)
 - 44.0mW

Max. TTL standby 88.0mW

Max. operating

Speed	Power
60	3.96W
70	3.52W
80	3.08W

- Single power supply of 5V \pm 10%
- TTL compatible inputs and outputs
- Fast access time

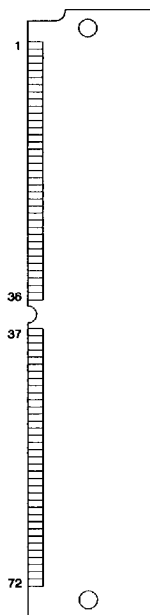
Speed	t _{RAC}	t _{CAC}	t _{PC}
60	60ns	15ns	40ns
70	70ns	20ns	40ns
80	80ns	20ns	45ns

- Fast page mode operation
- CAS-before-RAS, RAS-only, Hidden refresh
- 512 refresh cycles / 64ms (L-part)
- 512 refresh cycles / 8ms

PIN DESCRIPTION

RAS0, RAS2	Row Address Strobe
CAS0-CAS3	Column Address Strobe
WE	Write Enable
A0-A8	Address Input
DQ0-DQ31	Data Input/Output
PD1-PD4	Presence Detect
Vcc	Power (+ 5V)
Vss	Ground

PIN CONNECTION



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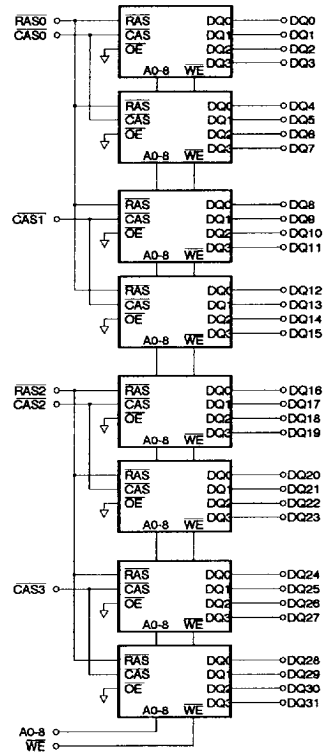
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PIN NAME

#	NAME	#	NAME
1	Vss	37	NC
2	DQ0	38	NC
3	DQ16	39	Vss
4	DQ1	40	CAS0
5	DQ17	41	CAS2
6	DQ2	42	CAS3
7	DQ18	43	CAS1
8	DQ3	44	RAS0
9	DQ19	45	NC
10	VCC	46	NC
11	NC	47	WE
12	A0	48	NC
13	A1	49	DQ8
14	A2	50	DQ24
15	A3	51	DQ9
16	A4	52	DQ25
17	A5	53	DQ10
18	A6	54	DQ26
19	NC	55	DQ11
20	DQ4	56	DQ27
21	DQ20	57	DQ12
22	DQ5	58	DQ28
23	DQ21	59	VCC
24	DQ6	60	DQ29
25	DQ22	61	DQ13
26	DQ7	62	DQ30
27	DQ23	63	DQ14
28	A7	64	DQ31
29	NC	65	DQ15
30	VCC	66	NC
31	A8	67	PD1
32	NC	68	PD2
33	NC	69	PD3
34	RAS2	70	PD4
35	NC	71	NC
36	NC	72	Vss

BLOCK DIAGRAM



PRESENCE DETECT PINS

PINS	-60	-70	-80
PD1	Vss	Vss	Vss
PD2	NC	NC	NC
PD3	NC	Vss	NC
PD4	NC	NC	Vss

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
TA	Ambient Temperature	0 to 70	°C
TSTG	Storage Temperature	-55 to 150	°C
VIN, VOUT	Voltage on Any Pin Relative to VSS	-1.0 to 7.0	V
VCC	Voltage on VCC Relative to VSS	-1.0 to 7.0	V
IOS	Short Circuit Output Current	50	mA
PD	Power Dissipation	4.8	W

NOTE : Operation at or above Absolute Maximum Ratings can adversely affect device reliability.

RECOMMENDED DC OPERATING CONDITIONS

(TA=0°C to 70°C)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
VCC	Supply Voltage	4.5	5.0	5.5	V
VIH	Input High Voltage	2.4	-	VCC + 1.0	V
VIL	Input Low Voltage	-1.0	-	0.8	V

NOTE : All voltages are referenced to VSS.

DC CHARACTERISTICS

($T_A = 0^\circ\text{C}$ to 70°C , $V_{CC} = 5\text{V} \pm 10\%$, $V_{SS} = 0\text{V}$, unless otherwise noted.)

SYMBOL	PARAMETER	TEST CONDITIONS	SPEED/ POWER	MIN.	MAX.	UNIT	NOTE
I _{LI}	Input Leakage Current (Any Input Pin)	$V_{SS} \leq V_{IN} \leq V_{CC} + 1.0$, All other pins not under test = V_{SS}		-80	80	μA	
I _{LO}	Output Leakage Current (High Impedance State)	$V_{SS} \leq V_{OUT} \leq V_{CC}$, RAS & CAS at V_{IH}		-10	10	μA	
ICC1	VCC Supply Current, Operating	trc = trc (min.)	60 70 80	- - -	720 640 560	mA	1,2,3
ICC2	VCC Supply Current, TTL Standby	RAS & CAS at V_{IH} , other inputs $\geq V_{SS}$		-	16	mA	
ICC3	VCC Supply Current, RAS-only refresh	trc = trc (min.)	60 70 80	- - -	720 640 560	mA	1,3
ICC4	VCC Supply Current, Fast Page mode	tPC = tPC (min.)	60 70 80	- - -	560 480 400	mA	1,2,3
ICC5	VCC Supply Current, CMOS Standby	RAS & CAS $\geq V_{CC} - 0.2\text{V}$	L-part	-	8 1.6	mA	5
ICC6	VCC Supply Current, CAS-before-RAS refresh	trc = trc (min.)	60 70 80	- - -	720 640 560	mA	1,3
ICC7	VCC Supply Current, Battery Back Up (L-part only)	trc = $125\mu\text{s}$, CAS = CBR cycling or 0.2V WE = $V_{CC} - 0.2\text{V}$ A0-A8 = $V_{CC} - 0.2\text{V}$ or 0.2V DQ0-DQ31 = $V_{CC} - 0.2\text{V}$, 0.2V , or open	trAS \leq 300ns trAS \leq $1\mu\text{s}$	-	2.4 3.2	mA	1,4,5
VOL	Output Low Voltage	IOL = 4.2mA		-	0.4	V	
VOH	Output High Voltage	IOH = -5mA		2.4	-	V	

NOTE :

1. ICC1, ICC3, ICC4, ICC6 and ICC7 depend on cycle rate.
2. ICC1 and ICC4 depend on output loading. Specified values are obtained with the output open.
3. It depends on user whether column address is changed or not at least once while RAS = V_{IL} and CAS = V_{IH} .
4. Only trAS(max.) = $1\mu\text{s}$ is applied to refresh of battery backup but trAS(max.) = $10\mu\text{s}$ is applied to normal functional operation.
5. ICC5(max.) = 1.6mA and ICC7 are applied to L-part only (HYM532256ALM and HYM532256ALMG).



AC CHARACTERISTICS

(TA=0°C to 70°C, VCC=5V±10%, VSS=0V, unless otherwise noted.) NOTE : 1, 2, 3

#	SYMBOL	PARAMETER	HYM532256AM/ALM/AMG/ALMG						UNIT	NOTE
			-60		-70		-80			
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
1	tRC	Random Read or Write Cycle Time	110	-	130	-	150	-	ns	
2	tRPC	RAS to CAS Precharge Time	0	-	0	-	0	-	ns	
3	tPC	Fast Page Mode Cycle Time	40	-	40	-	45	-	ns	
4	tRHCP	RAS Hold Time from CAS Precharge	30	-	35	-	35	-	ns	
5	tRAC	Access Time from RAS	-	60	-	70	-	80	ns	4,9,10
6	tCAC	Access Time from CAS	-	15	-	20	-	20	ns	4,9
7	tAA	Access Time from Column Address	-	30	-	35	-	40	ns	4,10
8	tCPA	Access Time from CAS Precharge	-	35	-	35	-	40	ns	4
9	tCLZ	CAS to Output Low Impedance	0	-	0	-	0	-	ns	4
10	tOFF	Output Buffer Turn-off Delay	0	20	0	20	0	20	ns	5
11	tT	Transition Time (Rise and Fall)	3	50	3	50	3	50	ns	3
12	tRP	RAS Precharge Time	40	-	50	-	60	-	ns	
13	tRAS	RAS Pulse Width	60	10K	70	10K	80	10K	ns	
14	tRASP	RAS Pulse Width (Fast Page Mode)	60	100K	70	100K	80	100K	ns	
15	tRSH	RAS Hold Time	15	-	20	-	20	-	ns	
16	tCSH	CAS Hold Time	60	-	70	-	80	-	ns	
17	tCAS	CAS Pulse Width	15	10K	20	10K	20	10K	ns	
18	tRCD	RAS to CAS Delay	20	45	20	50	20	60	ns	9
19	tRAD	RAS to Column Address Delay Time	15	30	15	35	15	40	ns	10
20	tCRP	CAS to RAS Precharge Time	5	-	5	-	5	-	ns	
21	tCP	CAS Precharge Time	10	-	10	-	10	-	ns	
22	tASR	Row Address Set-up Time	0	-	0	-	0	-	ns	
23	tRAH	Row Address Hold Time	10	-	10	-	10	-	ns	
24	tASC	Column Address Set-up Time	0	-	0	-	0	-	ns	
25	tCAH	Column Address Hold Time	15	-	15	-	15	-	ns	
26	tAR	Column Address Hold Time from RAS	45	-	50	-	55	-	ns	
27	tRAL	Column Address to RAS Lead Time	25	-	35	-	40	-	ns	
28	tRCS	Read Command Set-up Time	0	-	0	-	0	-	ns	
29	tRCH	Read Command Hold Time Referenced to CAS	0	-	0	-	0	-	ns	6
30	tRRH	Read Command Hold Time Referenced to RAS	0	-	0	-	0	-	ns	6
31	tWCH	Write Command Hold Time	10	-	15	-	15	-	ns	
32	tWCR	Write Command Hold Time from RAS	45	-	50	-	55	-	ns	
33	tWP	Write Command Pulse Width	10	-	15	-	15	-	ns	
34	tRWL	Write Command to RAS Lead Time	15	-	20	-	20	-	ns	
35	tCWL	Write Command to CAS Lead Time	15	-	20	-	20	-	ns	
36	tDS	Data-In Set-up Time	0	-	0	-	0	-	ns	7
37	tDH	Data-In Hold Time	15	-	15	-	15	-	ns	7
38	tDHR	Data-In Hold Time Referenced to RAS	45	-	50	-	55	-	ns	
39	tREF	Refresh Period (512 cycles)	-	8	-	8	-	8	ms	
		L-part	-	64	-	64	-	64		11
40	tWCS	Write Command Set-up Time	0	-	0	-	0	-	ns	8

AC CHARACTERISTICS

(continued)

#	SYMBOL	PARAMETER	HYM532256AM/ALM/AMG/ALMG						UNIT	NOTE
			-60		-70		-80			
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
41	tCSR	CAS Set-up Time (CBR Cycle)	5	-	5	-	5	-	ns	
42	tCHR	CAS Hold Time (CBR Cycle)	10	-	10	-	10	-	ns	
43	tCPT	CAS Precharge Time (CBR Counter Test)	40	-	40	-	40	-	ns	

NOTE :

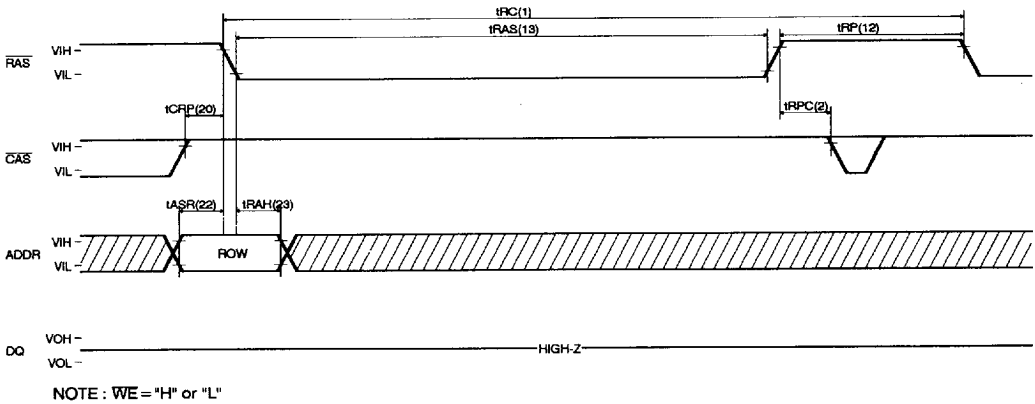
1. An initial pause of 200 μ s is required after power-up followed by 8 RAS cycles before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 CAS-before-RAS initialization cycles instead of 8 RAS-only refresh cycles are required.
2. VIH(min.) and VIL(max.) are reference levels for measuring timing of input signals. Transition time is measured between VIH and VIL and assumed to be 5ns for all inputs.
3. Refer to the HY534256A data sheet for detailed information.
4. Measured with a load equivalent to 2 TTL loads and 100pF.
5. tOFF(max.) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
6. Either tRCH or tRRH must be satisfied for a read cycle.
7. These parameters are referenced to CAS leading edge in early write cycles.
8. twCS is not a restrictive operating parameter. It is included in the data sheet as electrical characteristics only. If twCS \geq twCS(min.), the cycle is an early write cycle and data out pin will remain open circuit (high impedance) through the entire cycle.
9. Operation within the tRCD(max.) limit insures that tRAC(max.) can be met. tRCD(max.) is specified as a reference point only. If tRCD is greater than the specified tRCD(max.) limit, then access time is controlled by tCAC.
10. Operation within the tRAD(max.) limit insures that tRAC(max.) can be met. tRAD(max.) is specified as a reference point only. If tRAD is greater than the specified tRAD(max.) limit, then access time is controlled by tAA.
11. tREF(max.) = 64ms is applied to L-part only (HYM532256ALM and HYM532256ALMG).

CAPACITANCE

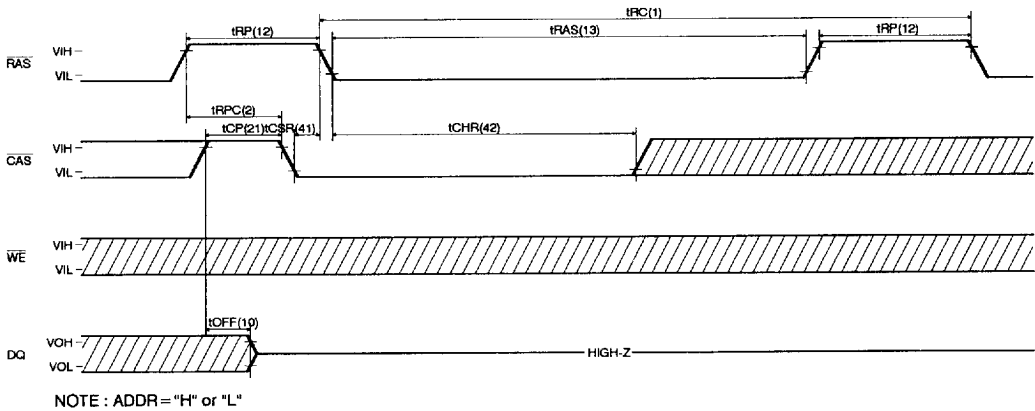
(TA = 25°C, VCC = 5V \pm 10%, VSS = 0V, f = 1MHz, unless otherwise noted.)

SYMBOL	PARAMETER	TYP.	MAX.	UNIT
CIN1	Input Capacitance (A0-A8)	-	65	pF
CIN2	Input Capacitance (WE)	-	70	pF
CIN3	Input Capacitance (RAS0, RAS2)	-	43	pF
CIN4	Input Capacitance (CAS0-CAS3)	-	17	pF
CdQ	Data Input/Output Capacitance (DQ0-DQ31)	-	17	pF

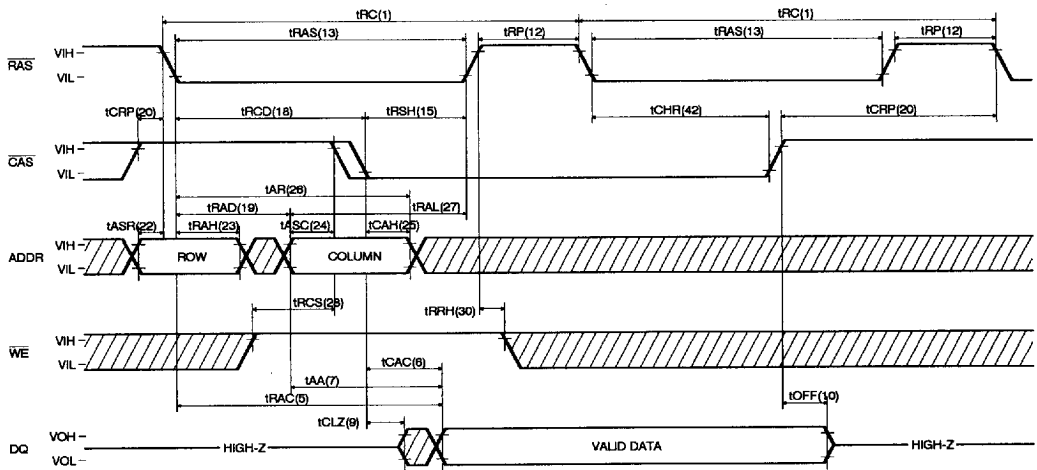
RAS-ONLY REFRESH CYCLE



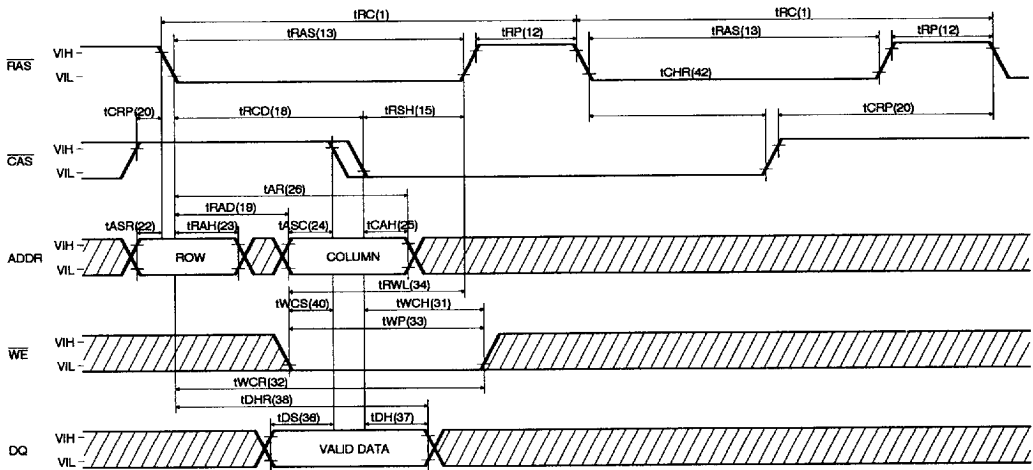
CAS-BEFORE-RAS REFRESH CYCLE



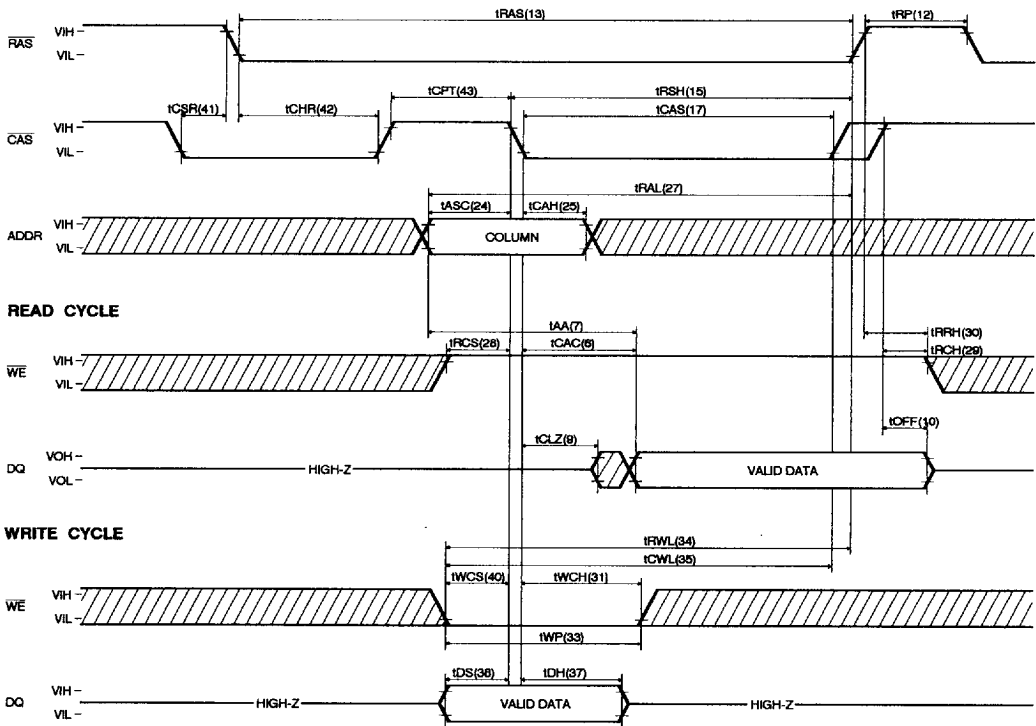
HIDDEN REFRESH CYCLE (READ)



HIDDEN REFRESH CYCLE (WRITE)



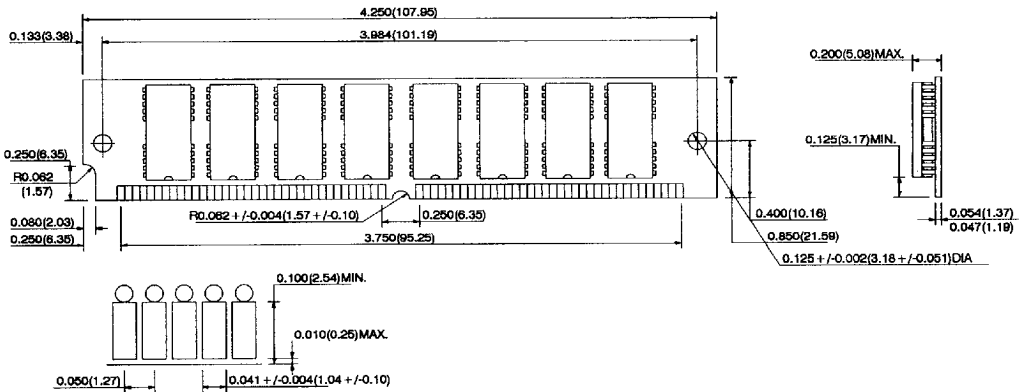
CAS-BEFORE-RAS REFRESH COUNTER TEST CYCLE



PACKAGE INFORMATION

72 pin Single In-line Memory Module (M ; Tin-Lead plated, MG ; Gold plated)

UNIT : INCH(mm)
TOLERANCE : +/-0.005(0.13)



ORDERING INFORMATION

PART NUMBER	SPEED	POWER	PACKAGE	PLATING
HYM532256AM	60/70/80		SIMM	Tin-Lead
HYM532256ALM	60/70/80	L-part	SIMM	Tin-Lead
HYM532256AMG	60/70/80		SIMM	Gold
HYM532256ALMG	60/70/80	L-part	SIMM	Gold

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