REAL TIME CLOCK MODULE
RTC-64611/64613
APPLICATION MANUAL

EPSON

■Characteristics

1. Absolute maximum ratings

Item		Symbol	Condition	Rated value	Unit
Supply voltage *		V_{DD}	—	−0.5～+7.0	V
Input voltage *		V_{IN}	—	−0.5* *～V_{DD}+0.3	V
Allowable output current		I I_O I	—	5	mA
Total allowable output current		I ΣI_O I	—	50	mA
Storage temperature	RTC-64611		V_{DD}=0V	−55～+85	°C
	RTC-64613			−55～+125	
Soldering conditions		T_{SOL}	RTC-64611 (Lead part)	Temperature: 260°C or less Time: 10 sec.	
			RTC-64613	Under 260°C within 10sec×2 or under 230°C within 3 min.	

* Allowable value for GND. * * −0.3V for 50ns pulse width

2. Operating range

Item	Symbol	Condition	Range	Unit
Supply voltage	V_{DD}	Ta=−20～+75°C	4.5～5.5	V
Operating temperature	T_{OPR}	V_{DD}=4.5～5.5V	−20～+75	°C

3. Frequency characteristics

Item		Condition	Range	Unit
Frequency tolerance	RTC-64611A	Ta=25°C V_{DD}=5V	+15／− 5 (5±10)	PPM
	RTC-64611B		+55／−45 (5±50)	
	RTC-64613A		+25／−15 (5±20)	
	RTC-64613		+55／−45 (5±50)	
Temperature characteristics		−10～+70°C (Standard at 25°C)	+10／−120	PPM
		−20～+75°C (Standard at 25°C)	+10／−220	
Aging		Ta=25°C, V_{DD}=5V first year	± 5	PPM/year
Voltage characteristics		Ta=25°C, V_{DD}=4.5～5.5V	± 5	PPM/V

4. Data holding characteristics at low supply voltages

Item	Symbol	Condition	MIN	TYP	MAX	Unit
Data holding voltage	V_{DR}	$\overline{CS}$≧V_{DD}−0.2V	2.0	—	4.5	V
Data holding current consumption	I_{DDDR}	V_{DD}=2.0, $\overline{CS}$≧1.8V H.START/$\overline{STOP}$≧1.8V $\overline{IRQ}$ with 1 MHz kept open.	—	—	2.0	μA
Chip select data hold time	T_{CDR}	See Fig. 1.	0	—	—	ns
Operation recovery time	T_R		85 (t_{RC})	—	—	ns

Note: t_{RC}……Read cycle time

5. Oscillation characteristics and control signal timing.

Item	Symbol	Condition	MIN	TYP	MAX	Unit	
Crystal oscillation start time	T_{OSC}	See Fig. 2.	—	—	3.0	sec	(Note 1)
$\overline{IRQ}$ release time	T_{IR}	See Fig. 3.	—	—	2.0	μsec	
H.START/$\overline{STOP}$ control delay time	T_{HSD}	See Fig. 4.	—	—	185	μsec	

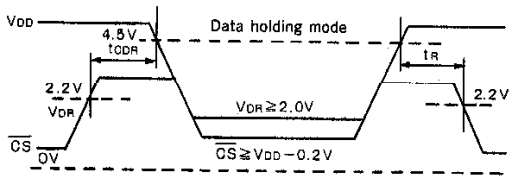
Note 1: Oscillation start is defined as Ta=−20～+75°C at the applied voltage of V_{DD}=5V±10%.
The oscillation start time at V_{DD}=4.5V or less cannot be specified.
Start at temperature: Ta=−20～+75°C.

Item	Symbol	Condition	MIN	TYP	MAX	Unit
Reset delay time	T_{RD}	See Fig. 5.	—	—	125	μsec
Reset time	T_{RST}		—	122	125	μsec
ADJ delay time	T_{AD}	See Fig. 6.	—	—	125	μsec
ADJ time	T_{ADJ}			122	125	μsec

Note 2: When Reset and ADJ have been set, set the next Reset and ADJ after operation is finished.
Both Reset and ADJ may be set simultaneously.

RTC-64611/64613

Fig.1 Low Voltage Data holding Wave Form



Note: $\overline{CS}$ control the address buffer, data buffer, $\overline{WE}$ buffer, and $\overline{OE}$ buffer. When the battery backup mode is controlled, the V_{IN} level (address, data, and $\overline{WE}$ and $\overline{OE}$) may be at a high impedance.

Fig.2 Oscillation start time of Timing Wave Form

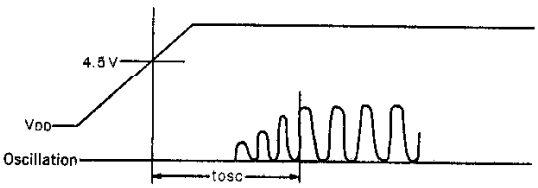


Fig.3 $\overline{IRQ}$ Control Timing

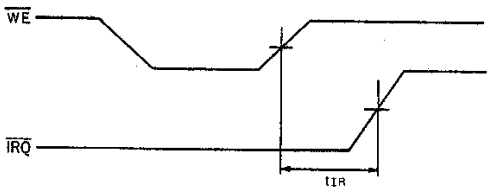


Fig.4 H-START/$\overline{STOP}$ Control Timing

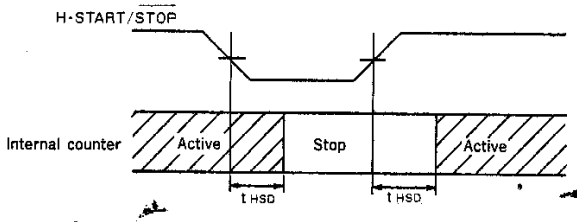


Fig.5 RESET Control Timing

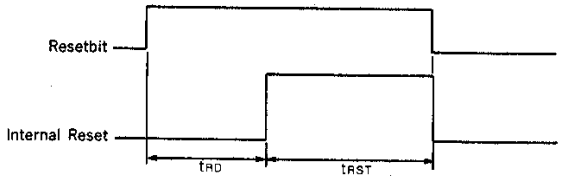
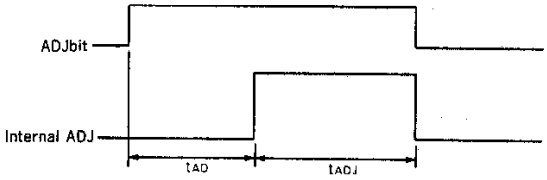


Fig.6 ADJ Control Timing



6. DC characteristics

(Unless otherwise specified, GND = 0V, Ta = −20 ~ +75°C)

Item	Symbol	Measuring conditions	V_{DD} = 5V ± 10%		V_{DD} = 2V		Unit
			MIN	MAX	MIN	MAX	
High level input voltage	V_{IH}	——	2.2	V_{DD}	V_{DD} − 0.2	V_{DD}	V
Low level input voltage	V_{IL}	——	−0.3	0.8	−0.3	0.2	V
Input leak current	I_{IN}	——	—	± 2	—	± 2	μA
Three-state leak current	I_{TSL}	——	—	±10	—	±10	μA
Output leak current	I_{LOH}	——	—	±10	—	±10	μA
High level output voltage (excl. 1Hz, $\overline{IRQ}$)	V_{OH}	I_{OH} = −1mA	2.4	—	—	—	V
Low level output voltage	V_{OL}	I_{OL} = 2.1mA	—	0.4	—	—	V
Input capacity	C_{IN}	V_{IN} = 0V Ta = 25°C f = 1.0MHz	—	12.5	—	—	pF
Output capacity	C_{ONT}		—	12.5	—	—	pF
Current consumption (at bus access)	I_{DD}	No load. min. cycle	—	2.0	—	—	mA

7. AC characteristics (Unless otherwise specified,)

(1) AC characteristics measuring conditions (applicable to the read and write cycles)

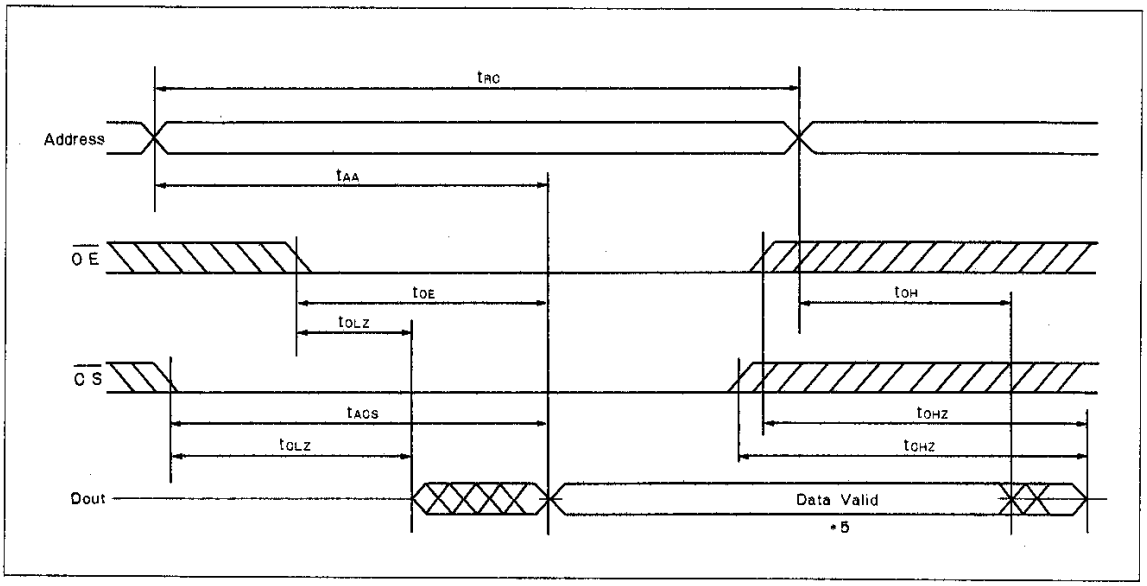
① Input pulse level: 0.8-2.4V
② Input rise/fall time: 5 ns
③ I/O timing reference level: 1.5V
④ Output load: 1 TTL gate + C_L (100pF)
(including the scope and jig capacity)

(2) Read cycle

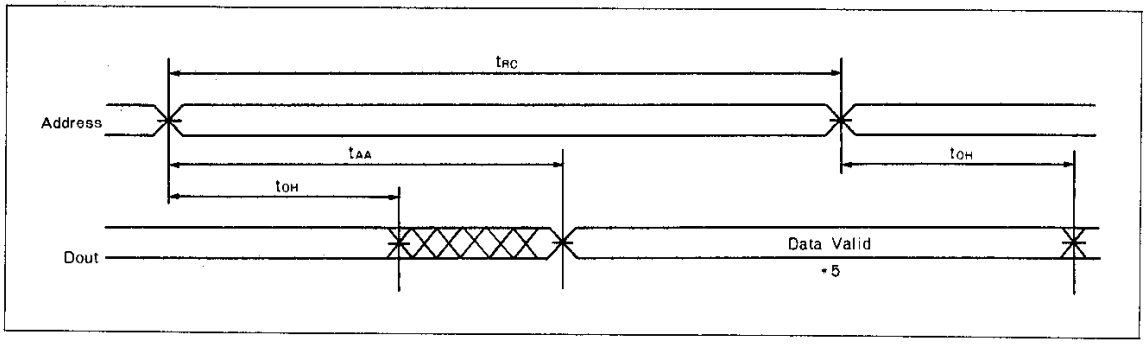
Read cycle	Symbol	MIN	MAX	Unit
Read cycle time	t_{RC}	85	—	ns
Address access time	t_{AA}	—	85	ns
Chip select access time	t_{ACS}	—	45	ns
Output enable access time	t_{OE}	—	45	ns
Output hold time	t_{OH}	10	—	ns
Chip select/output set time	t_{CLZ}	10	—	ns
Output enable /output set time	t_{OLZ}	5	—	ns
Chip deselect/output floating	t_{CHZ}	0	35	ns
Output disable/output floating	t_{OHZ}	0	35	ns

Note: The bus cannot be accessed in Battery Backup mode.

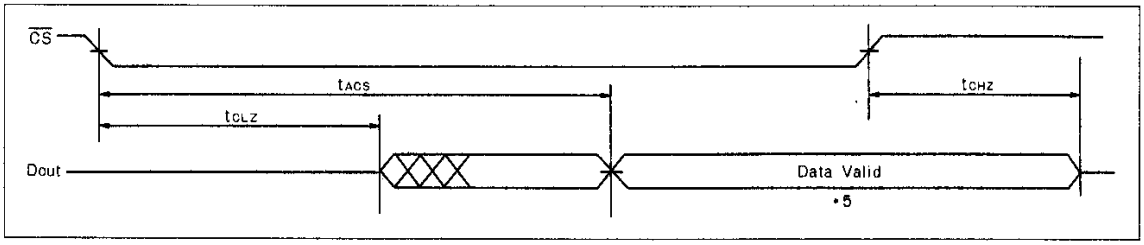
① Read cycle-1 timing wave form *1



② Read cycle-2 timing wave form *1, *2, and *4



③ Read cycle-3 timing wave form *1, and *4



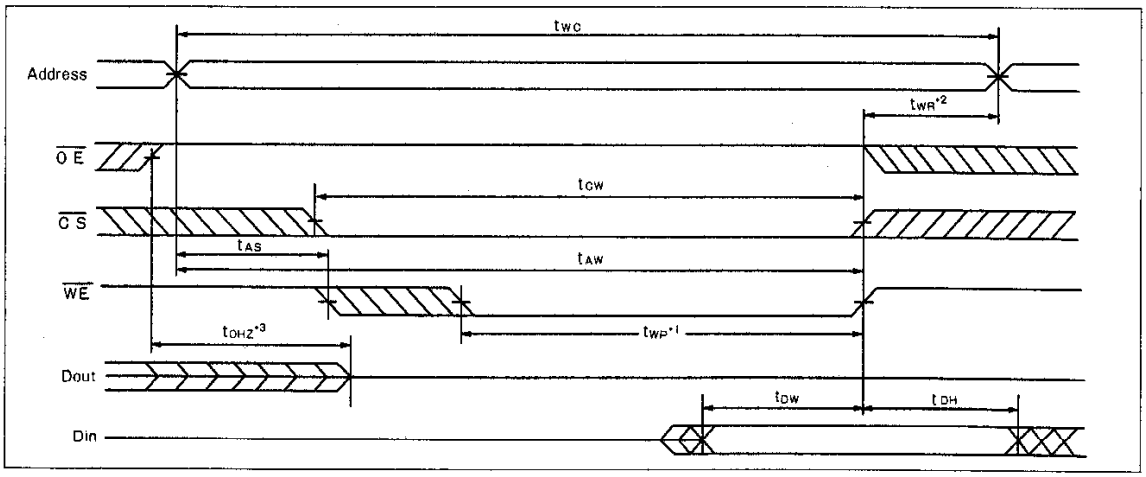
* 1. In read cycle, keep WE "High".
* 2. The device is always selected in $\overline{CS}=V_{IL}$.
* 3. The address must be defined simultaneously with or before activation of CS.
* 4. $\overline{OE}=V_{IL}$
* 5. During read, read data varies as the contents of the register change.

(3) Write cycle

Item	Symbol	MIN	MAX	Unit
Write cycle time	t_{WC}	85	—	ns
Chip select time	t_{CW}	75	—	ns
Address valid time	t_{AW}	75	—	ns
Address setup time	t_{AS}	0	—	ns
Write pulse time	t_{WP}	60	—	ns
Address holding time	t_{WR}	10	—	ns
WE output floating	t_{WHZ}	0	35	ns
Input date set time	t_{DW}	40	—	ns
Input date hold time	t_{DH}	0	—	ns
Output disable/output floating	t_{OHZ}	0	35	ns
WE output set time	t_{OW}	5	—	ns

Note: During battery backup, the bus cannot be accessed.

① Write cycle 1 timing wave from (when the OE clock is used)



* 1. Write is executed while CS="Low" overlaps with WE="Low" (t_{WP}).
* 2. The t_{WR} is measured from the"High" transition of CS or WE, whichever is earlier, to the end of the write cycle.
* 3. During this period, the I/O terminal is in the the output state. Do not apply an input signal with opposite phase to the output.

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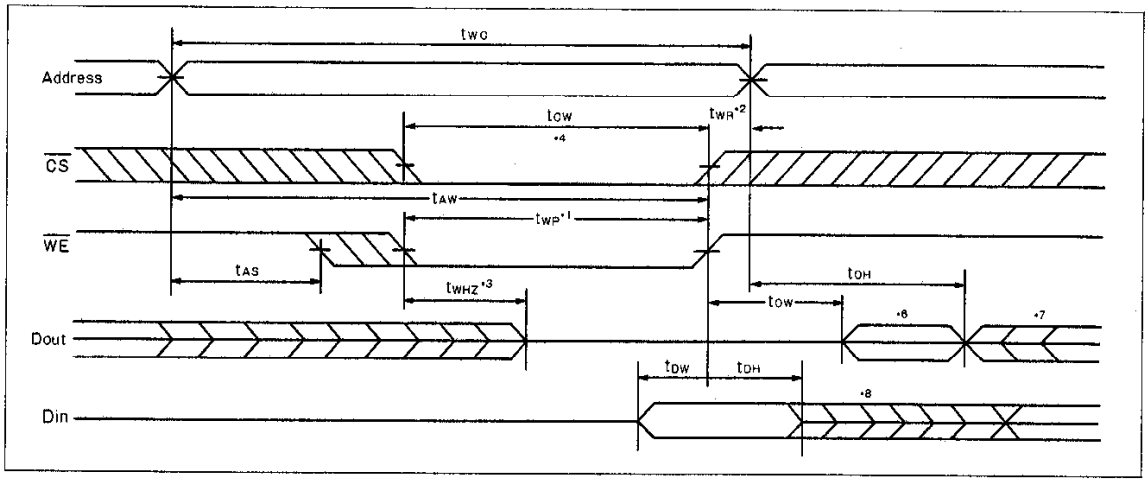
② Write cycle 2 timing wave form (when $\overline{OE}$ = GND is fixed)



* 1. Write is executed while $\overline{CS}$ = "Low" is overlapped with $\overline{WE}$ = "Low" (t_{WP}).
* 2. The t_{WR} is measured from the "High" transition of $\overline{CS}$ or $\overline{WE}$, whichever is earlier, to the end of the write cycle.
* 3. During this period, the I/O terminal is in the output state. Do not apply an input signal with opposite phase to the output.
* 4. When the "Low" transition of $\overline{CS}$ occurs simultaneously with the "Low" transition of $\overline{WE}$ or after the $\overline{WE}$ transition, output is kept at high impedance.
* 5. $\overline{OE}$ is always "Low."
* 6. Dout is in the same phase as data to be written in this write cycle.
* 7. Dout is the data to be read for the next address.
* 8. During this period, the I/O terminal goes to the output state when $\overline{CS}$ is "Low." At this point, do not apply an input signal with opposite phase to the output.

RTC-64611/64613

■Register

1. Register table

	A_3	A_2	A_1	A_0	b_7 (I/O_8)	b_6 (I/O_7)	b_5 (I/O_6)	b_4 (I/O_5)	b_3 (I/O_4)	b_2 (I/O_3)	b_1 (I/O_2)	b_0 (I/O_1)	Register name
0	0	0	0	0	*	1Hz	2Hz	4Hz	8Hz	16Hz	32Hz	64Hz	64Hz Counter
1	0	0	0	1	*	$c\text{-}s_{40}$	$c\text{-}s_{20}$	$c\text{-}s_{10}$	$c\text{-}s_8$	$c\text{-}s_4$	$c\text{-}s_2$	$c\text{-}s_1$	Second digit counter
2	0	0	1	0	*	$c\text{-}mi_{40}$	$c\text{-}mi_{20}$	$c\text{-}mi_{10}$	$c\text{-}mi_8$	$c\text{-}mi_4$	$c\text{-}mi_2$	$c\text{-}mi_1$	Minute digit counter
3	0	0	1	1	*	*	$c\text{-}h_{20}$	$c\text{-}h_{10}$	$c\text{-}h_8$	$c\text{-}h_4$	$c\text{-}h_2$	$c\text{-}h_1$	Hour digit counter
4	0	1	0	0	*	*	*	*	*	$c\text{-}w_4$	$c\text{-}w_2$	$c\text{-}w_1$	Day of week digit counter
5	0	1	0	1	*	*	$c\text{-}d_{20}$	$c\text{-}d_{10}$	$c\text{-}d_8$	$c\text{-}d_4$	$c\text{-}d_2$	$c\text{-}d_1$	Day digit counter
6	0	1	1	0	*	*	*	$c\text{-}mo_{10}$	$c\text{-}mo_8$	$c\text{-}mo_4$	$c\text{-}mo_2$	$c\text{-}mo_1$	Month digit counter
7	0	1	1	1	$c\text{-}y_{80}$	$c\text{-}y_{40}$	$c\text{-}y_{20}$	$c\text{-}y_{10}$	$c\text{-}y_8$	$c\text{-}y_4$	$c\text{-}y_2$	$c\text{-}y_1$	Year digit counter
8	1	0	0	0	ENB	1Hz	2Hz	4Hz	8Hz	16Hz	32Hz	64Hz	64Hz alarm
9	1	0	0	1	ENB	$a\text{-}s_{40}$	$a\text{-}s_{20}$	$a\text{-}s_{10}$	$a\text{-}s_8$	$a\text{-}s_4$	$a\text{-}s_2$	$a\text{-}s_1$	Second digit alarm
A	1	0	1	0	ENB	$a\text{-}mi_{40}$	$a\text{-}mi_{20}$	$a\text{-}mi_{10}$	$a\text{-}mi_8$	$a\text{-}mi_4$	$a\text{-}mi_2$	$a\text{-}mi_1$	Minute digit alarm
B	1	0	1	1	ENB	*	$a\text{-}h_{20}$	$a\text{-}h_{10}$	$a\text{-}h_8$	$a\text{-}h_4$	$a\text{-}h_2$	$a\text{-}h_1$	Hour digit alarm
C	1	1	0	0	ENB	*	*	*	*	$a\text{-}w_4$	$a\text{-}w_2$	$a\text{-}w_1$	Day of week digit alarm
D	1	1	0	1	ENB	*	$a\text{-}d_{20}$	$a\text{-}d_{10}$	$a\text{-}d_8$	$a\text{-}d_4$	$a\text{-}d_2$	$a\text{-}d_1$	Day digit alarm
E	1	1	1	0	CF	*	*	CIE	AIE	*	*	AF	Control register A
F	1	1	1	1	RAM7	RAM6	RAM5	RAM4	TEST	30sec ADJ	RESET	S•START /$\overline{\text{STOP}}$	Control register B

2. Note the following:

(1) In positive logic, "H" of the data bus corresponds to "1" in the register.

(2) Do not set date out of the clock, otherwise, a counting error may occur.

(3) When the power is turned on (before initializing) the state of the bits is undefined. Write the registers to set the values.

3. Function of the register bits

Bit name	Functions
* Mark	Not used and invalid for write. In the read mode, data equals "0".
64Hz counter	Read-dedicated bit (inavlid for write). Date is read in binary code.
64Hz alarm	Data appears in binary code.
Second digit-year digit	BCD code
Ten o'clock digit	Only for the 24-hour system.
Day of week digit	Encode the days of the week. Example: Data 0 1 2 3 4 5 6 / Day of week Sunday Monday Tuesday Wednesday Thursday Friday Saturday
CF (Carry Flag)	Mainly used to read the time. This bit is set to "1" in any of the following conditions: ① A carry of the second digit has occurred. ② A 64Hz carry and 64Hz register read overlap. In any condition other than the aboves, the bit can be cleared by writing CF = 0.
CIE (Carry Interrupt Enable)	When this bit is set to "1", CF bit = 1 and $\overline{\text{IRQ}}$ terminal = L when the carry conditions are met. When CF = 0 is written, $\overline{\text{IRQ}}$ terminal = OPEN (cleared). When this bit is set to "0", $\overline{\text{IRQ}}$ terminal remains open regardless of the value of the CF bit.
AIE (Alarm Interrupt Enable)	When this bit is set to "1", AF bit = 1 and $\overline{\text{IRQ}}$ terminal = L when the alarm conditions are met. When AF = 0 is written, $\overline{\text{IRQ}}$ terminal = OPEN (cleared). When this bit is set to "0", $\overline{\text{IRQ}}$ terminal remains open regardless of the value of the CF bit.
AF (Alarm Flag)	When the time and calendar match the set alarm time, this bit is set to "1". In any other condition, this bit can be cleared by writing AF = 0.
RAM7 to 4	May be used as RAM or flag.
TEST	This bit is used by us to test the system. The user must set this bit to 0 (TEST = 0).
ADJ	In ADJ = 1, a 30-second correction is executed. Simultaneously, the dividing circuit is reset.
RESET	In RESET = 1, the dividing circuit (less than 1 second counter) is reset.
S•START/$\overline{\text{STOP}}$	This bit is used in combination with H•START/$\overline{\text{STOP}}$ terminal. Only when H•START/$\overline{\text{STOP}}$ terminal = L and S•START/$\overline{\text{STOP}}$ bit = 0, counting stops. Otherwise, the time control counting by using the S•START/$\overline{\text{STOP}}$ bit, connect the H•START/$\overline{\text{STOP}}$ terminal to GND ("L").

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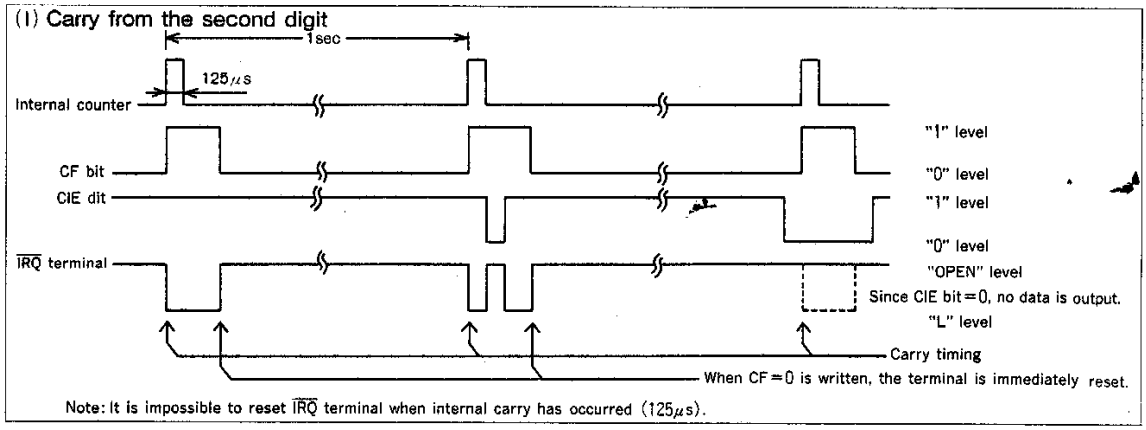
4. Setting the carry interrupt mode

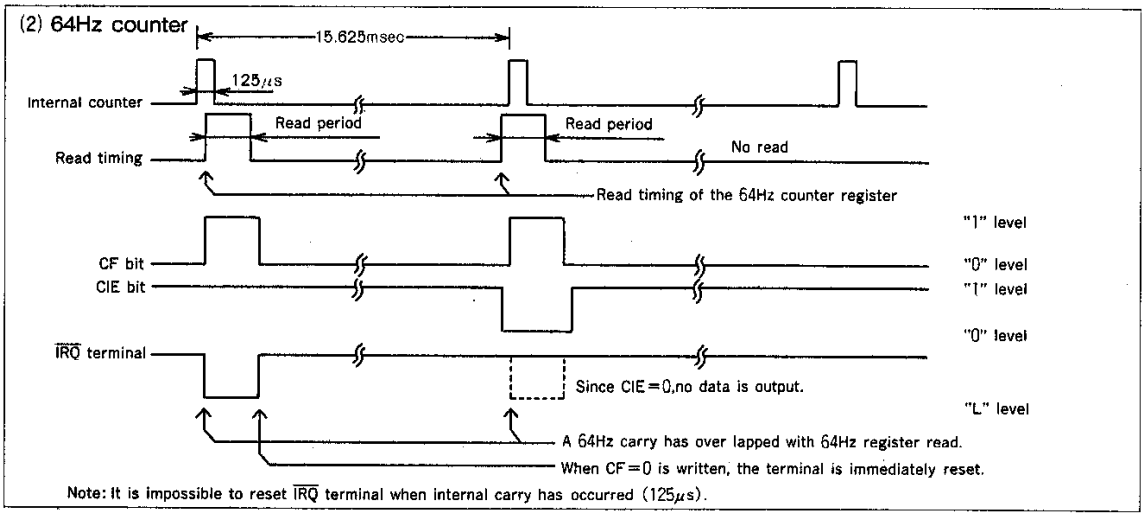
CIE (Carry Interrupt Enable)	Condition	CF (Carry Flag)	$\overline{IRQ}$ terminal
1	A carry has occurred from the second digit, or a 64 Hz carry and a 64Hz register read overlap.	0→1 (The flag is set)	OPEN→L
0			OPEN (Remains)
1	No carry has occurred from the second digit, or a 64 Hz carry and a 64Hz register read do not overlap.	AF=0 is written. (The flag is reset)	L→OPEN
0			OPEN (Unchanged)

5. Setting the alarm interrupt mode.

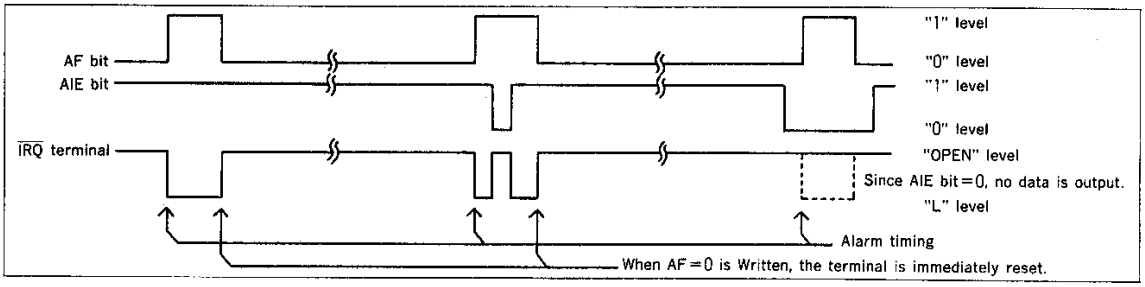
AIE (Carry Interrupt Enable)	Condition	AF (Alarm Flag)	$\overline{IRQ}$ terminal
1	The set alarm time matches the time and calendar.	0→1 (The flag is set)	OPEN→L
0			OPEN (Unchanged)
1	The set alarm time does not match the time and calendar.	AF=0 is written. (The flag is rset)	L→OPEN
0			OPEN (Unchanged)

6. Setting the carry interrupt mode and its reset timing





7. Setting the alarm interrupt mode and its reset timing



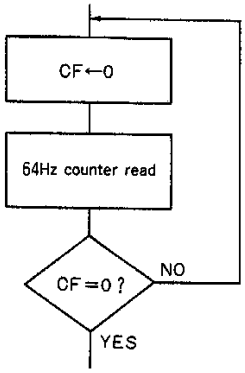
■ Register explanation

1. 64Hz counter

(1) The 64Hz counter can read a value of 64 - 1 Hz (data in binary code) of the dividing circuit (read only).

(2) When a carry from the 128 Hz stage (internal counter) and read of this register are overlapped, CF (b7 of the control register A) is set to "1" In this case, read this register again according to the procedure shown in the flowchart below. (A carry takes place once every approximately 8 ms in the 125 μs period.)

(3) This register is reset using RESET or 30-second ADJ.



2. Second - year counters

(1) These registers set and count the time and calendar.

(2) Each register is in BCD code.
Example: (*,S_{40},S_{20},S_{10},S_8,S_4,S_2,S_1)=(0,1,0,1,1,0,0,1)→59 seconds

(3) Encode the days of the week for use.

Example:

data	0	1	2	3	4	5	6
Day of week	Sun.	Mon.	Tue.	Wed.	Thur.	Fri.	Sat.

(4) The time register uses the 24-hour system. The year register uses the western calendar. Leap years are automatically recognized. (Note: A year whose lower two digits are a multiple of four is recognized as a leap year.)

(5) A carry is generated once each second in the 125 μs period.
Data read during a carry operation (during CF=1) is not guaranteed. (See the time read procedure on page 14.)

(6) The second and minute registers are not affected by RESET.

(7) The hour - year registers are not affected by ADJ and RESET.

3. 64Hz and second - year alarm registers

(1) These registers set the alarm time (the data code is 64Hz; see section "second - year registers).

(2) When the alarm register with its ENB set to "1" matches the counter,AF is set to "1"
When CIE bit (control register A-b3) has been set to "1",$\overline{IRQ}$ terminal is set to "Low "level.

4. Control register A

b_7	b_6	b_5	b_4	b_3	b_2	b_1	b_0
CF	*	*	CIE	AIE	*	*	AF

① This register processes flags which come in ansynchronously from the clock circuit.

② Note the following:
Do not use the Set Bit and Clear Bit instructions to "read-modify-write" because a flag may be set after read.

(1) CF (Carry Flag) (b_7)

① Flag occurrence
This bit is set to "1"in hardware when one of the following conditions is met:
* When a carry from the second digit has occurred.
* When a 64Hz carry overlaps with read access to the 64Hz register (see section "64Hz register/counter).

Carry flag	Function
0	After this bit is reset to "0",there was no read at the time of the second digit carry and the 64Hz carry
1	After this bit is reset to "0",there was a read at the time of the second digit carry or the 64Hz carry

② Resetting
Resetting can be accomplished by writing "0"to the CF bit during any period except the carry period.

③ Note the following:
This bit will not accept a write of "1."

(1) CIE (Carry Interrupt Enable) (b_4)

① When this bit is set to "1", the CF is set when the carry condition is met, and the $\overline{IRQ}$ terminal goes "low".
When CF is reset the $\overline{IRQ}$ terminal returns to the "High"level.

② Relation between CIE/CF bits and $\overline{IRQ}$ terminal.

CIE	CF	$\overline{IRQ}$ terminal *	Remarks
1	0→1 (The flag is set)	High→Low	When the flag is set, $\overline{IRQ}$ terminal goes "Low". When the flag is reset, $\overline{IRQ}$ terminal is also reset.
1	1→0 (The flag is reset)	Low→High	
0	0 or 1	High (No changes)	

* $\overline{IRQ}$ terminal has an open drain output. Therefore, it must be forced up.

(3) AIE (Alarm Interrupt Enable) (b_3).

① When this bit is set to "1", the AF is set when the alarm condition is met and the $\overline{IRQ}$ terminal goes "Low". When the AF is reset, the $\overline{IRQ}$ terminal returns to the "High" level.

② Relation between the AIE/AF bits and the $\overline{IRQ}$ terminal.

AIE	AF	$\overline{IRQ}$ terminal	Remarks
1	0→1 (The flag is set)	Hight→Low	When the flag is set, $\overline{IRQ}$ terminal goes "Low". When the flag is reset, $\overline{IRQ}$ terminal is also reset.
1	1→0 (The flag is reset)	Low→High	
0	0 or 1	High (No changes)	

(4) AF (Alarm Flag) (b_0).

① Flag occurrence

This bit set to "1" in hardware when one of the following condition is met: When the set time of the alarm register (only the register with ENB="1") matches the time and calendar of the counter register.

AF	Function
0	After the bit is reset to "0", the alarm register does not match the clock and counter.
1	The alarm register matches the clock and counter (only for the register with ENB set).

② Resetting

Reset can be conducted by writing "0" to the AF bit during any period except the alarm time.

③ Note the following:

This bit will not accept write of "1".

5. Control register B

b_7	b_6	b_5	b_4	b_3	b_2	b_1	b_0
RAM_7	RAM_6	RAM_5	RAM_4	TEST	ADJ	Reset	S·START /STOP

Note: User functions in the state TEST="1" are not guaranteed. Use the system in the state TEST="0".

(1) RAM 7, 6, 5, 4 ($b_{7,\ 6,\ 5,\ 4}$).

The bit can be used as RAM or flags by writting "1" or "0".

They cannot be used as RAM if TEST="1".

(2) TEST (b_3)

This bit is used by us to test the system. Use the system with TEST set to "0".

If TEST="1", user functions are not guaranteed.

(3) 30-second ADJ (30-second ADJUST) (b_2)

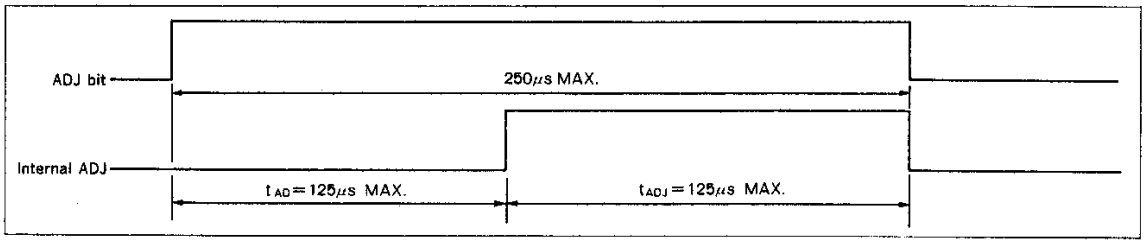
① When this bit is set to "1", the 30-second correction is executed. At this time, 64Hz counter (dividing circuit) is also reset.

* Before 30 seconds, this bit has "00" seconds without a carry of the minute digit.

* After 30 seconds, this bit has "00" second with a carry of the minute digit.

② Reset

"1" is held for 250 μs after this bit is set to "1". This bit then automatically returns to "0".

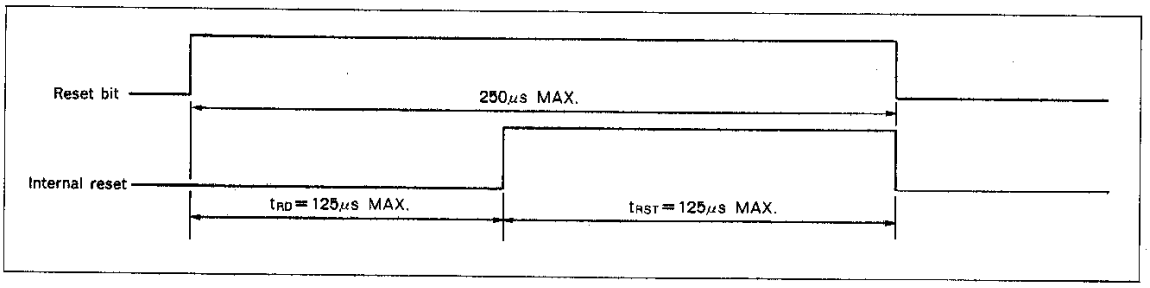


③ Note the following:
Conduct the next writing, only after this bit returns to"0" (is reset),
Writing"0" to this bit is invalid.

(4) RESET (b1)

① When this bit is set to"1", only the dividing circuit is initialized.

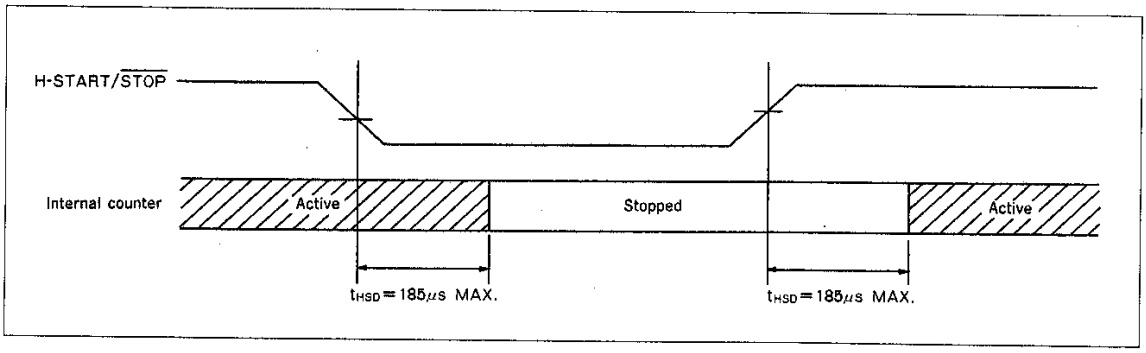
② Reset
"1" is held for 250μs after this bit is set to"1". The bit then automatically returns to"0".



③ Note the following:
Conduct the next writing, only after this bit returns to"0" (is reset),
Writing"0" to this bit is invalid.

(5) S·START/$\overline{\text{STOP}}$ (Software START/$\overline{\text{STOP}}$) (b_0).
Use this function in combination with the H.START/$\overline{\text{STOP}}$ terminal.

H·START/$\overline{\text{STOP}}$ terminal	H·START/$\overline{\text{STOP}}$ bit	Clock state
L	0	Stopped
L	1	Active
H	0	Active
H	1	Active



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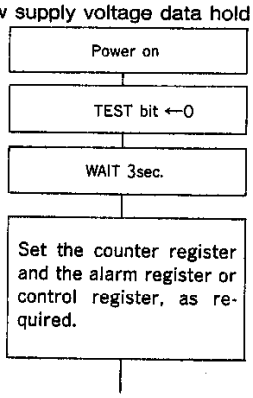
■ Operation procedure

1. Initialization when power on.

Initialization is needed only when the power is initially turned on. To return from battery backup mode, follow the specifications for low supply voltage data hold wave form.



When the power is turned on, all registers and $\overline{IRQ}$ output are undefined.

To assure operation (Write "0" every time).

Time necessary for oscillation stability.

Note: This module has no terminal for resetting registers.
Therefore, after the power is turned on, all registers must reinitialized. Before initialization of the registers is completed, follow the instructions below:

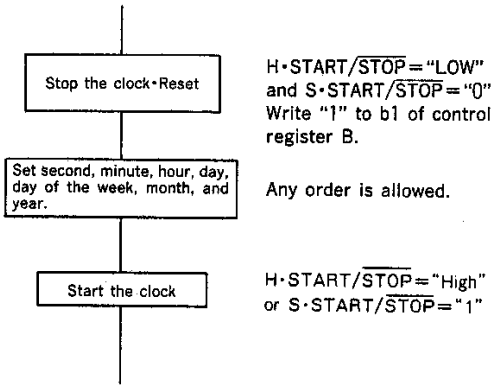
(1) Undefined $\overline{IRQ}$
As all registers are undefined when the power is turn on, the interruption from a carry or alarm may occur.
This may cause an interrupt from a carry or may cause an alarm to occur. In the system software,to prevent such error, do not accept any interrupts before all registers are completely initialized.

(2) Undefined calender clock operation
When the power is turned on, the TEST bit is undefined. With this bit="1" the system operates in test mode, then begins normal operation. Set this to"0" before using the clock function.

(3) Undefined countar START/$\overline{STOP}$
When the power is turned on, the S.START/$\overline{STOP}$ bit is undefined.
Starting and stopping of the counter is controlled by the OR logic of this bit and the external terminal H.START/$\overline{STOP}$.
Set this bit in accordance with the control method.

2. Time setting procedure

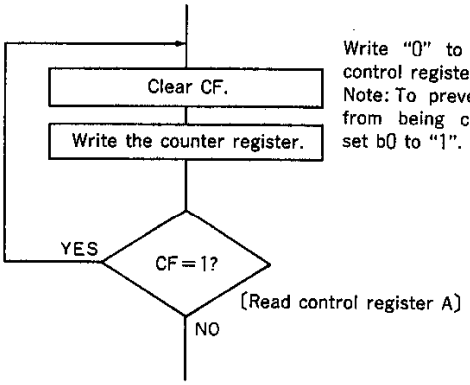
(1) To reset the dividing circuit and then set the counter (2) To set the second - year counter



H•START/$\overline{STOP}$="LOW" and S•START/$\overline{STOP}$="0" Write "1" to b1 of control register B.

Any order is allowed.

H•START/$\overline{STOP}$="High" or S•START/$\overline{STOP}$="1"



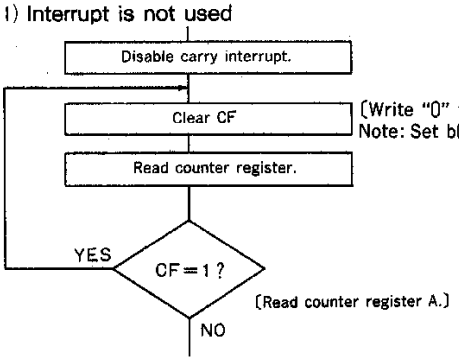
Write "0" to b7 of control register A.
Note: To prevent AF from being cleared, set b0 to "1".

(Read control register A)

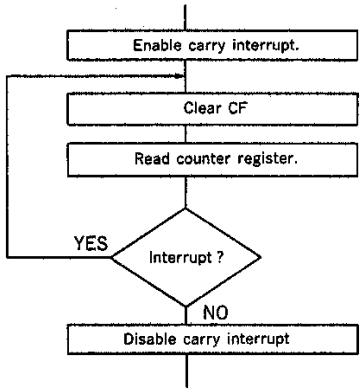
Section (1) indicates the method of stopping the clock and setting the time. This method is effective when the entire calendar clock is exchanged. With this method, programming is easy.
Section (2) indicates the method for setting the time while keeping the clock operating. The method is effective when a part of the calendar clock is exchanged (for example, only data on the second or time is exchanged). The carry flag is used to check the write state. When a carry is generated during write, the written data is automatically updated and an error occurs in the set data. Therefore, when the carry flag has been set to"1", rewriting must be done.
The interrupt function can be used to check the carry flag.
Note: A carry of second to year digits is executed once per second in the 125μs period, Therefore, when a carry is detected in write operation, the writing can be done after 125μs from the carry starts. The write must be completed before the next carry starts.

3. Time reading procedure

(1) Interrupt is not used



(2) Interrupt is used.

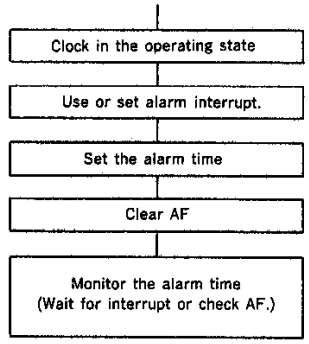


When a carry occurs during time read, the correct time is unavailabl. In this case, the read must be repeated. The method in (1) does not use an interrupt. The method in (2) uses an interrupt ($\overline{IRQ}$ terminal). To simplify the program, the method in (1) is generally used.

Note: 1). The second - year digit carry is executed once per second during the 125μs period. When a carry is detected in the read operation, the reading can be done after 125μs from carrystart. Now a normal read is achieved. The read must be completed before the new carry starts.

2). The 64Hz counter is carried once each approximately 8 msec, in the 125μs period

4. Alarm function



To use interrupt, the AIE bit
(b3 of the control register A) must be "1".

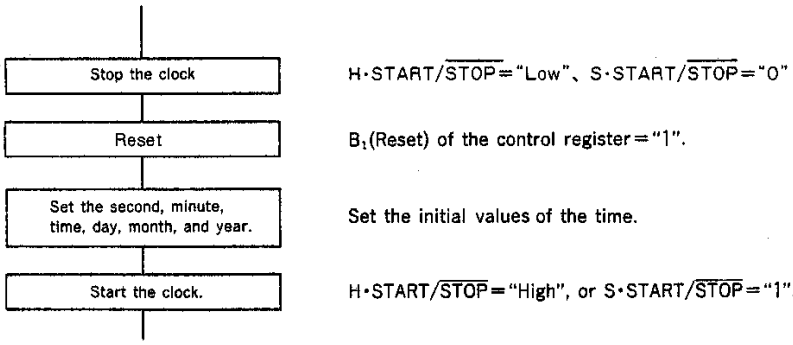
The must be reset, considering that the flag was set during the alarm time setting operation (Clear AF by writing "0" to b0 of control register A.)
Note: Set CF to "1" not to be cleared.

The alarm can be generated for any of the 64Hz, second, minute, hour, day of the week, or in any combination of them. For the register to which you want to generate alarm, write "1" to ENB bit of b7 and set the alarm time in the low-order bits. For other registers, write"0" to ENB bit of b7.

When the clock matches the alarm time, the AF bit (b0 of the control register A) is set to"1". Alarm detection may be recognized byreading this bit, however, an interrupt is commonly used. When AIF (b3 of the control register A) has been set to"1", the $\overline{IRQ}$ terminal goes"Low" when an alarm occurs. Thus, an alarm can be detected.

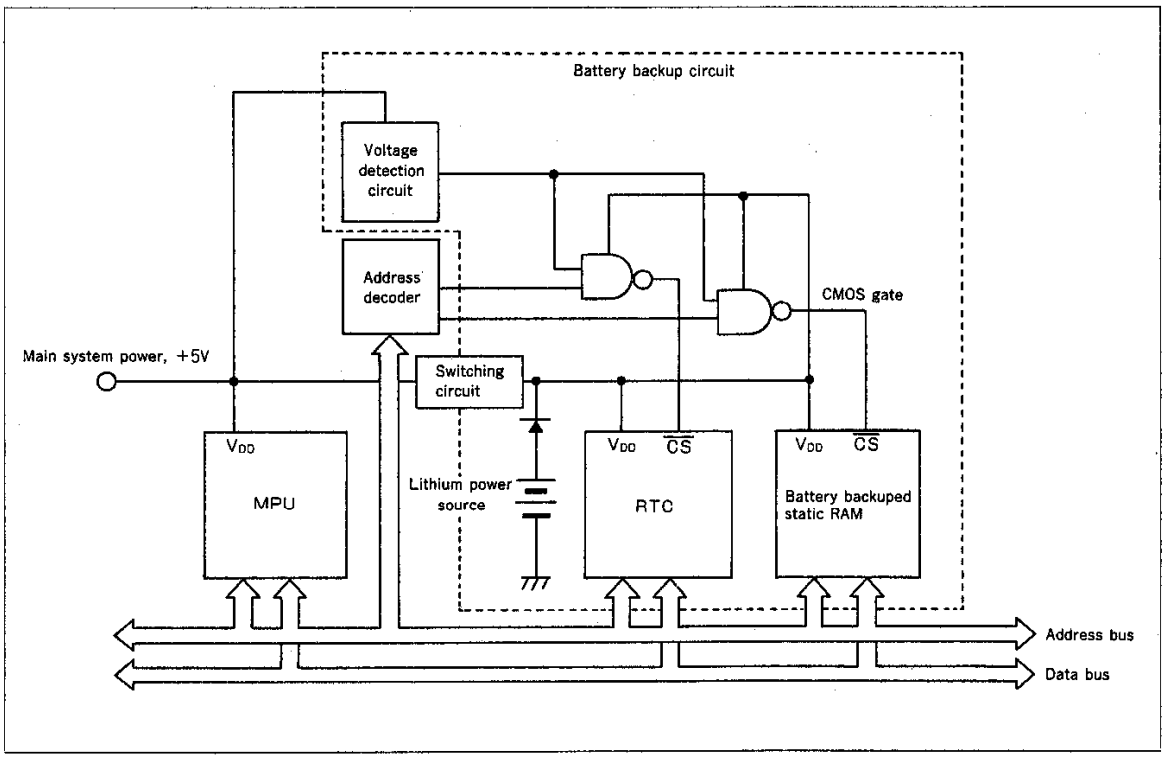
AF is always set when time register and alarm register match. That is, when the AF bit is reset by writing "0", AF is immediately set again after write. The programmer must be aware of this point.

5. Application as a long term timer



This module contains the counter start/stop function. This function enables the module to be used as a long-term timer. In this application, the timer uses the normal calendar clock function.
This requires setting of the month and year, even if they are not required. For example, When the timer is used with the month setting undefined, the month may end on any day from 28th to 31st. The timer will not indicate when the next month starts.

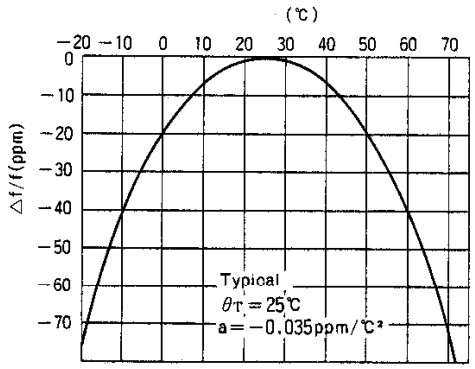
■ System configuration sample



RTC-64611/64613

■ Reference data

(1) Example of frequency /temperature characteristics



How to determine frequency stability (clock error)

① The frequency temperature characteristics can be approximated by the expression below :

$$\triangle f_T\ (ppm) = a\ (\theta_T - \theta_X)^2$$

$\triangle f_T$(ppm)	: Frequency deviation at any temperature
a(ppm/℃²)	: Secondary temperature coefficient (−0.035±0.005ppm/℃²)
θ_T(℃)	: Peak temperature (25℃ ±5℃)
θ_X(℃)	: Any temperature

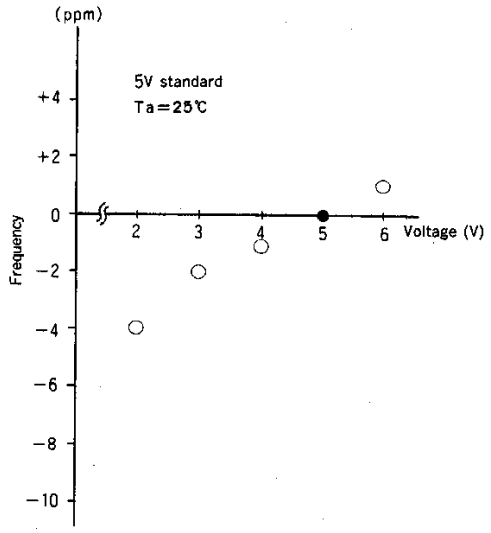
② To determine the clock error (accuracy), add the frequency tolerances and voltage characteristic to the above.

$$\triangle f/f\ (ppm) = \triangle f/f_0 + \triangle f/f_T + \triangle f_V$$

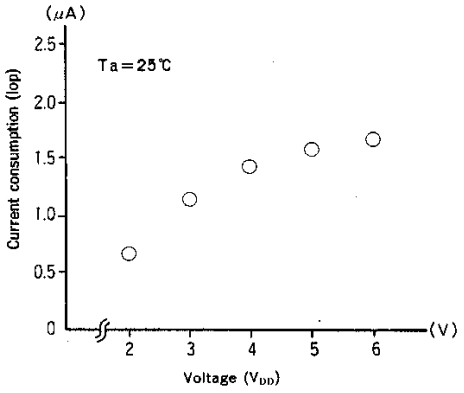
△f/f(ppm)	: Clock accuracy (frequency stability) at any temperature and voltage
$\triangle f/f_0$(ppm)	: Frequency tolerances
$\triangle f_T$(ppm)	: Frequency deviation at any temperature
$\triangle f_V$(ppm)	: Frequency deviation at any voltage

③ How to determine the day difference (second/day).
Daily difference (second) = $\triangle f/f \times 10^{-6} \times 86,400$ (second).
The daily difference is approximately one second per day, at △f/f is 11.574ppm.

(2) Example of the frequency/voltage characteristics



(3) Example of the current consumption/ voltage characterisitcs



Note: The data shows the typical values of a sample lot.
For the rated values, see the specifications (P3-4)

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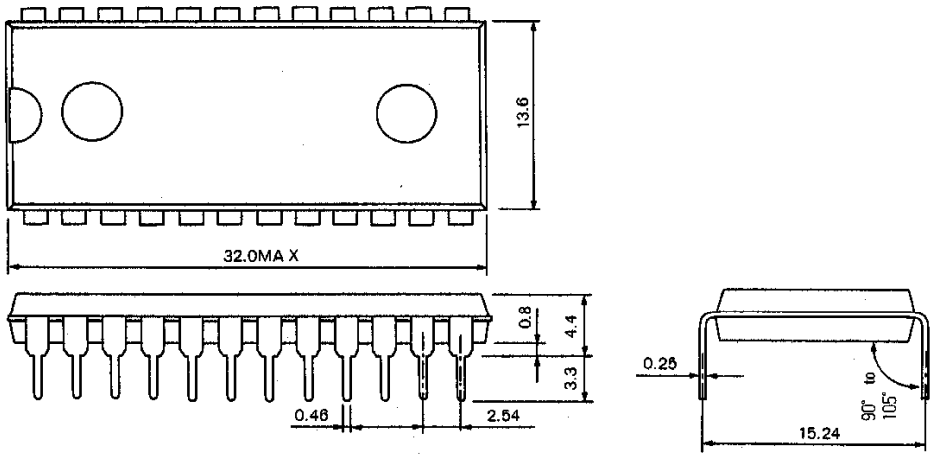
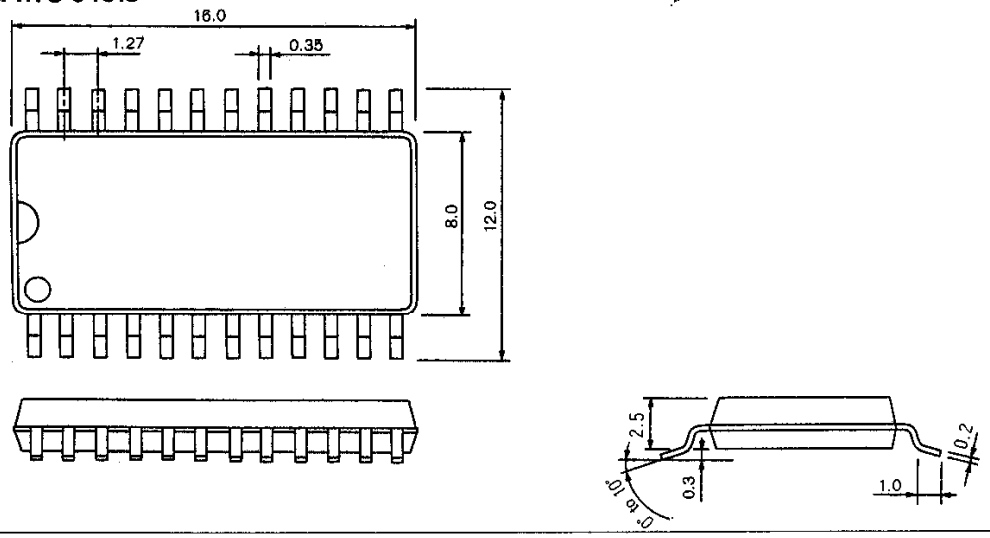
■ Package size

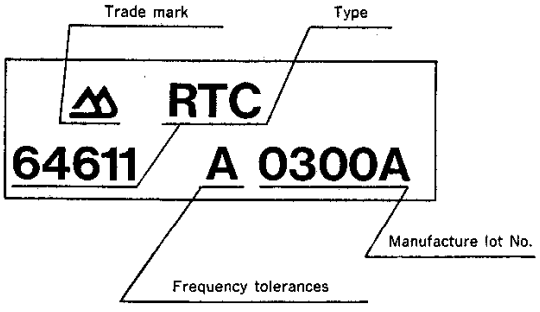
1. RTC-64611



2. RTC-64613



■ Marking layout



Indication and frequency tolerances

Type	Indication	Tolerances
RTC-64611	A	5±10ppm
	B	5±50ppm
RTC-64613	A	5±20ppm
	Not indicated	5±50ppm

Note: The indication above details the markings and outline their positions.
But does not specify the details of the type faces and sizes of characters and their positions.

■ Precautions

(1) This module uses a C-MOS IC for low power consumption. This following precautions must be taken to ensure that it is not damaged.

① Static electricity

This unit have circuits to protect it from damage caused by static electricity, but exposure to excessive static electricity could damage the IC. Please use conductive packaging or shipping containers. Also, please use grounded soldering irons, measuring circuits, etc. that do not leak.

② Noise

Exposing the power source or input/output terminals to excessive noise could cause malfunctioning or a latch up phenomenon. To ensure stable operation, please attach a by pass capacitor (recommend ceramic type) of at least 0.1 μF as close as possible to the module's power-source terminal (between V_{DD}-GND). Please do not place the module near anything that emits high nois.

③ Voltage level of input terminals

Please make the input terminal voltage level setting as close to the V_{DD}-GND potential as possible, since a mid-level potential setting will cause an increase in current consumption, a decrease in the noise margin, and a deterioration of devices.

④ Unused input terminals (with exception of (NC) terminal)

Because the input impedance of input terminals is extremely high, use in the open state may cause malfunctioning due to unset potential or noise. Therefore, unused input terminals should be either pulled up or down. Further, the NC terminal should be grounded in order to avoid noise.

(2) Packaging precautions

① Soldering temperature conditions

I. RTC-64611

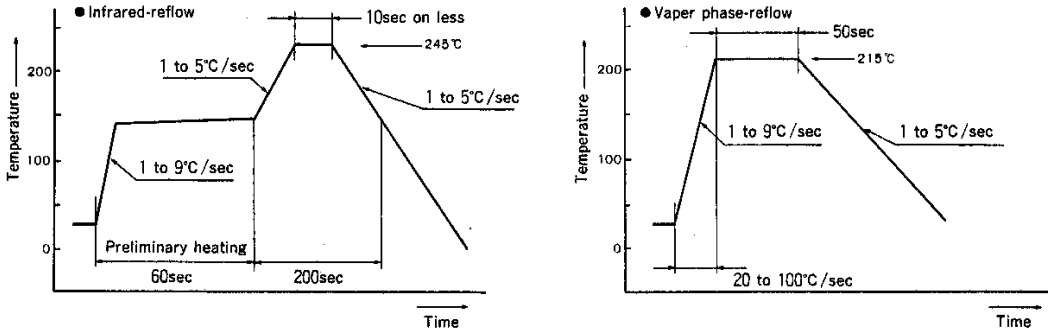
Since solder is used on the quartz oscillator, if the temperature inside the package exceeds 150°C, the quartz could deteriorate or be damaged. (Solder conditions: 260℃ or less × 10 seconds or less (lead portion)). Either use a solder dip tank or solder by hand. Please refrain from using paper, reflow, infrared, etc.

II. RTC-64613

Be certain to check the mounting temperature before mounting the unit, as the quartz oscillator could deteriorate and be damaged if the temperature inside the package exceeds 260℃. Also, please check the packaging temperature before using RTC-64613 when conditions change.

(Solder conditions: 260°C or less × 10 seconds or less × 2 times or fewer, or 230°C or less × 3 minutes or less)

Soldering conditions for SMD products



(The rate of the rise in resin temperature should be as gradual as possible)

② Mounting machine

It is possible to use an all-purpose mounting machine, but please be sure to check the machine's suitability at your company before using it, as physical shocks during mounting could lead to damage of the internal quartz crystal. When there is a change in conditions, please use the machine after making the above-mentioned check.

③ Ultrasonic cleaning

Depending on the conditions, ultrasonic cleaning could cause resonance damage to the quartz crystal.
Since we are unable to determine the usage conditions (type of cleaning unit, power, time, conditions inside the bath, etc.) at our company, we cannot guarantee the safety of this unit when it is cleaned in an ultrasound cleaner.

④ Mounting direction

This module will be damaged if it is mounted backwards, so please make sure that it is packaged in the correct position.

⑤ Leak between terminals

Since turning on the unit when it is dirty or covered with condensation could lead to leaks between terminals, please clean and dry the module before turning it on.

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Application Manual for RTC-64611/64613

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The manufacturer has been approved by the Reliability Center for Electronic Components of Japan (RCJ).