NEC
NEC Electronics Inc.

μPD31442
RAB2IT-MEMC Memory Controller
A Component of the RAB2IT Chip Set

Preliminary Information

October 1994

RAB2IT Chip Set

The RISC Architecture Bus-Bridge Interface Technology (RAB2IT) chip set is a high-performance system solution for the RISC 64-bit architecture. The RAB2IT interface between the main memory, external I/O devices, and the VR4000™ family of microprocessors provides scalable performance that meets a variety of requirements. Two highly integrated VLSI components, RAB2IT-IOC and RAB2IT-MEMC, enable users to configure various system architectures from low-cost, low-end systems to high-performance workstations.

Features

- Highly integrated
  - — Secondary cache controller: supports 1M-byte secondary cache
  - — DRAM controller: supports high-speed synchronous DRAM and standard DRAM
  - — Data buffer: integrates data bus driver and parity generation logic
  - — Supports fully i486 CPU compatible interface
- Tightly coupled interface of high-speed VR4400™ (4000)PC/SC microprocessors and low-cost VR4200™ microprocessor
- Flexible system configuration
  - — Low-cost i486™ upgrade system with one RAB2IT-IOC (figure 1)
  - — High-performance VR4400(4000)SC system with both RAB2IT-IOC and -MEMC (figure 2)
  - — High-performance VR4400(4000)PC or VR4200 system with both RAB2IT-IOC and -MEMC to support local secondary cache (figure 3)
- Flexible memory implementation
  - — High-speed DRAM
  - — Synchronous DRAM
- i486 fully compatible local bus interface
- Big endian and little endian support
- 240-pin PQFP package
- 3.3-volt operation with 5-volt capability

System Address Mapping

Refer to figure 4, table 1, and table 2.

RAB2IT has an 8-gigabyte area for 33-bit addresses. In a VR4400/VR4000 (36-bit address) system, a mirror image appears due to the insufficient decoding (only 33-bit addresses are decoded). In the address area, the high-order 4 gigabytes are allocated to the system and the low-order 4 gigabytes are used as the memory area. The area between 0x0 1000 0000 and 0x0 1FFF FFFF can be allocated as an I/O area and internal register area according to the setting of the internal registers.

The addresses of the internal registers and the I/O area are allocated to 0x0 1000 0000 through 0x0 1FFF FFFF and 0x1 1000 0000 through 0x1 1FFF FFFF on reset. The area between 0x0 1000 0000 and 0x0 1FFF FFFF can be allocated to the I/O area by setting the Device Control register.

RAB2IT-MEMC samples the RAO state on reset to allocate the internal register address area if two -MEMCs are operating in parallel.

The area between 0x0 0000 0000 and 0x0 FFFF FFFF has to be set by the user; otherwise, the external agents might use this space later on. When the CPU issues an address in the RAB2IT-IOC I/O area, RAB2IT-IOC puts the low-order 16-bit address to the 486 compatible bus. The high-order 16-bit address is unchanged or 0 according to the mode select.

In a multiple external agents system (RAB2IT-IOC and -MEMC), the SysAD bus arbitration is done by decoding the given address map on each agent.

Figure 1. VR4400SC System With Single RAB2IT-IOC

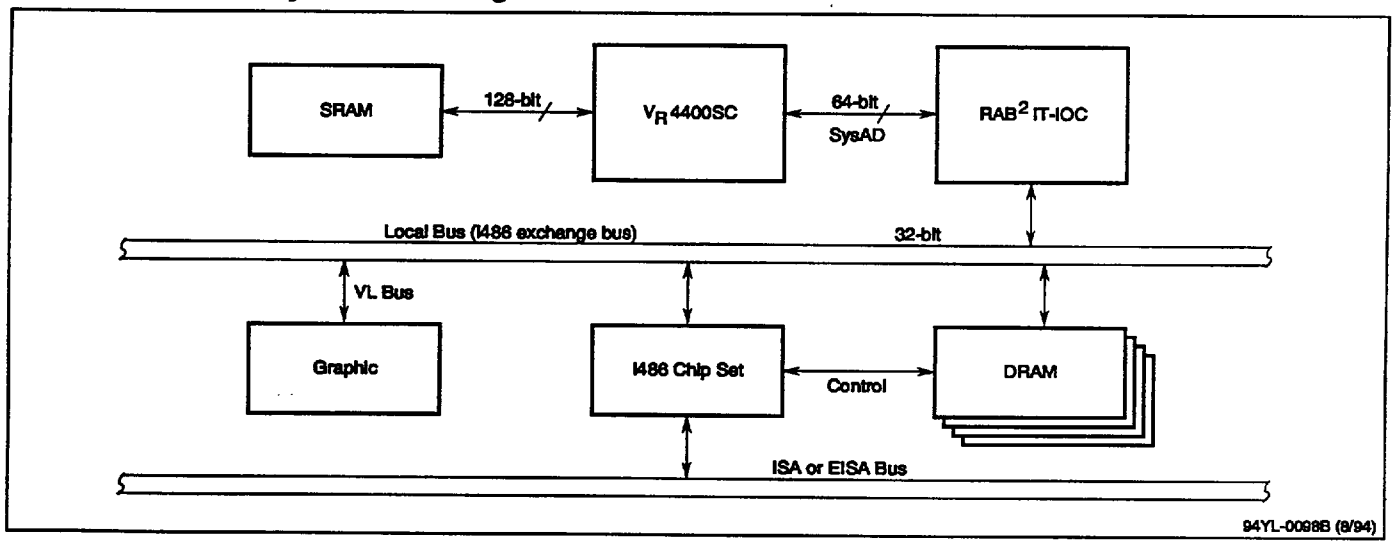


Figure 2. VR4400SC System With RAB2IT-MEMC and RAB2IT-IOC

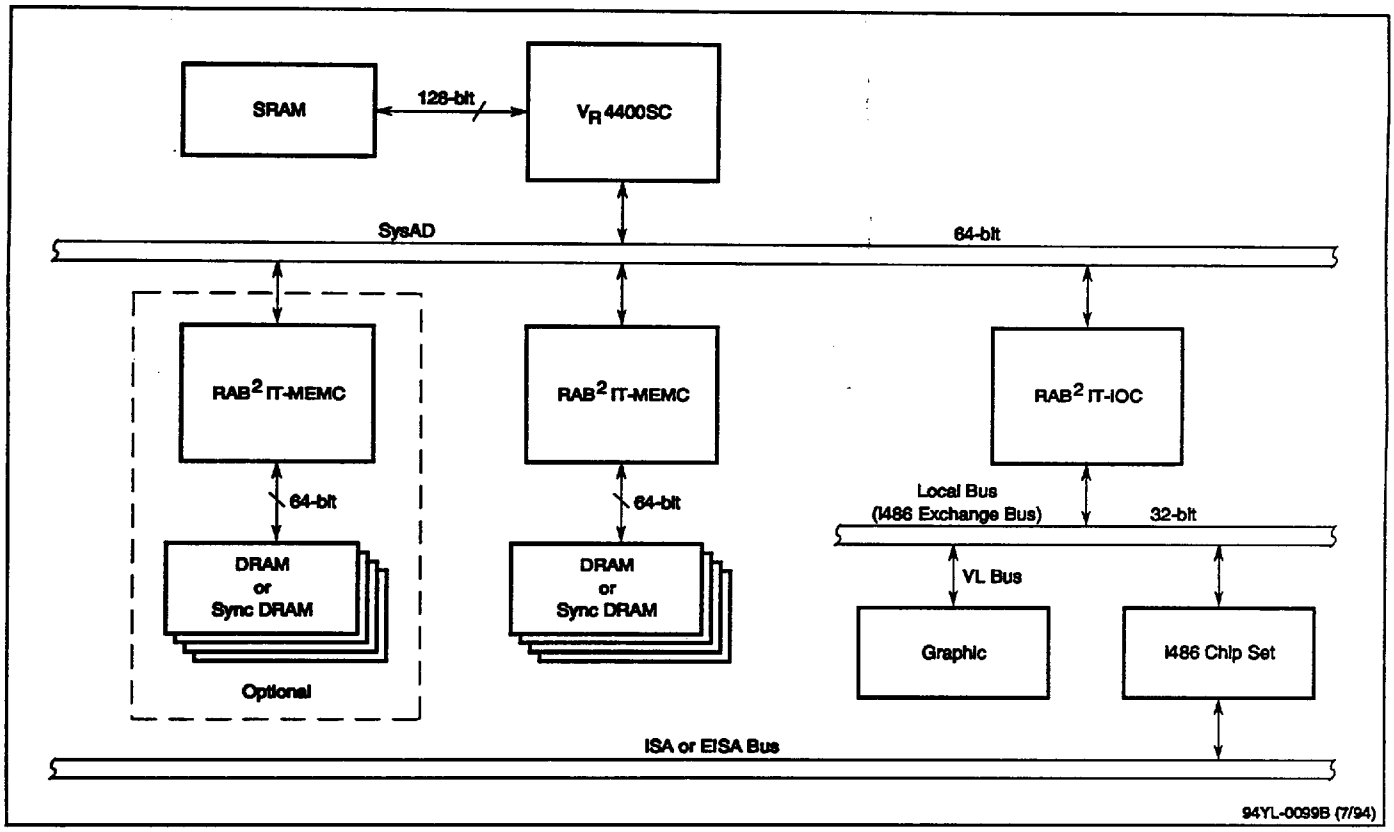


Figure 3. VR4400PC/VR4200 System With RAB2IT-MEMC and RAB2IT-IOC

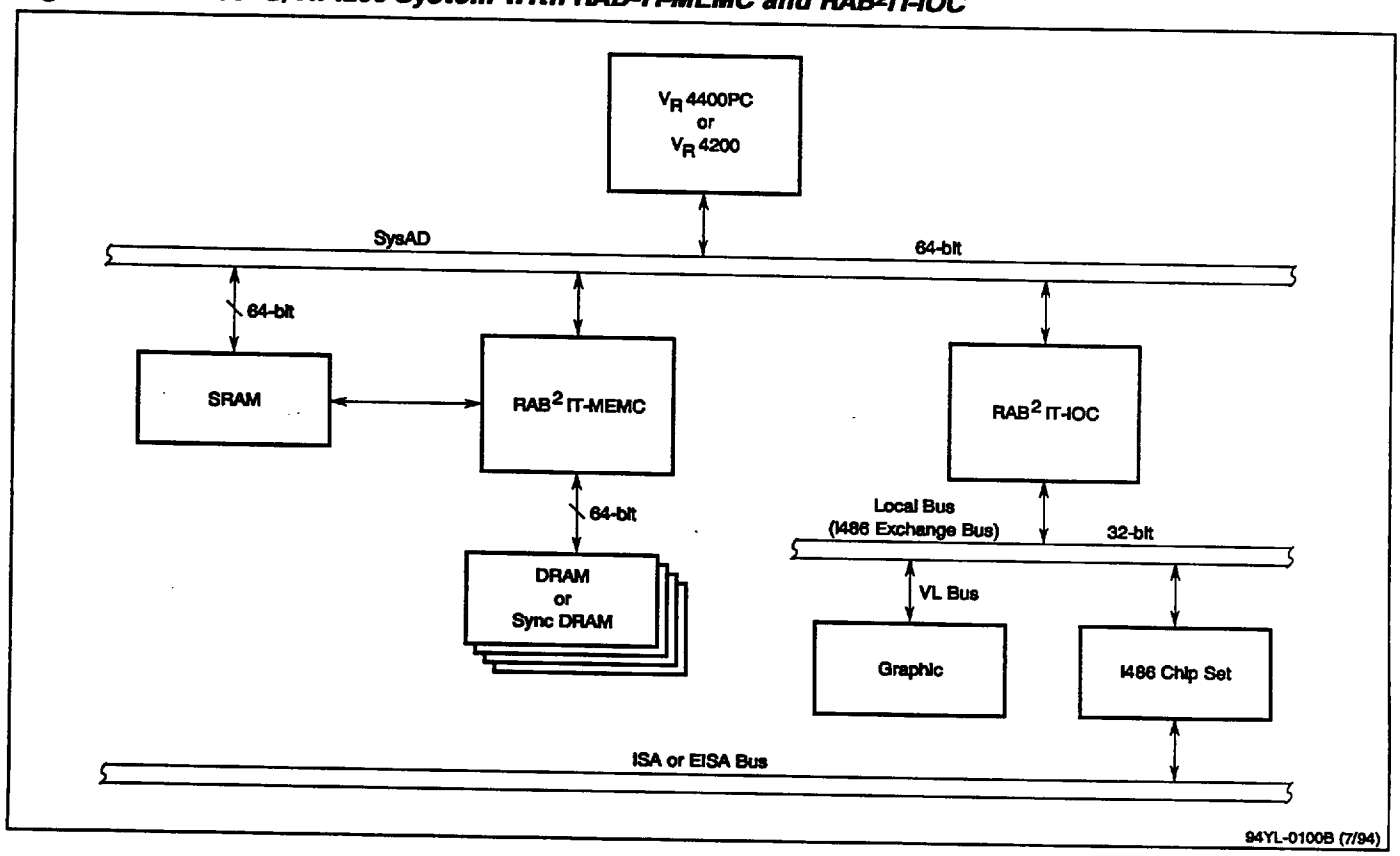


Figure 4. Memory Mapping

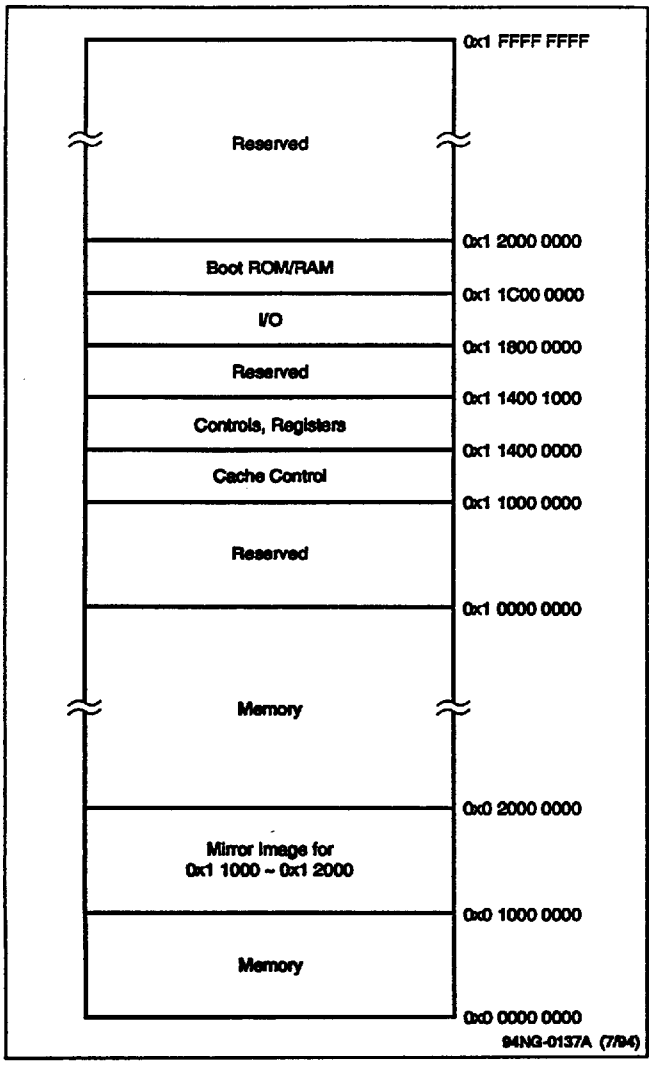


Table 1. Address Map

Addresses on SysAD	Address on 486 Compatible Bus	Name	Bus Master
0x1 1C00 0000 ~ 0x1 1FFF FFFF	AT = 1: 0x1 1C00 0000 ~ 0x1 1FFF FFFF AT = 0: 0x0 000E 0000 ~ 0x0 000F FFFF	Boot ROM/RAM area	RAB²IT-IOC
0x1 1800 0000 ~ 0x1 1BFF FFFF	AT = 1: 0x0 1800 0000 ~ 0x0 1BFF FFFF AT = 0: 0x0 0000 0000 ~ 0x0 0000 FFFF	I/O	RAB²IT-IOC
0x1 1400 1000 ~ 0x1 17FF FFFF	—	Reserved	Not valid for the RAB²IT system.
0x1 1400 0F00 ~ 0x1 1400 0FFF	0x03	Write back cycle	RAB²IT-IOC
0x1 1400 0E00 ~ 0x1 1400 0EFF	0x02	Halt cycle	
0x1 1400 0D00 ~ 0x1 1400 0DFF	0x01	Flush cycle	
0x1 1400 0C00 ~ 0x1 1400 0CFF	0x00 or 0x04 0x00	Interrupt acknowledge Shutdown cycle	
0x1 1400 0400 ~ 0x1 1400 0BFF		Reserved	Not valid for the RAB²IT system.

Table 1. Address Map (cont)

Addresses on SysAD	Address on 486 Compatible Bus	Name	Bus Master
0x1 1400 0300 ~ 0x1 1400 03FF		RAB²IT-MEMC internal register; RAO = high	RAB²IT-MEMC
0x1 1400 0200 ~ 0x1 1400 02FF		RAB²IT-MEMC internal register; RAO = high	RAB²IT-MEMC
0x1 1400 0000 ~ 0x1 1400 01FF		RAB²IT-IOC internal register	RAB²IT-IOC
0x1 1000 0000 ~ 0x1 13FF FFFF	0x00 0000 0000 ~ 0x0 0000 FFFF	Cache control	See table 2
0x1 0000 0000 ~ 0x1 0FFF FFFF		† Reserved	
0x0 2000 0000 ~ 0x1 FFFF FFFF		† Memory	
0x0 1000 0000 ~ 0x0 1FFF FFFF		Mirror image for 0x1 1000 0000 ~ 0x1 1FFF FFFF or memory (depends on register setting)	
0x0 0000 0000 ~ 0x0 0FFF FFFF		† Memory	

† This area will be the memory area on the 486 bus if only RAB²IT-IOC is used in the system. This area will be the memory area based on the setting of the memory base address register in the RAB²IT-MEMC if both -IOC and -MEMC are used in the system.

Table 2. Cache Control Area

Device Control Register Bit 20	SysAD Address	RAO = 0	RAO = 1
RAMAPIO = 0	0x0 1000 0000 ~ 0x0 11FF FFFF 0x1 1000 0000 ~ 0x1 11FF FFFF	Read/Write	Write
	0x0 1200 0000 ~ 0x0 12FF FFFF 0x1 1200 0000 ~ 0x1 12FF FFFF	Read/Write	Tag memory access disabled
	0x0 1300 0000 ~ 0x0 13FF FFFF 0x1 1300 0000 ~ 0x1 13FF FFFF	Tag memory access disabled	Read/Write
RAMAPIO = 1	0x1 1000 0000 ~ 0x1 11FF FFFF	Read/Write	Write
	0x1 1200 0000 ~ 0x1 12FF FFFF	Read/Write	Access disabled
	0x1 1300 0000 ~ 0x1 13FF FFFF	Access disabled	Read/Write

Table 3. Pin Assignments, 240-Pin PQFP

System Address/Data	Pin No.	System Address/ Data/Command	Pin No.	Memory Address/Data	Pin No.	Memory Data	Pin No.
Sys AD0	218	SysAD50	44	MA0	182	MD30	130
1	219	51	45	1	179	31	129
2	220	52	46	2	178	32	128
3	221	53	47	3	177	33	127
4	222	54	50	4	176	34	126
5	223	55	51	5	175	35	125
6	224	56	52	6	174	36	124
7	225	57	53	7	173	37	123
8	226	58	54	8	172	38	122
9	227	59	55	9	171	39	119
SysAD10	230	SysAD60	56	MA10	170	MD40	118
11	231	61	57	11	167	41	117
12	232	62	58			42	116
13	233	63	59			43	115
14	234					44	114
15	235					45	113
16	236					46	112
17	237					47	111
18	238					48	110
19	239					49	107
SysAD20	2	SysADC0	208	MD0	166	MD50	106
21	3	1	209	1	165	51	105
22	4	2	210	2	164	52	104
23	5	3	211	3	163	53	103
24	6	4	212	4	162	54	102
25	7	5	213	5	161	55	101
26	8	6	214	6	160	56	100
27	9	7	215	7	159	57	99
28	10			8	158	58	98
29	11			9	155	59	95
SysAD30	14	SysCmd0	62	MD10	154	MD60	94
31	15	1	63	11	153	61	93
32	16	2	64	12	152	62	92
33	17	3	65	13	151	63	91
34	18	4	66	14	150	64	90
35	19	5	67	15	149	65	89
36	20	6	68	16	148	66	88
37	21	7	69	17	147	67	87
38	22	8	70	18	146	68	86
39	23			19	143	69	83
SysAD40	32			MD20	142	MD70	82
41	33			21	141	71	81
42	34			22	140		
43	35			23	139		
44	38			24	138		
45	39			25	137		
46	40			26	136		
47	41			27	135		
48	42			28	134		
49	43			29	131		

Table 3. Pin Assignments, 240-Pin PQFP (cont)

Clock and Control	Pin No.	V_{DD}	Pin No.	Gnd	Pin No		
BS	197	V_{DD}	12	Gnd	1		
CA3A	202		24		13		
CA3B	203		36		25		
CA4A	206		48		29		
CA4B	207		61		37		
			72		49		
$\overline{CDRD}$	201		84		60		
$\overline{CDWR}$	200		96		73		
CKE/SLVC	194		108		85		
			120		97		
$\overline{CS0/RAS0}$	188	V_{DD}	132	Gnd	109		
$\overline{CS1/RAS1}$	189		144		121		
$\overline{CS2/RAS2}$	190		156		133		
$\overline{CS3/RAS3}$	191		168		145		
			181		157		
DQM0/$\overline{CAS0}$	183		192		169		
DQM1/$\overline{CAS1}$	184		204		180		
DQM2/$\overline{CAS2}$	185		216		187		
DQM3/$\overline{CAS3}$	186		228		193		
			240		199		
$\overline{PERR}$	80			Gnd	205		
$\overline{PwrRdy}$	31				217		
					229		
RA0	30						
$\overline{RClock}$	26						
$\overline{Release}$	74						
$\overline{Reset}$	76						
$\overline{RRelease}$	79						
$\overline{RValidIn}$	77						
$\overline{RValidOut}$	78						
$\overline{SCAS}$	196						
$\overline{SRAS}$	195						
TClock	28						
$\overline{ValidIn}$	71						
$\overline{ValidOut}$	27						
$\overline{WE}$	198						
$\overline{WrRdy}$	75						

RAB2IT-MEMC MEMORY CONTROLLER

The RAB2IT-MEMC provides the high-performance memory interface solution for the VR4000 family of microprocessors. Due to the high integration, the flexible architecture brings the benefit for a variety of the CPUs and system configurations; for example, the internal secondary cache controller will boost the performance of systems with non-secondary cache controller integrated microprocessors: VR4400PC, VR4000PC, and VR4200. The 64-bit local system memory data bus as well as internal read/write buffers increases the data transfer bandwidth. Two of the RAB2IT-MEMC controllers can even be parallel-connected to the SysAD bus to support a 128-bit local DRAM bus.

Features

- DRAM and synchronous DRAM
- Secondary cache interface
- Slave mode DMA data transfer
- Ordering of block read response
- Programmable big endian or little endian configuration
- Addresses setting of the internal registers
- Optional dual devices operation

Figure 5 is the RAB2IT-MEMC block diagram, figure 6 is the package pin configuration drawing, table 3 lists package pin assignments, and table 4 describes pin functions.

Figure 5. RAB2IT-MEMC Block Diagram

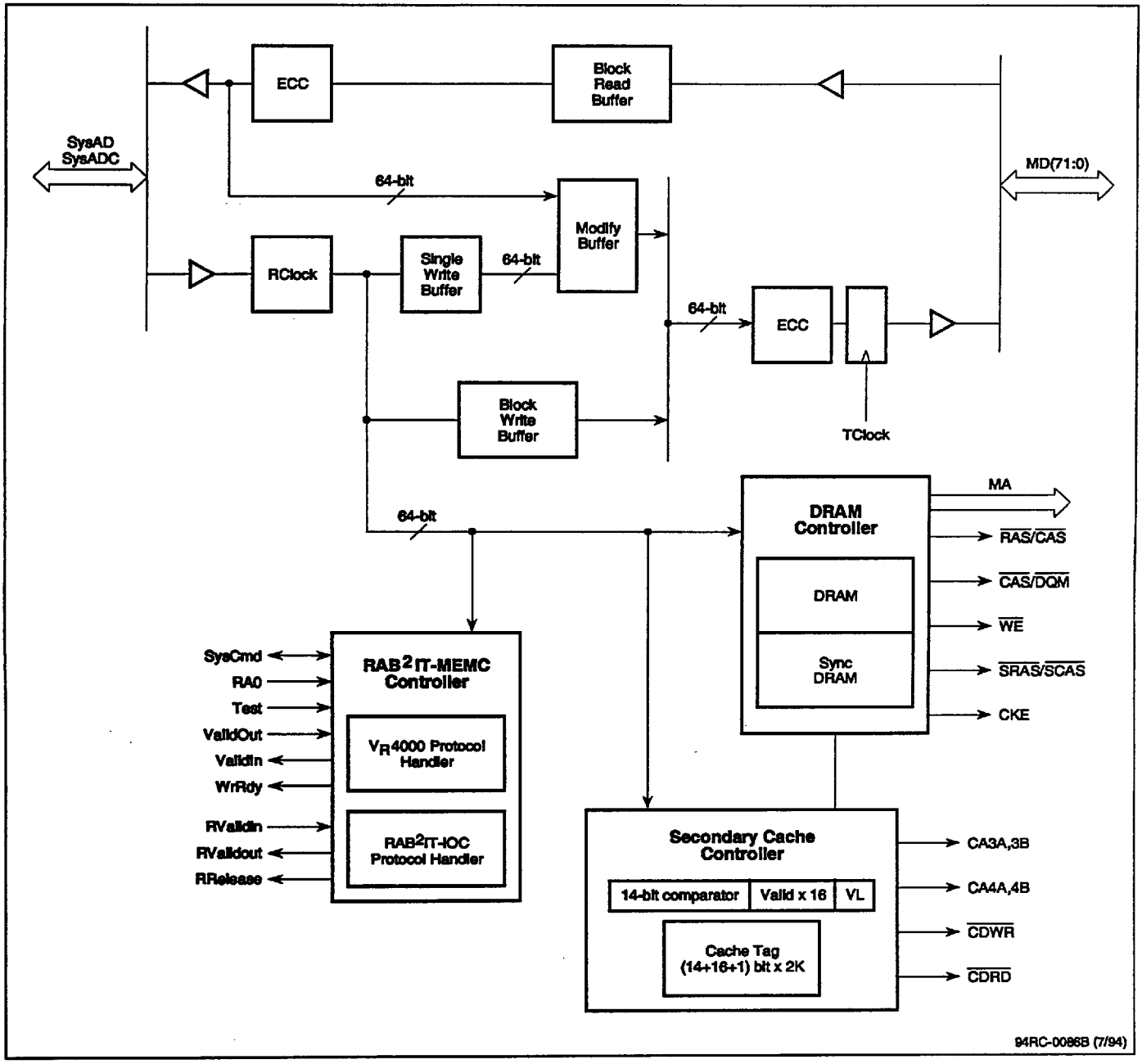


Table 4. Pin Descriptions, 240-Pin PQFP

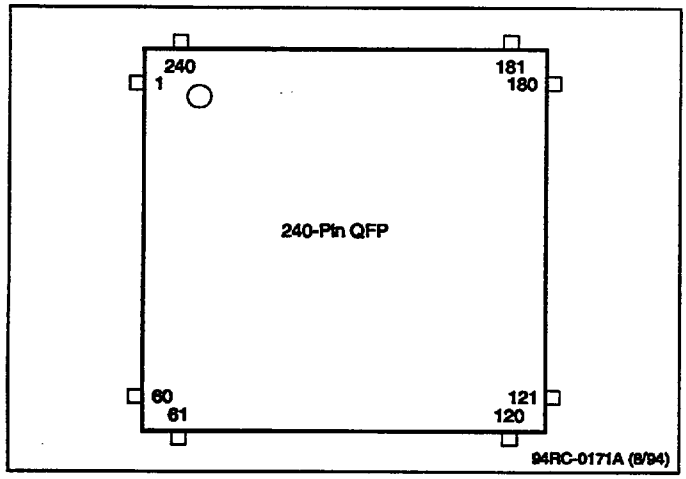
Interface Signals	Symbol	* Input/Output	Description
VR4000 family bus interface	TClock	Input	Transmit clock from CPU establishes the system interface frequency.
	RClock	Input	Receive clock from CPU establishes the system interface frequency, 90°-phase shift prior to TClock.
	SysAD[63:0]	Input/Output	System address and data bus is a 64-bit bus for communication between CPUs.
	SysADC[7:0]	Input/Output	System address and data check bus is an 8-bit bus containing check bits for the SysAD bus.
	SysCmd(8:0)	Input/Output	System command and data identifier is a 9-bit bus for transmission between CPUs.
	$\overline{\text{Release}}$	Input	$\overline{\text{Release}}$ is the CPU response signal indicating that ownership of the system interface is available to the external agent.
	$\overline{\text{PWrRdy}}$	Input	Processor write ready is the VR4x00 write ready control. It is asserted by the -IOC controller to indicate that the system is ready for the processor write request.
	$\overline{\text{ValidIn}}$	Input/Output	Valid input informs the CPU that an address or data on the SysAD bus and a valid command or data identifier on the SysCmd bus are being driven. External pullup required.
	$\overline{\text{ValidOut}}$	Input	Valid output is asserted by the CPU to indicate that it is driving a valid address or data on the SysAD bus and a valid command or data identifier on the SysCmd bus.
	$\overline{\text{PERR}}$	Output	Parity error
Slave mode montrol interface	$\overline{\text{WrRdy}}$	Output	Write ready is the -IOC write ready control. It connects to $\overline{\text{RWrRdy1}}$ of the -IOC controller to indicate that the memory is ready for the processor write request and DMA write.
	$\overline{\text{RValidIn}}$	Output	RAB2IT valid input is to inform the -IOC controller that an address or data on the SysAD bus and a valid command or data identifier on the SysCmd bus are being driven to it. External pullup required.
	$\overline{\text{RValidOut}}$	Input	RAB2IT valid output is asserted by the -IOC controller to indicate that it is driving a valid address or data on the SysAD bus and a valid command or data identifier on the SysCmd bus.
	$\overline{\text{RRelease}}$	Input	RAB2IT release is the response signal from the -IOC controller to indicate the availability of the system interface
Secondary cache interface	$\overline{\text{CDRD}}$	Output	Cache data read
	$\overline{\text{CDWR}}$	Output	Cache data write
	CA3(A:B)	Output	Least significant cache address, A0
	CA4(A:B)	Output	Second least significant cache address, A1
DRAM and synchronous DRAM control interface	MD(71:0)	Input/Ouput	72-bit memory data bus
	MA(11:0)	Output	12-bit memory address bus
	BS	Output	Synchronous DRAM bank select
	WE	Output	Write enable
	DQM/$\overline{\text{CAS}}$(3:0)	Output	Data mask for sync DRAM and column address strobe for regular DRAM.
	$\overline{\text{CS}}$/$\overline{\text{RAS}}$(3:0)	Output	Chip select for sync DRAM and row address strobe for regular DRAM.
	CKE/SLVC	Input/Output	Clock control for sync DRAM and master/slave control for regular DRAM
	$\overline{\text{SRAS}}$	Output	Synchronous DRAM row address strobe
	$\overline{\text{SCAS}}$	Output	Synchronous DRAM column address strobe

Table 4. Pin Descriptions, 240-Pin PQFP (cont)

Interface Signals	Symbol	* Input/Output	Description
Test and initialization	$\overline{\text{Reset}}$	Input	$\overline{\text{Reset}}$ must be asserted for any reset sequence
	RA0	Input	Initialize internal register address
	TEST	Input	NEC test pin

* I/O and O pins are Hi-Z in the Reset state.

Figure 6. Pin Configuration, 240-Pin PQFP



MICROPROCESSOR INTERFACE

CPU Protocol Handler

The CPU protocol is the interface between the processor and the RAB2IT chip sets. All elements are identical to the system interface protocol of the VR4000 family processors except CPU $\overline{\text{WrRdy}}$ should be connected to $\overline{\text{PWrRdy}}$ of RAB2IT-MEMC.

Read Buffer

One 8-byte, 16-stage read buffer of the RAB2IT-MEMC gives the best processor read request performance to match the maximum readblock size (32-word) of VR4400SC. The effective data size is set by SysCmd in an address cycle.

Write Buffers

Two 8-byte wide write buffers—single- and block-write—of the RAB2IT-MEMC reduce the pipeline stall cycles during the processor write request.

The two-stage single-write butffer consecutively accepts doubleword, word, and partial word processor writes. The 16-stage buffer for block write, including memory write and DMA write, matches the maximum write block size (32-word) of VR4400SC. The effective data size is set by SysCmd in an address cycle.

RAB2IT-MEMC drives the $\overline{\text{WrRdy}}$ and $\overline{\text{PWrRdy}}$ active (low) all the time except if the first stage of the single-write buffer or any stage of the block-write buffer is filled. In addition, it performs weight control for all stages of the buffers to secure the received write data without failure. However, if single-write or block-write fails to receive the "busy" status of WrRdy, the buffer weight control cannot be performed.

Address Register/Command Register

An address register is to hold and decode addresses on the SysAD bus, and a command register is to hold and decode the system interface commands. The addresses of data that have been decoded and match the address area of the RAB2IT-MEMC will be registered in the address queue.

RAB2IT-MEMC Controller

A five-stage address queue handles the SysAD input and a one-stage address queue is used for SysAD output. Two out of five stages in the input SysAD queue are used for the DMA bypass access.

The values of the 32-bit registers are copied to both high-order and low-order bits of the data bus during a register read cycle. On a register write cycle, the high-order 32-bit data on the data bus is written to the 32-bit register when the big endian configuration is set on word write mode. Otherwise, the low-order 32-bit data on the data bus is written to the 32-bit register with the little endian configuration.

MEMORY INTERFACE

DRAM Controller

The DRAM controller in RAB²IT-MEMC is capable of controlling the standard high-speed DRAM interface as well as a synchronous DRAM interface.

The RAB²IT-MEMC does not process the data but swaps, redirects, or merges the data among system memory, processor or I/O interface according to the endian configuration and data size.

ECC/Parity. RAB²IT-MEMC generates 1-bit correction and 2-bit detection for the ECC (Error Checking and Correcting) code during DRAM or sync DRAM access cycles by setting the device control register. RAB²IT-MEMC can also use the parity on SysAD bus operation.

Word Write. On doubleword, word, or partial word write cycles, RAB²IT-MEMC reads the data at the appropriate addresses in memory as doubleword data and rewrites the valid data by merging them. On processor read cycles, the RAB²IT-MEMC always sends the doubleword data to the processor. The processor will fetch the valid word or partial word data internally during the non-doubleword read cycles. The ECC code is included in the rewritten data when the ECC function is on. The data is correct if a 1-bit error is found.

Endian. The byte order of the doubleword (64-bit), word (32-bit), half-word (16-bit), and byte (8-bit) can be designated in big endian or little endian by a device control register in RAB²IT-MEMC. See figures 7 and 8.

Figure 7. Addresses of Bytes Within Doublewords; Big-Endian Byte Alignment

64							0	Doubleword Address
16	17	18	19	20	21	22	23	16
8	9	10	11	12	13	14	15	8
0	1	2	3	4	5	6	7	0

- Most-significant byte is at lowest address.
- Word is addressed by byte address of most-significant byte.

Figure 8. Addresses of Bytes Within Doublewords; Little-Endian Byte Alignment

64							0	Doubleword Address
23	22	21	20	19	18	17	16	16
15	14	13	12	11	10	9	8	8
7	6	5	4	3	2	1	0	0

- Least-significant byte is at lowest address.
- Word is addressed by byte address of least-significant byte.

Table 5. Memory Type and Size for VR4x00/RAB²IT System

Type of SIMM	Size in Minimum Configuration (2 SIMMs)	Number of SIMMs in Maximum Configuration	Remarks: Double-Sided/Single-Sided	Remarks: NEC Product Code
1M x 36 bit (4M byte)	8M byte	8	Single	MC-421000A36
2M x 36 bit (8M byte)	16M byte	4	Double	MC-422000A36
4M x 36 bit (16M byte)	32M byte	8	Single	MC-424000A36
8M x 36 bit (32M byte)	64M byte	4	Double	MC-428000A36
16M x 36 bit (64M byte)	128M byte	8	Single	
32M x 36 bit (128M byte)	256M byte	4	Double	

Notes:

(1) The different memory-size SIMMs can be installed simultaneously.

(2) Two banks for one double-sided SIMM.

(3) In master/slave mode, the memory configurations of master side and slave side should be identical.

DRAM Protocol Handler

The standard DRAM interface—RAS, CAS, and multiplexed address—is controlled by the DRAM protocol handler. It is able to support the system memory configuration from 8M-byte to 512M-byte with the DRAM type from 4M (1M x 36) to 128M (32M x 36) DRAMs. See table 5 for details. Figure 9 and table 6 illustrate the four memory banks system configurations.

Figure 9. RAB²IT-MEMC and DRAM (72-Pin SIMM) Interface

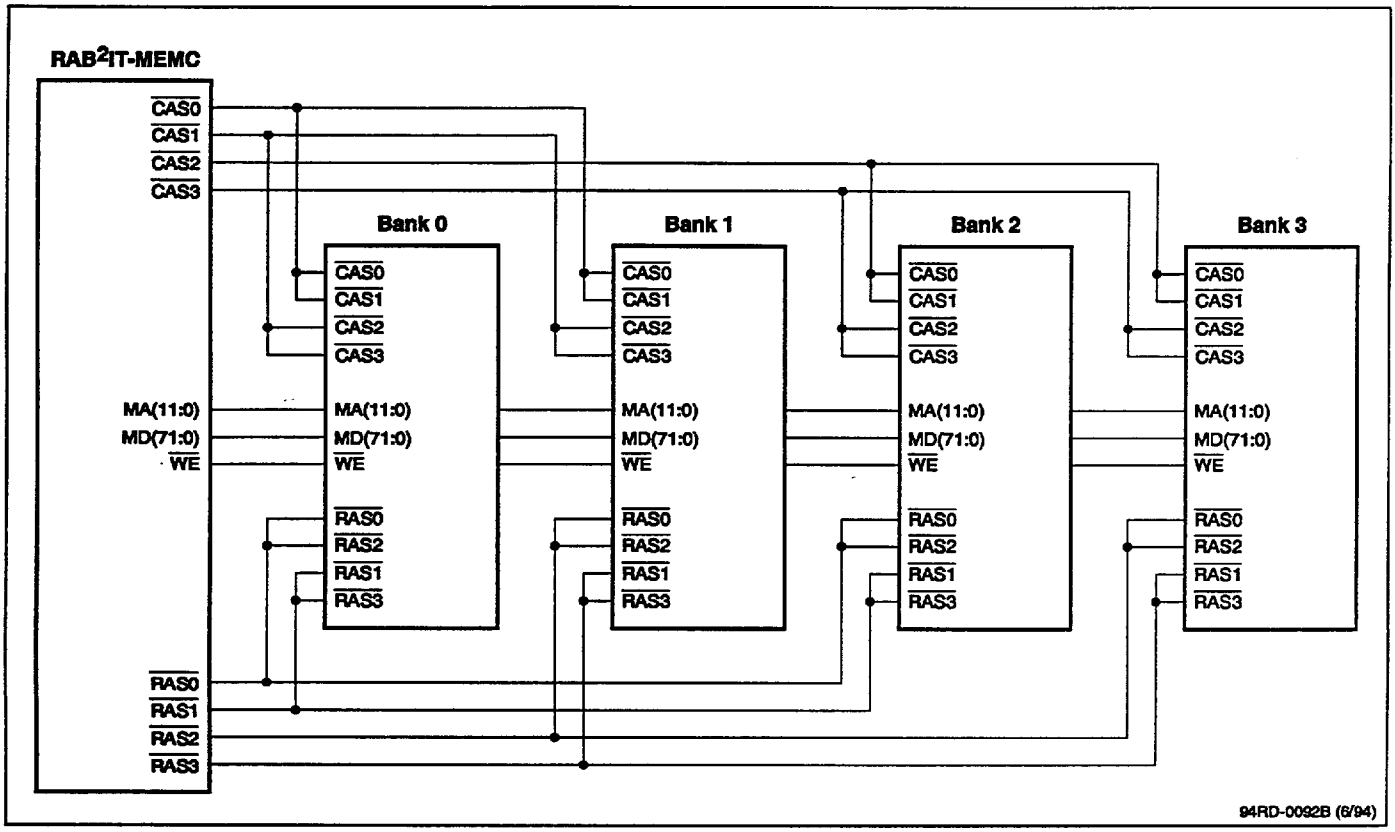
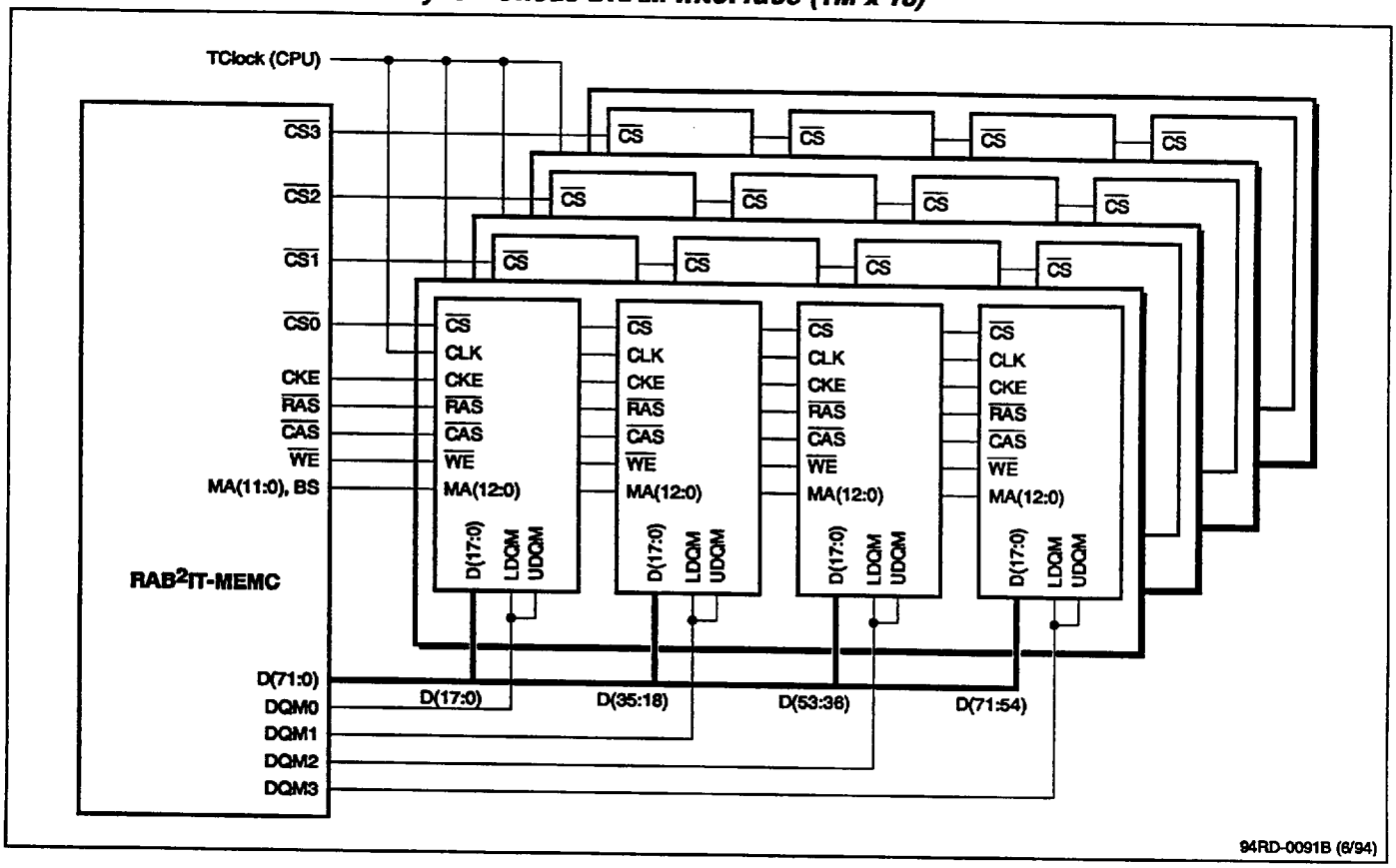


Table 6. Memory and Capacity In Each Bank

Memory Bank				Memory Size
0	1	2	3	
8M				8M
8M	8M			16M
8M	8M	8M		24M
8M	8M	8M	8M	32M
32M				32M
32M	8M			40M
32M	8M	8M		48M
32M	8M	8M	8M	56M
32M	32M			64M
32M	32M	8M		72M
32M	32M	8M	8M	80M
32M	32M	32M		96M
32M	32M	32M	8M	104M
32M	32M	32M	32M	128M
128M				128M
128M	8M			136M
128M	8M	8M		144M
128M	8M	8M	8M	152M
128M	32M			160M
128M	32M	8M		168M
128M	32M	8M	8M	176M
128M	32M	32M		192M
128M	32M	32M	8M	200M
128M	32M	32M	32	224M
128M	128M			256M
128M	128M	8M		264M
128M	128M	8M	8M	272M
128M	128M	32M		288M
128M	128M	32M	8M	296M
128M	128M	32M		320M
128M	128M	128M		384M
128M	128M	128M	8M	392M
128M	128M	128M	32M	416M
128M	128M	128M	128M	512M

Note: Two 72-pin SIMMs are counted as one bank if single-sided or two banks if double-sided.

Figure 10. RAB²IT-MEMC and Synchronous DRAM Interface (1M x 18)



Synchronous DRAM Protocol Handler

The synchronous DRAM protocol handler is to control SRAS, SCAS, CKE, CS, and the multiplexed address of the synchronous DRAM interface. It is able to support configurations from 8M-byte to 64M-byte with 2M (1M x 18 or 2M x 9) synchronous DRAMs. See table 7 for details. Table 8 and figure 10 illustrate the four memory banks system configurations.

Table 7. Synchronous DRAM Type and Size for VR4x00/RAB²IT System

Type	Minimum Configuration and Size		NEC Product Code
	Size	Number	
1M x 18-bit	8M byte	8	μPD4516181
2M x 9-bit	16M byte	4	μPD4516821
1M x 18-bit	32M byte	16	μPD4516181
2M x 9-bit	64M byte	32	μPD4516821

Table 8. Synchronous DRAM Memory and Capacity In Each Bank

Memory Bank				Memory Size
0	1	2	3	
8M				8M
8M	8M			16M
8M	8M	8M		24M
8M	8M	8M	8M	32M
16M				16M
16M	8M			24M
16M	8M	8M		32M
16M	8M	8M	8M	40M
16M	16M			32M
16M	16M	8M		40M
16M	16M	8M	8M	48M
16M	16M	16M		48M
16M	16M	16M	8M	56M
16M	16M	16M	16M	64M

The synchronous DRAM mode should be set prior to operation of the synchronous DRAM access cycle. The mode should be set as follows.

Burst size = 2

CAS latency = 2 or 3

Wrap type may be either sequential or interleave (The same operation is performed when burst size = 2.)

The mode does not support a unique function from a manufacturer.

Ten commands for synchronous DRAMs are listed below.

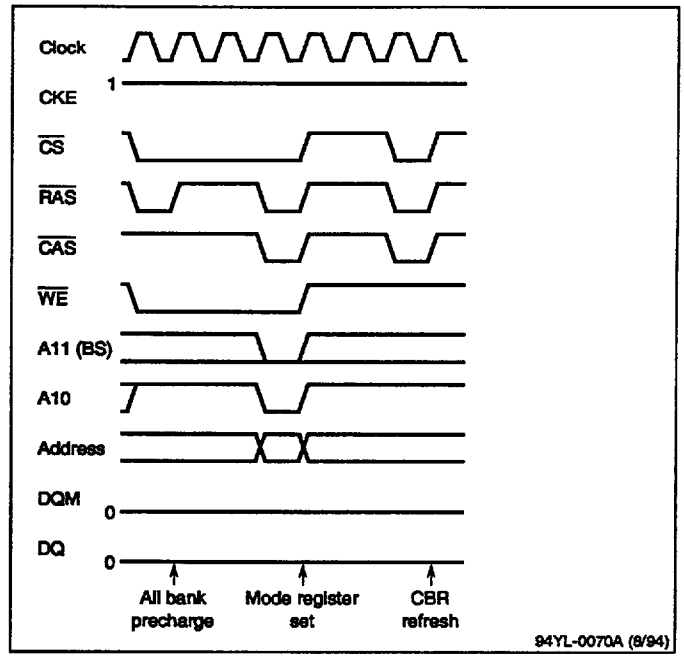
Mode register set
CBR refresh
Entry self-refresh
Self-refresh end
Bank active
Write
Write and autoprecharge
Read
Read and autoprecharge
Data mask

Block write, partial write, block read, and partial read cycles are initiated by the processor or the -IOC controller. The -MEMC controller generates the corresponding synchronous DRAM interface protocol to accomplish the access cycles.

A refresh timer that has been initialized requests the refresh cycles at certain time intervals. The refresh cycles occur by issuing the "CBR refresh" command. But the command should not be issued until the RAS high pulse width meets the timing set in the DRAM speed register and all of the chip select signals are active. The self-refresh function is also provided when the DRAM sleep control register is set.

Mode Setting. Setting is done by writing 0021H or 0031H into the synchronous DRAM mode register. After the register is set, the "all bank precharge" command is issued followed by the "mode register set" command three clocks later. Then, wait for three or more clocks to activate "CBR refresh" twice and terminate the mode setting. See figure 11.

Figure 11. Mode Setting



Block Write. The CPU or RAB2IT-IOC initiates the block write cycle by asserting MA(11:0) and BS for the period of time equal to RAS-high width and asserting CS. The RAS activates the bank select and the CAS, along with "write" command, performs the write operation with sub-block ordering. Instead of the last "write," "write and autoprecharge" is asserted to terminate the cycle and perform the precharge. See figure 12.

Partial Write. The CPU or RAB2IT-IOC initiates the partial write cycle by asserting MA(11:0) and BS for the period of time equal to RAS-high width and asserting CS. The RAS activates the bank select and the CAS, along with "read" command, reads the data, which is used to merge the data from the CPU. The merged data is written to memory with "write and autoprecharge" command two clocks later after "read." The data and "write and autoprecharge" command are asserted immediately without the first read if in doubleword write cycle. The "data mask" command is asserted in the next clock. See figure 13.

Figure 12. Block Write

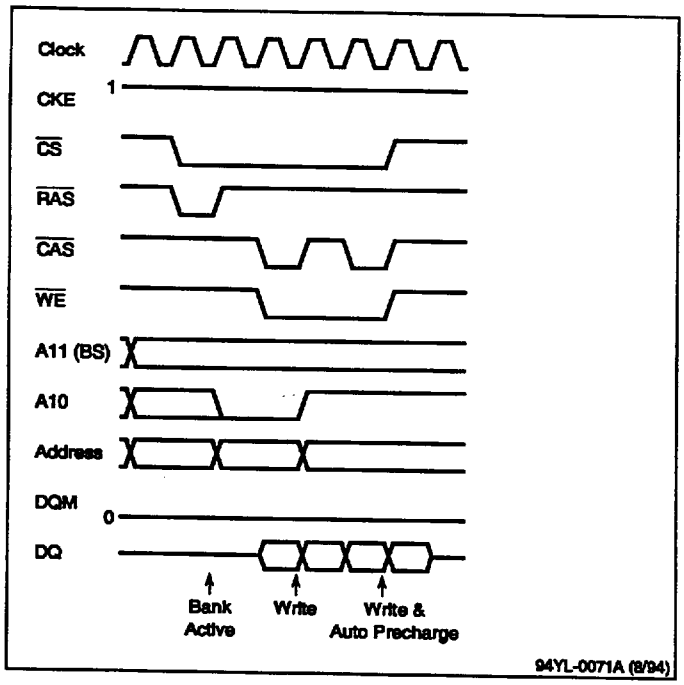
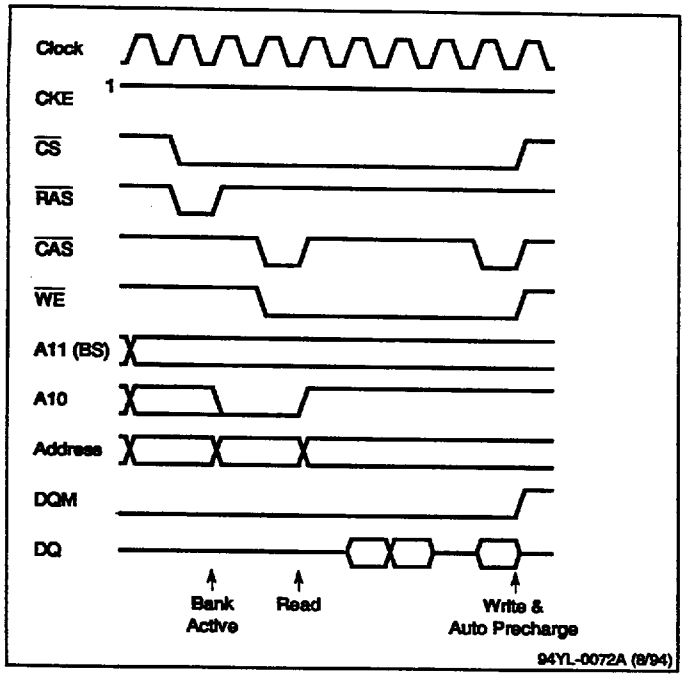
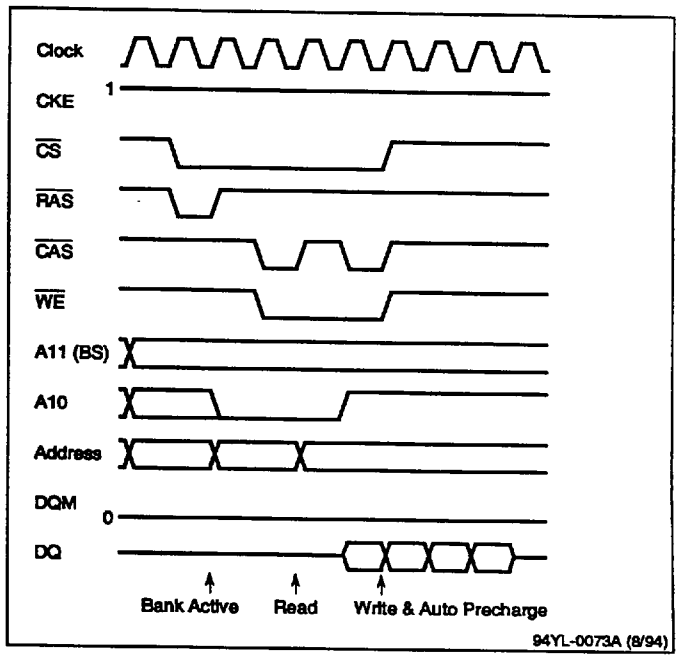


Figure 13. Partial Write



Block Read. The CPU or RAB²IT-IOC initiates the block write cycle by asserting MA(11:0) and BS for the period of time equal to $\overline{RAS}$-high width and asserting $\overline{CS}$. The $\overline{RAS}$ activates the bank select and the $\overline{CAS}$, along with "read" command, performs the read operation with sub-block ordering. Instead of the last "write." "write and autoprecharge" is asserted to terminate the cycle and perform the precharge. See figure 14.

Figure 14. Block Read



CBR Refresh. All "chip select" commands are activated after a period of time equal to the $\overline{RAS}$-high width, which is set in the refresh timer. Then, the "CBR refresh" command is asserted to perform the refresh operation. See figure 15.

Figure 15. CBR Refresh

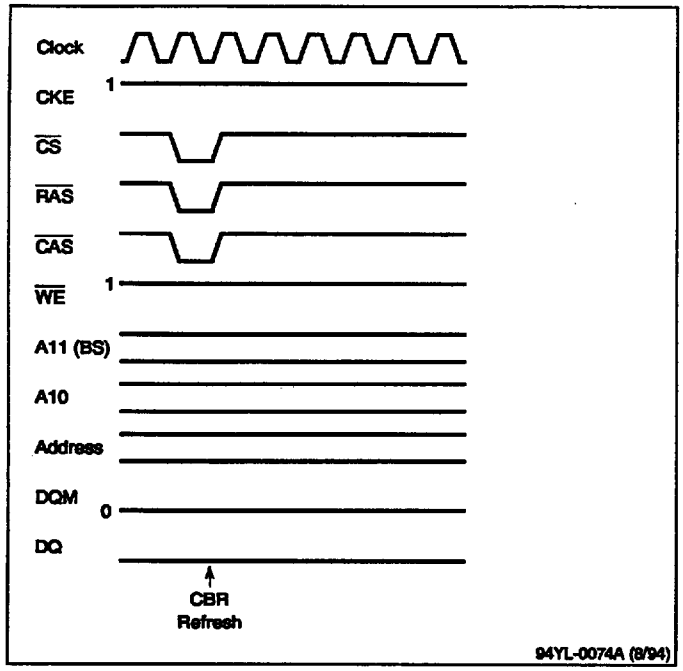


Figure 16. Self-Refresh

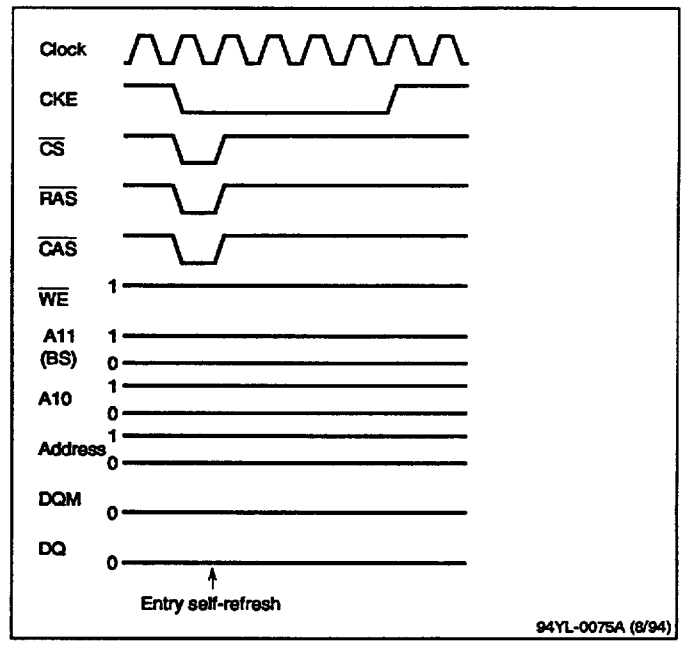
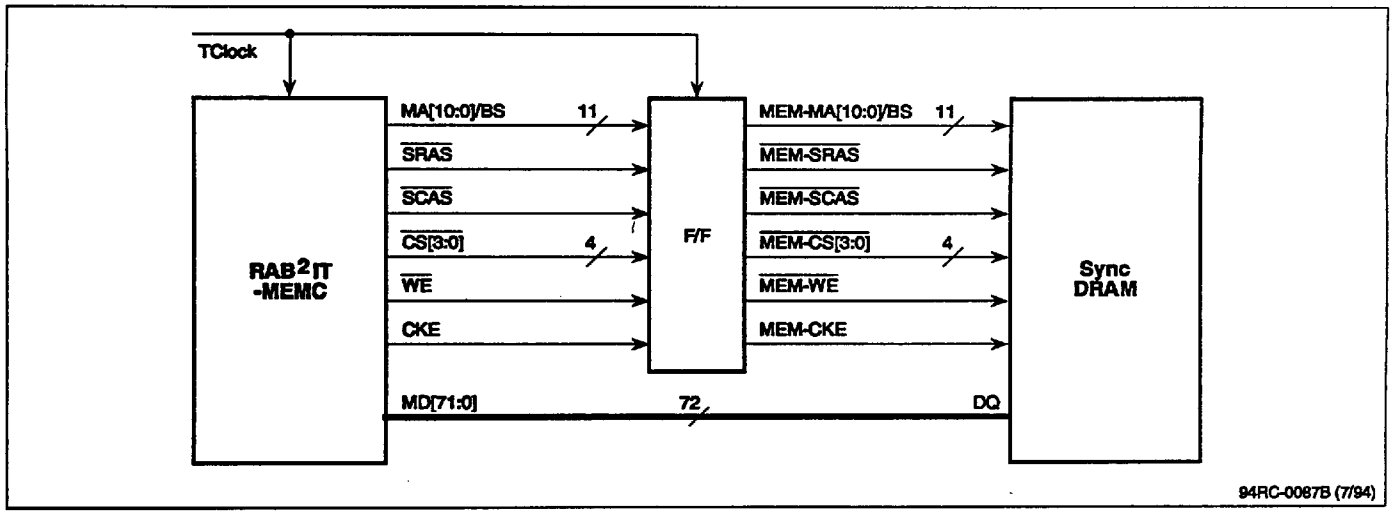


Figure 17. System Diagram With Buffer



Self-Refresh. Self-refresh is required by a refresh request signal from the refresh timer in standby mode. All "chip select" commands are activated after a period of time equal to the $\overline{RAS}$-high width, which is set in the refresh timer. Then, the "entry self-refresh" command is asserted to perform the refresh operation. Once the CPU or RAB2IT-IOC accesses the memory in the self-refresh state, the "self-refresh end" command is asserted to exit the self-refresh cycle. If the DRAM sleep control register is not written, the self-refresh is activated again on any refresh request signal sent by the refresh timer. See figure 16.

Buffer. The buffer mode can be configured as the system memory bus loading is overloaded. Access is made at one clock-pulse interval and the duration of the output is prolonged by two clock signals with the CKE signal. See figure 17.

Table 9. Multiplexer

			MA											
			0	1	2	3	4	5	6	7	8	9	10	11	BS
		$\overline{RAS}$	21	20	19	18	17	16	15	14	13	12	22	24	11
$\overline{CAS}$	Single Mode	1M DRAM	3	4	5	6	7	8	9	10	22	11			11
		4M DRAM	3	4	5	6	7	8	9	10	23	11	24		11
		16M DRAM	3	4	5	6	7	8	9	10	23	11	25	26	11
		16M Sync DRAM	3	4	5	6	7	8	9	10	23		CMD	24	11
		64M Sync DRAM	3	4	5	6	7	8	9	10	23	25	CMD	24	11
	MS	1M DRAM	23	4	5	6	7	8	9	10	22	11			11
		4M DRAM	23	4	5	6	7	8	9	10	22	11	24		11
		16M DRAM	23	4	5	6	7	8	9	10	22	11	25	26	11

Multiplexer

The RAB²IT-MEMC has a built-in multiplexer for the DRAM or Sync DRAM interface. Table 9 shows correspondence of the processor addresses and DRAM addresses. $\overline{RAS}$ addresses are common on all modes.

Parallel Mode

Two -MEMC controllers can be operated in parallel to increase the memory interface performance and expand memory size. For this feature, internal register address change function and master/slave mode function are provided.

Internal Register Address Change. This function is turned on for each device by the RAO input on reset. And the addresses of the registers are determined by the value of the RAO on the memory address bus of RAB²IT-MEMC during reset.

RAO	Register Address Allocation
0	1 1400 03xx ~ 0 1400 03xx
1	1 1400 02xx ~ 0 1400 02xx

Master/Slave Operation. In this mode (figures 18 and 19), data transfer is performed at high bus bandwidth with 128-bit memory system bus configuration. One -MEMC performs as master with 64-bit DRAM data throughput; the other performs as slave with 64-bit DRAM data throughput. On the SysAD bus, master -MEMC only uses the SysAD[31:0] for data transfer and slave -MEMC uses SysAD[63:32] for data transfer. With this configuration, block cycles can be done by accessing memory once, 1.5 CPU bus cycle time, for one or two doublewords of data to satisfy the VR4x00 family processor. At the CPU point of view, it is identical to a single external agent configuration.

The CKE/SLV, which is controlled by the master -MEMC, is used to synchronize the master and slave -MEMCs during memory cycles.

Parallel Operation. Two -MEMCs are able to operate independently in parallel mode to meet the large memory size requirement with different address allocations.

Error Detection and Correction

The RAB²IT-MEMC has the function of detecting and correcting errors in memory access cycles with the parity and ECC (SECDED) code. Parity is used to read from and write to CPU/RAB²IT-IOC and ECC code is used for the data transfer between memory. In write cycles, -MEMC adds the ECC codes to the data sent by -IOC after parity check and writes them to memory. In read cycles, -MEMC sends data to -IOC after ECC checking. See table 10.

Data in the DRAM should be initialized at power on if the ECC function is active. Normal ECC codes are written to the memory area by using block write function, or by using partial write function to all memories with the MSKERR bit set to 1 in the device control register.

Table 10. Error Detection With MSKERR and MSKERR1 Status

	* MSKERR, MSKERR1			
Error	0,0	0,1	1,0	1,1
Parity	Detected	Detected	Not detected	Not detected
1-Bit	Detected/ corrected	Corrected	Corrected	Corrected
Multibit	Detected	Detected	Not detected	Not detected

* Detected means detectable and will enable interrupt.

Figure 18. Data Bus Scheme in Master/Slave Mode

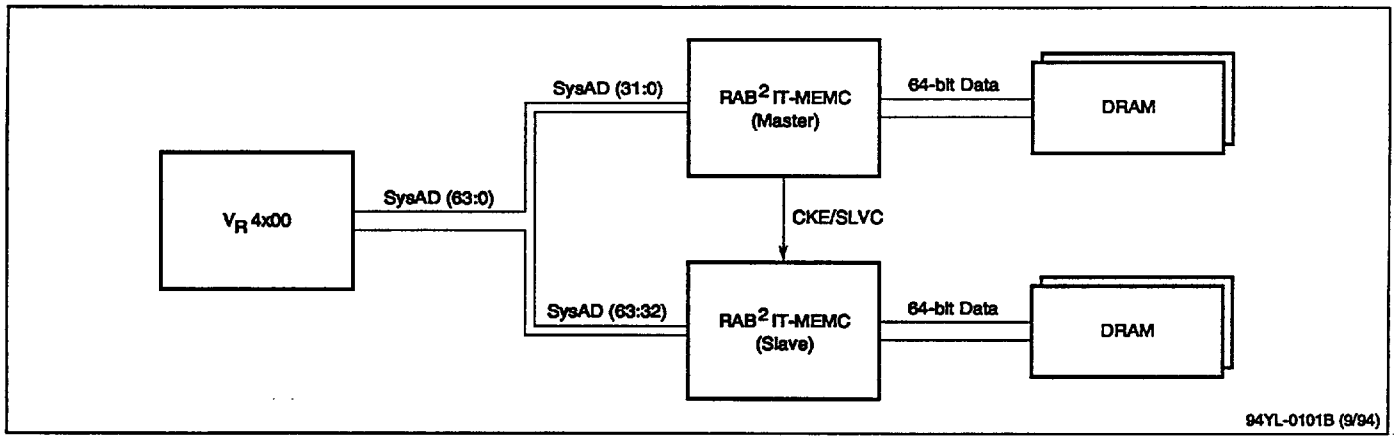
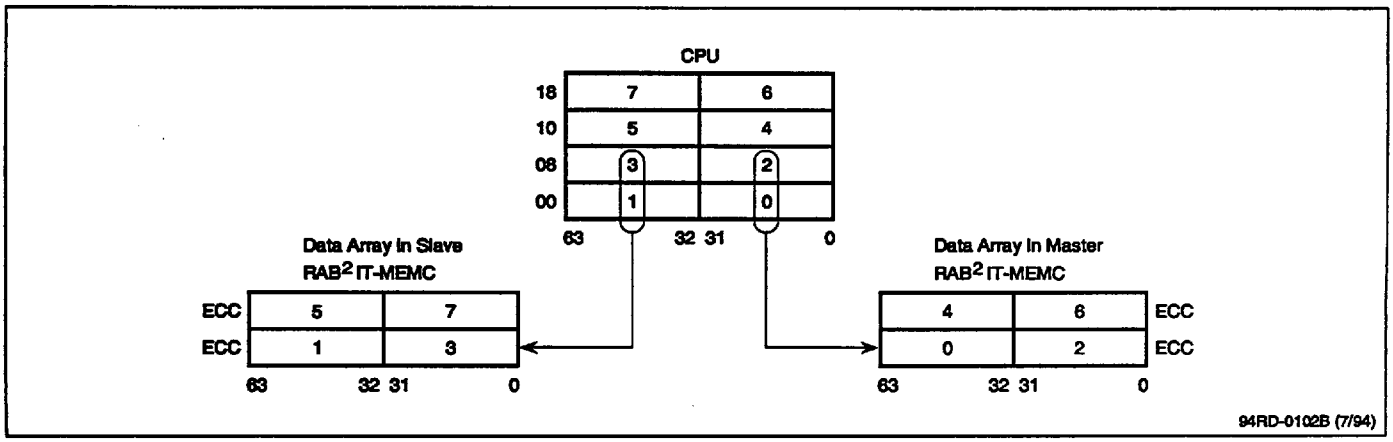


Figure 19. Data Storage in Master/Slave Mode



Parity Error. A parity error on the SysAD bus is detectable and correctable. Condition A or B below applies.

	A	B
PEO bit	0	1
or MSKERR	1	0
ERRADR bit	Indefinite	*Address
PERR bit	0	1
PERR pin	High	Low

*Error address is held until the bit is reset.

A parity error on the SysAD bus will cause the interrupt when (1) MSKERR = 0 and parity errors are detected in write cycles on the SysAD bus master device. Or (2) the address where the error occurs is set in the error address register and the PERR pin = low. Data is written to the memory but the values in the Error address register and the Error syndrome register and the status of the PERR pin are held until flushed by the Error flush register.

A parity error on the SysAD bus will not cause the interrupt when MSKERR = 1; the parity error check function is not active. The data will be written into the memory regardless of the parity error.

One-Bit Error. A one-bit error in memory is detectable (applicable to memory read) and correctable. RAB²IT-MEMC detects errors by using the ECC function in partial write to memory to perform read-modify-write. The detection occurs on A, B, or C below.

	A	B	C
PEO bit	0	1	1
or MSKERR	1	0	0
MSKERR1	—	1	1
ERRADR bit	Indefinite	Indefinite	*Address
PERR bit	0	1	1
PERR pin	High	Low	Low
Read response SysCmd5	—	0	0

*Error address is held until the bit is reset.

A one-bit error in memory will cause the interrupt when (1) MSKERR = 0, MSKERR1 = 1, and one-bit errors are detected and corrected in read cycles or partial read cycles on the SysAD bus master device. Or (2) the data in memory is read, the address where the error occurs is set in the error address register, and the error syndrome is set in the error syndrome register.

Along with the PERR pin = low, SysCMD5 will inform the CPU that the data error occurs; then the data will be sent back as read response after being corrected. The values in the error address register and the error syndrome register and the status of the PERR pin are held until flushed by the error flush register.

A parity error on the SysAD bus will not cause the interrupt when MSKERR = 1, MSKERR1 = 1, and one-bit errors are detected in read cycles or partial write cycles on the SysAD bus master device. The results detected during error correction are not reported to the processor. In read cycles, data that has been corrected will not be written back to memory. In partial write cycles, data with errors will not be in the memory since the corrected data is merged to the original data and written back to memory.

Multibit Error. Two-bit errors and 3/4-bit nibble errors can be detected and corrected (applicable to memory read). RAB²IT-MEMC detects errors by using the ECC function in partial write to memory to perform read-modify-write. The detection occurs on condition A or B below.

	A	B
PEO bit	0	1
or MSKERR	1	0
MSKERR1	—	1
ERRADR bit	Indefinite	Indefinite
$\overline{\text{PERR}}$ bit	0	1
$\overline{\text{PERR}}$ pin	High	Low
Read response SysCmd5	—	0

A multibit error in memory will cause the interrupt when (1) MSKERR = 0, MSKERR = 1, and multibit errors are detected and corrected in read cycles or partial read cycles on the SysAD bus master device. Or (2) the data in memory is read, the address where the error occurred is set in the error address register, and the error syndrome is set in the error syndrome register.

Along with the PERR pin = Low, SysCMD5 will inform the CPU that the data error occurred; then the data will be sent back as read response without being corrected.

The values in the error address register and the error syndrome register and the status of the PERR pin are held until flushed by the error flush register.

In partial write cycles, the merged data with the new ECC codes that are generated based on the data for which error correction has failed are written into memory. Therefore, the errors in memory are not corrected and will not be detected again on memory access cycles because of the new ECC codes. (The interrupt will occur in the first access.)

A parity error on the SysAD bus will not cause the interrupt when (1) MSKERR bit = 1, multibit errors are not detected. Or (2) multibit errors occur, but the data that has not been corrected is returned as response data.

Illegal Access. RAB²IT-MEMC inhibits the following bus cycles.

- Block access to the register area and cache tag area.
- Access to the memory location whose address is in the address base register and address master register, but the memory size is not in the device control register.

A special process is performed on any illegal access. The illegal access can be detected on condition A or B below.

	A	B
MSKERR	0	1
ERRADR bit	Indefinite	Indefinite
ILLACC bit	0	0
PERR pin	Low	Low
Read response SysCmd5	0	1

In write cycles, access to these areas is ignored. In read, the indefinite values are returned. The ILLACC bit in the error syndrome register will be set to 1 on accessing these areas. The bus error will be reported to the CPU by SysCMD if MSKERR bit = 0; otherwise, the SysCMD will not inform the CPU of the bus error if MSKERR bit = 1.

An interrupt request is generated by the $\overline{\text{PERR}}$ pin regardless of the status of the MSKERR bit.

Reset Error Bits. All four bits below are reset simultaneously by RESET = 0. When error bits are cleared, the ERRADDR bit is cleared.

ERERR bit	Bit Reset
0 = 1	ERRI = 0
1 = 1	ERR = 0
2 = 1	PERR = 0
3 = 1	ILLACC = 0

ECC in Master/Slave Mode. ECC detection is also performed on the 128-bit basis in master/slave mode. That is, as error exists in a four-word area, which masked bit 3 in the error address register. Master RAB2IT-MEMC asserts SysCMD5 in memory access cycles, and the $\overline{PERR}$ pin is used for error notification by slave RAB2IT-MEMC. The error address register, error syndrome register, and error flush register are in both the master and slave RAB2IT-MEMC.

SECONDARY CACHE CONTROLLER

The RAB2IT-MEMC incorporates the secondary cache interface controller to support VR4x00PC and VR4200 processors, which do not have the integration of the secondary cache interface. The local secondary cache can be configured as 256K- or 512K-byte size. The internal Tag and Comparator determines the hit/miss cycles; data flows are handled through the interface signals: CA3, CA4, $\overline{CDRD}$, and $\overline{CDWR}$. See figure 20.

Cache Tag

The internal cache tag memory has 2048 entries. Each entry consists of a 14-bit tag part, 16-bit valid bit part, and one-line valid bit. For a 256K-byte configuration, a 32-word cache line size and a 4-word sub-block are used. For the 512K-byte configuration, a 64-word cache line size and a 4-word sub-block are used. On system reset, all the line invalid bits are reset. Validity of each sub-block is checked by ANDing valid bits of each sub-block.

The cache tag can be read and written by accessing the address 0x1 1800 0000 through 0x1 IBFF FFFF. The values for read and write are shown below. Writing to the undefined location is ignored.

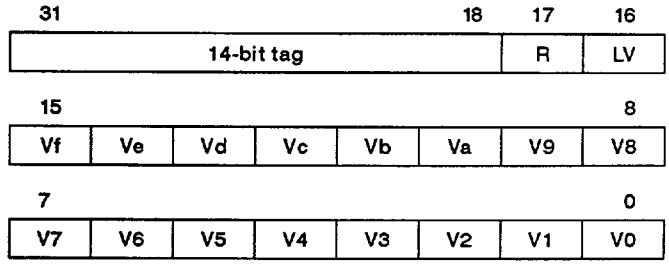
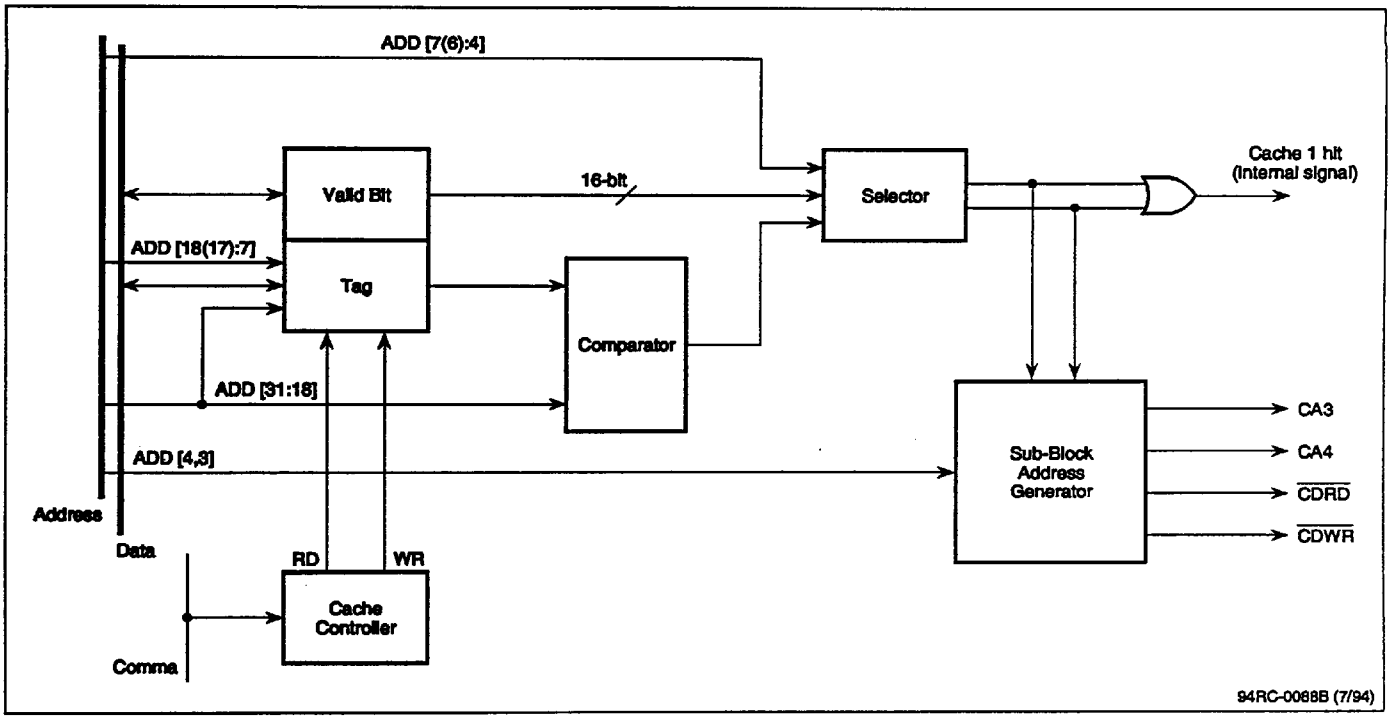
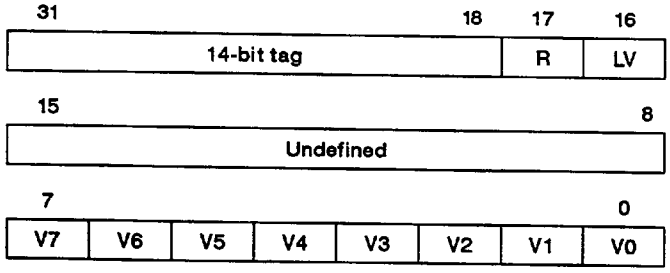


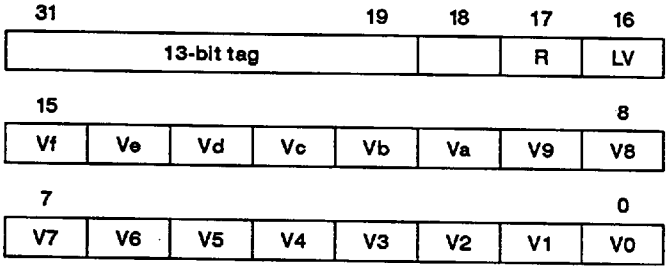
Figure 20. 512K (256K) Mode Cache Block Diagram



In 256K mode, 2K entries are selected by address bits 17-7. The address written into the cache tag is A[31:18]; A[6:4] select the valid bits.



In the 512K mode, 2K entries are selected by address bits 18-8. The address written into the cache tag is A[31:19]; A[7:4] select the valid bits.



Comparator. The cache address comparator is 14 bits wide.

Selector. The selector selects 2 bits correspondent to an 8-word block transfer from among the 16 valid bits.

Cache Control Operation

On cache read miss, the tag values are updated and appropriate valid bits are set; then the rest of the valid bits are reset. Cache line fill cycle is asserted with sub-block ordering after the line valid bit is set.

On cache read hit if valid bit = 0 (invalid), appropriate valid bits are set, but the rest of the valid bits are not reset. Cache line fill cycle is asserted with sub-block ordering.

On cache write hit, correspondent valid bits are reset. There is no operation on cache write miss.

For block read cycles generated by the processor, data will be provided to the processor in doubleword, word, and partial word format on cache hit.

Cache Coherency

- Processor Write. Tag memory is checked and valid bits of the hit tag are set invalid. Data in the secondary cache will not be updated.
- Processor Read. If a tag memory is checked and hit, the values in the tag are not changed and data in the secondary cache is sent to the processor without being modified.

In block read miss, the tag addresses are updated and appropriate valid bits are set. Data in the secondary cache will be replaced with data from the DRAM (cache line fill).

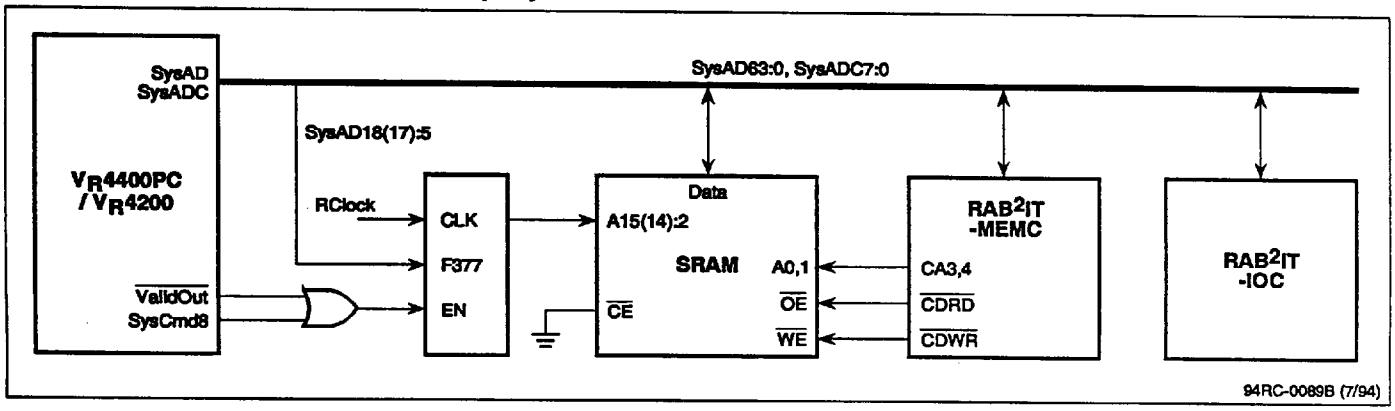
Cache Interface

Figure 21 shows the system configuration with 512K (256K) secondary cache memory interface. RAB²IT-MEMC generates the low-order address bits, A3 and A4, according to the sub-block ordering.

RAB²IT-IOC PROTOCOL HANDLER

Signals $\overline{\text{RValidIn}}$, $\overline{\text{RValidOut}}$, and $\overline{\text{RRelease}}$ are the interface signals between -IOC and -MEMC. This protocol is used when the processor releases the bus mastership, such as DMA transfer function. The details of the DMA operation are in the RAB²IT-IOC data sheet.

Figure 21. RAB²IT-MEMC and 512K(256) SRAM Interface



RAB2IT-MEMC CONTROL REGISTERS

Table 11 shows the internal registers of the RAB2IT-MEMC. The addresses of these internal registers are determined by the status of RAO.

Table 11. Internal Register Map

Register Name	Read/ Write	Address (on reset) RAO = 0	RAO =1	Default
Device control register	R/W	1 1400 0200	1 1400 0300	0002 0000
Address base register	R/W	1 1400 0208	1 1400 0308	0000 0000
Address mask register	R/W	1 1400 0210	1 1400 0310	0000 0000
Sync DRAM mode register	R/W	1 1400 0218	1 1400 0318	000 0001
DRAM speed register	R/W	1 1400 0220	1 1400 0320	0000 0000
Refresh counter	R/W	1 1400 0228	1 1400 0328	000F 0000 Refresh Disable
DRAM sleep control register	R/W	1 1400 0230	1 1400 0330	0000 0000
Secondary cache control register	R/W	1 1400 0238	1 1400 0338	000 0000
Secondary cache flush register	W	1 1400 0240	1 1400 0340	Invalid
Error address register	R	1 1400 0248	1 1400 0348	Invalid
Error syndrome register	R	1 1400 0250	1 1400 0350	Invalid
Error flush register	W	1 1400 0258	1 1400 0358	Invalid
Address limit register	R/W	1 1400 0260	1 1400 0360	
	R	1 1400 0264	1 1400 0364	

Device Control Register

The device control register (table 13) contains the basic setting information of the RAB2IT-MEMC. The setting information includes Slave mode, re-mapping of the I/O area, endian, ECC/Parity operation, DRAM type, and bank configuration; the register is initialized on the system initialization sequence.

Table 12. Device Control Register

31 — 26	25 MER	24 2BK	23 MS 22	21 DP

20 RI	19 BED	18 EPO	17 MEI	16 SDR	15 B3E	14 B2E	13 B1E	12 B0E

11 B3S 9	8 B2S 6	5 B1S 3	2 B0S 0

Field	Name	Description
25	MSKERR	ECC error/parity detecting mask. 1: Default setting on DRAM initialization
24	2 Bank	
23-22	M_Slave	00: Single mode; 10: Master mode; 01: Undefined; 11: Slave mode
21	D_Pat	Read response data pattern. 0: D; 1: Dx
20	Remap_IO	0: Remap 0x1 1000 0000 ~ 0x1 1FFF FFFF to 0x0 1000 0000 ~ 0x0 1FFF FFFF
19	Big_Endian	0: Little endian (default); 1: Big endian
18	EPO	0: Parity; 1: ECC
17	MSKERR1	0: Interrupt on 1-bit error occurs during ECC mode (default)
16	SyncDRAM	0: Standard DRAM; 1: Synchronous DRAM
15	Bank3_En	1: Memory is installed in Bank 3
14	Bank2_En	1: Memory is installed in Bank 2
13	Bank1_En	1: Memory is installed in Bank 1
12	Bank0_En	1: Memory is installed in Bank 0
11-9	Bank3_Size	Memory size on each bank 000: 8M-byte; 011: 64M-byte; 001: 16M-byte; 100: 128M-byte; 010: 32M-byte; 101: 256M-byte.
8-6	Bank2_Size	
5-3	Bank1_Size	
2-0	Bank0_Size	

Address Base Register

The Address Base register (table 13) indicates the address of the memory area controlled by the RAB2IT-MEMC.

Table 13. Address Base Register

31	23	22	0
Mem_Base		—	

Field	Name	Description
31-23	Mem_Base	The base address of the installed area for 8M-byte block.

Address Mask Register

The Address Mask register (table 14) is used to mask the address decoder and specify the range of memory area to be controlled by the RAB²IT-MEMC. A 1 is set in a bit correspondent to the address for masking. For this register, a 1 must be set beginning with bit 23. Thus, the following nine values can be set:

0 0000 0001	0 0001 1111	1 1111 1111
0 0000 0011	0 0011 1111	
0 0000 0111	0 0111 1111	
0 0000 1111	0 1111 1111	

Table 14. Address Mask Register

31	23	22	0
Mem_Mask		—	

Field	Name	Description
31-23	Mem_Mask	Designates a bit used to mask address decoding of a memory area;. 0's are in the least significant 23 bits in the address.

Synchronous DRAM Mode Register

The Synchronous DRAM Mode register (table 15) indicates the synchronous DRAM mode. The least significant 13 bits are invalid and the most significant 15 bits are ignored in write. The values are latched inside the RAB²IT-MEMC and written into the mode register of synchronous DRAM. The values are read into the least significant 13 bits and 0 is written to the most significant 51 bits in read. Burst length should be set to 2. CAS latency should be 2 or 3. Do not set any other values.

Table 15. Synchronous DRAM Mode Register

63	17	16	13	12	0
—		Buffer	—	Sync Set	

Field	Name		Description
16	Buffer		Set for using buffer. Timing changed by one clock pulse.
12-7	Sync Set		
† 6-4		Latency	001: 1; 010: 2; 011: 3
3		Wrap type	0: Interleave (sub block); 1: Sequential
*2-0		Burst length	000: 1; 001: 2; 010: 4; 011: 8; 111: Full page

* Bits 2 through 0 are fixed at 001 for RAB²IT-MEMC.
† Set 010 or 011 in bits 6 through 4.

DRAM Speed Register

The DRAM Speed register (table 16) specifies the access timing for DRAM. The least significant 7 bits are valid and the most significant 57 bits are ignored in write. The values are read into the least significant 7 bits, and 0 is written to the most significant 57 bits in read. See figure 22.

Table 16. DRAM Speed Register

63	7	6	5	4	3	2	1	0
—		CAS	RFU	RIC		RFU	CIC	

Field	Name	Description		
6	CA_Sup	One clock pulse is added as the time from the first column address to $\overline{CAS}$		
5	RFU	Reserved		
4-3	$\overline{RAS}$_Cycle		† $\overline{RAS}$ to Addr	$\overline{RAS}$ min
		00	1 TClock	3 TClock
		01	2 TClock	4 TClock
		10	3 TClock	5 TClock
		11	4 TClock	6 TClock
1-0	$\overline{CAS}$_Cycle		$\overline{CAS}$ low	$\overline{CAS}$ high
		00	1.5 TClock	0.5 TClock
		01	2.0 TClock	1.0 TClock
		10	2.5 TClock	1.5 TClock
		11	3.0 TClock	2.0 TClock

† Time from $\overline{RAS}$ to column address.

Figure 22. DRAM Timing

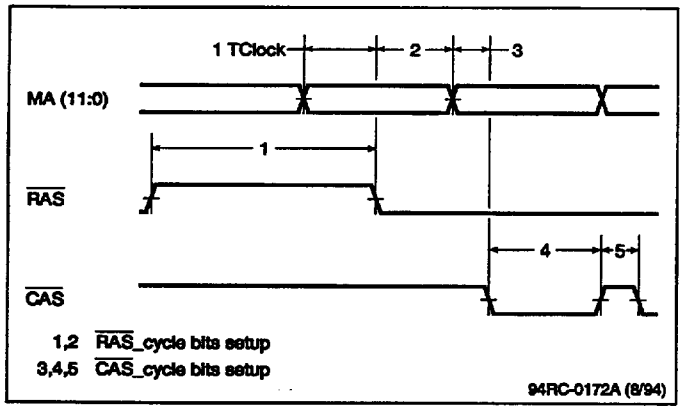
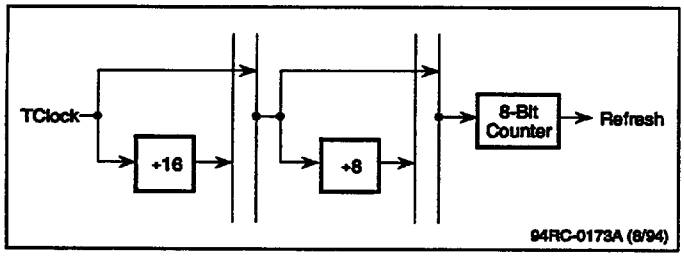


Figure 23. Refresh Counter Block Diagram



Refresh Timing

The 8-bit counter is used to count the refresh timing for DRAM or Sync DRAM. A 4-bit prescaler scales the divide-by-16 of TClock and an additional 3-bit prescaler (divide-by-8) provides the slow refresh function by setting bit 8. The prescalers can be bypassed with bit 9 set for testing purpose. See figure 23.

The refresh timing should be written into the refresh counter (bits 23-16) with the counting value equal to the desired number of clocks minus one. In bypass mode, the counting value written to the counter should be equal to the desired number of clocks minus two to ensure the read values are available one clock before the read response cycle.

The least significant 11 bits are valid and the most significant 53 bits are ignored in write cycle. In read cycle, the written value is read from the least significant 11 bits and the current count is read from the field. See table 17.

Table 17. Refresh Counter

63 — 24	23 — 16	15 — 11	10	9	8	7 — 0
—	Refresh counter	—	RE	CAS	SLO	Refresh timer

Field	Name	Description
23-16	Ref_Count	Refresh counter (Read only)
10	Ref_En	1: Refresh enable
9	B_P	Bypass prescaler
8	Slow_Ref	1: Enable slow refresh function
7-0	Ref_Timer	Refresh timer

Example 1. If 425H (Slow_Ref = 0, Ref_Timer = 37) is set in the refresh counter on 40-MHz system speed, the refresh timing is 25 ns (system speed) x 16 (divide-by-16) x (37+2) = 15,600 ns = 15.6 μs.

Example 2. If 412H (Slow_Ref = 1, Ref_Timer = 46) is set in the refresh counter on 50-MHz system speed, the refresh timing is 20 ns (system speed) x 16 (divide-by-16) x 8 (divide-by-8) x (46+2) = 122,880 ns = 122.88 μs.

DRAM Sleep Mode Control Register

The DRAM Sleep Mode Control register (table 18) is used to put the DRAM in sleep (self-refresh or standby) mode when the system is in standby mode. Once the DRAM is accessed during standby mode, the sleep mode will be cancelled automatically and will be set again in the next refresh cycle. The access time will be delayed by several clocks due to the DRAM precharge time when standby mode is cancelled.

Table 18. DRAM Sleep Mode Control Register

63 — 1	0
—	STB

Field	Name	Description
0	Set_Stby	1: Standby (self-refresh) mode; 0: Cancellation of standby mode

Secondary Cache Control Register

The Secondary Cache Control register (table 19) saves the control status of the cache operation. The least significant 7 bits are used for read and write. The most significant 57 bits are written with 0's on write and

ignored on read. All bits are set to 0 on reset. It cannot be enabled when working with VR4000SC/VR4400SC microprocessors.

Table 19. Secondary Cache Control Register

63 — 7	6	5 4	3	2	1	0
—	BSP	1SP	512		INV	STB

Field	Name	Description
6-5	B-Speed	Set the speed of the second-time and subsequent cache access 00: 1 Clock; 01: 2 Clock; 1: Reserved*
4-3	1st Speed	Set the speed of the second-time and subsequent cache access 00: 3 Clock; 01: 4 Clock; 1: Reserved*
2	512K	0: 256K; 1: 512K
1	Invalid*	0: Valid bits are set; 1: Invalid (all valid bits are reset to 0)
0	Cache Enable	0: Disable; 1: Enable

* Do not set a value for "Reserved"

Secondary Cache Flush Register

The Secondary Cache Flush register (table 20) is used to invalidate all the bits in a cache tag. The least significant 8 bits are valid on write and undefined on read. The most significant 58 bits are written with 0's on read and ignored on write. All bits are set to 0 on reset and line valid bits for all entries of the cache tag become invalid.

Table 20. Secondary Cache Flush Register

63 — 8	7 — 0
—	CFR

Field	Name	Description
7-0	CFR	0: Reset all (2048) LV (line valid) bits

Error Address Register

The Error Address register (table 21) holds the address where an ECC/parity error has occurred. If no error occurs, values in the register are undefined. If two or more errors occur, the address of the first error is held in the register. When a one-bit error occurs on ECC active, the device control register sets the correspondent bits to process the correction or generate an interrupt request based on the error address. The error flush register then discards the held address; undefined values are in the register until an error occurs again.

Table 21. Error Address Register

31 — 0
ERRADDR

Field	Name	Description
31-0	ERRADDR	Error address. The least significant 3 bits are 0.

Error Syndrome Register

The Error Syndrome register (table 22) holds the syndrome generated by ECC and error status. If no error occurs, values of bits 7-0 are undefined and bits 10-8 are 0. If two or more errors occur, the syndrome for the first error is held in the register. The error syndrome register will hold the insignificant data on a parity error. When a one-bit error occurs on ECC active, the device control register sets the correspondent bits to process the correction or generate an interrupt request. The error flush register discards the held error bits and continues the error detection.

Table 22. Error Syndrome Register

31 — 12	11	10	9	8	7 — 0
—	ILL	PER	ERR	ER1	ERR_SYN

Field	Name	Description
11	ILL	1: An illegal access is detected
10	PER	1: Parity error is detected on the SysAD bus when the Device Control register MSKERR bit = 0
9	ERR	1: An error is detected in memory when the Device Control register MSKERR bit = 0 and the MSKERR1 bit = 0
8	ER1	1: An uncorrectable error is detected in memory when the Device Control register MSKERR bit = 0
7-0	ERR_SYN	Syndrome bits for an error

Error Flush Register

Ther Error Flush register (table 23) flushes the contents of the error address register and the error syndrome register when the correspondent bits are set.

Table 23. Error Flush Register

31 — 8	7 — 0
—	ERFRR

Field	Name	Description
7-0	ERFRR	0: Discard the contents of the error address register and the error syndrome register Bit 3 = 1: ILL bit is cleared Bit 2 = 1: PER bit is cleared Bit 1 = 1: ERR bit is cleared Bit 0 = 1: ER1 bit is cleared

SysAD Bus Operation

All SysAD bus operations of the VR4x00 family of processors are supported by the RAB2IT-MEMC: word, partial word, doubleword and partial doubleword for read and write, block read/write, and read with write forthcoming,

Figures 24 through 32 are timing diagrams of the SysAD bus operations as follows:

- Register read/write: CPU accesses the -MEMC registers (figure 24)
- DRAM read: one -MEMC system (figure 25); Master/Slave mode of two -MEMC systems (figure 26)
- DRAM write: one -MEMC system (figure 27); Master/Slave mode of two -MEMC systems (figure 28)
- Secondary cache read hit on the VR4000PC, VR4400PC, or VR4200 system (figure 29)
- Read with write forthcoming cycles on the VR4400SC system (figure 30)
- Synchronous DRAM read (figure 31)
- Synchronous DRAM write (figure 32)

Figure 24. RAB2IT-MEMC Register Access

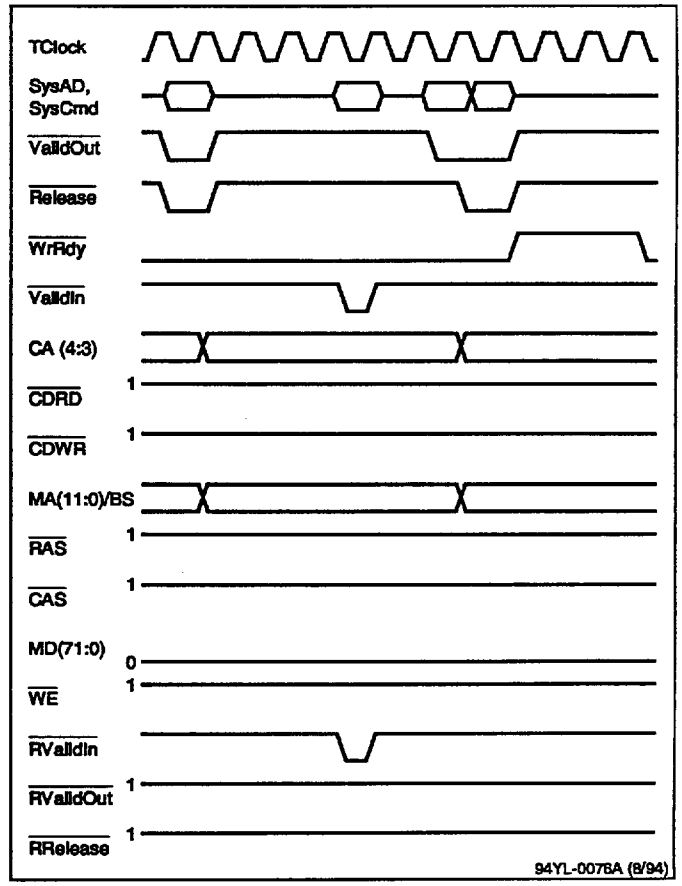


Figure 25. DRAM Read

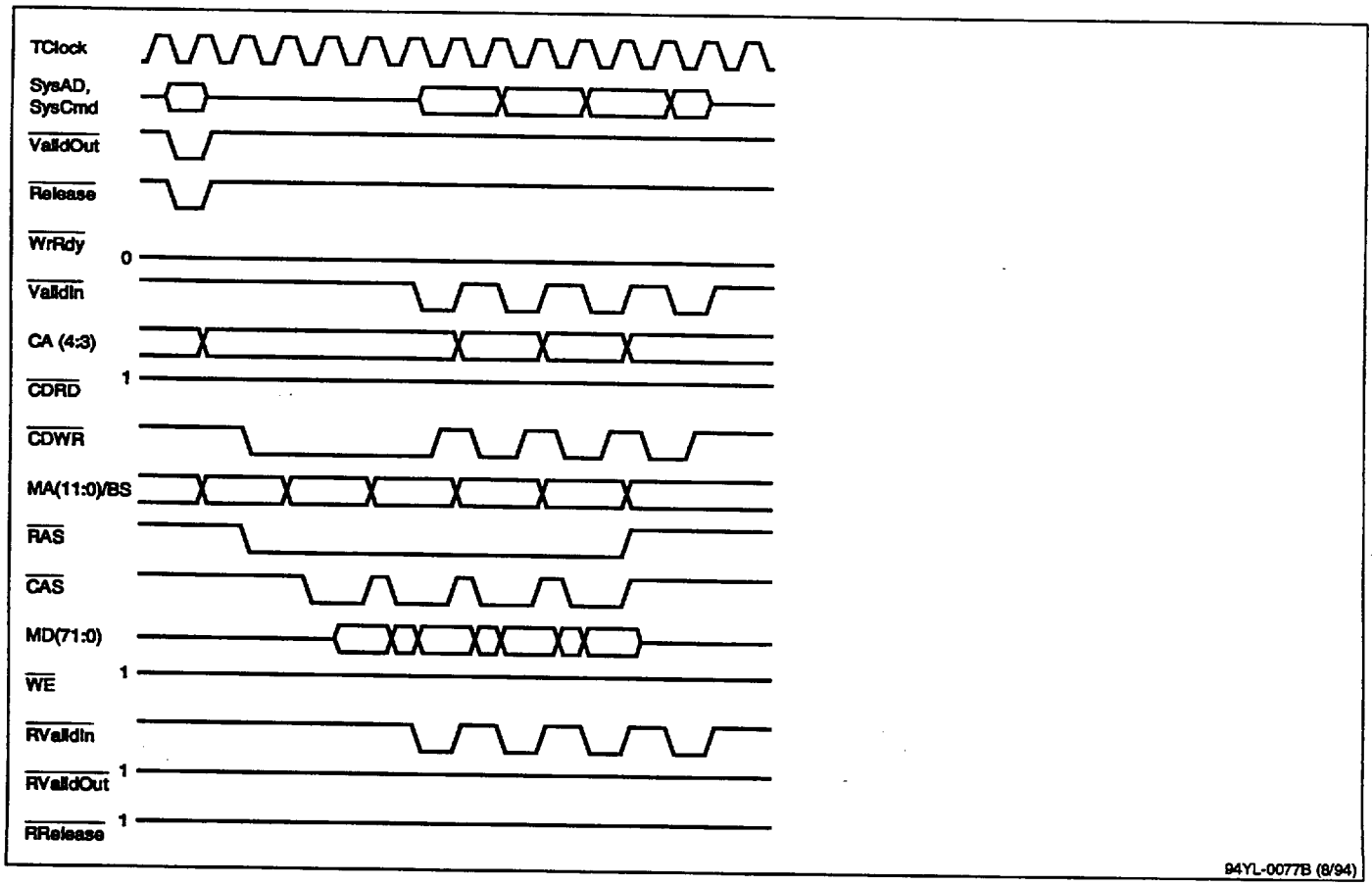


Figure 26. DRAM Read (Master/Slave Mode)

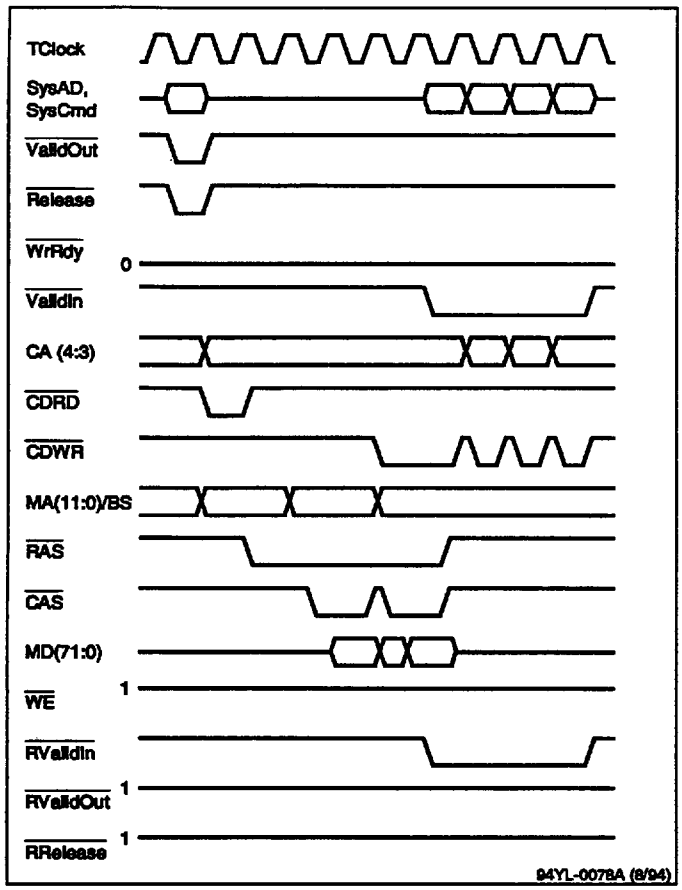


Figure 27. DRAM Write

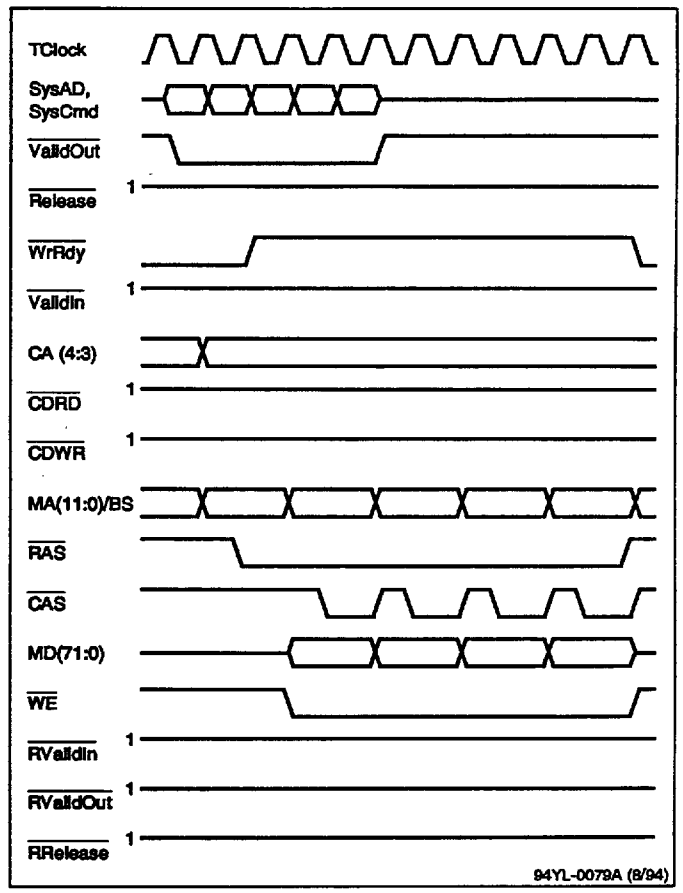


Figure 28. DRAM Write (Master/Slave Mode)

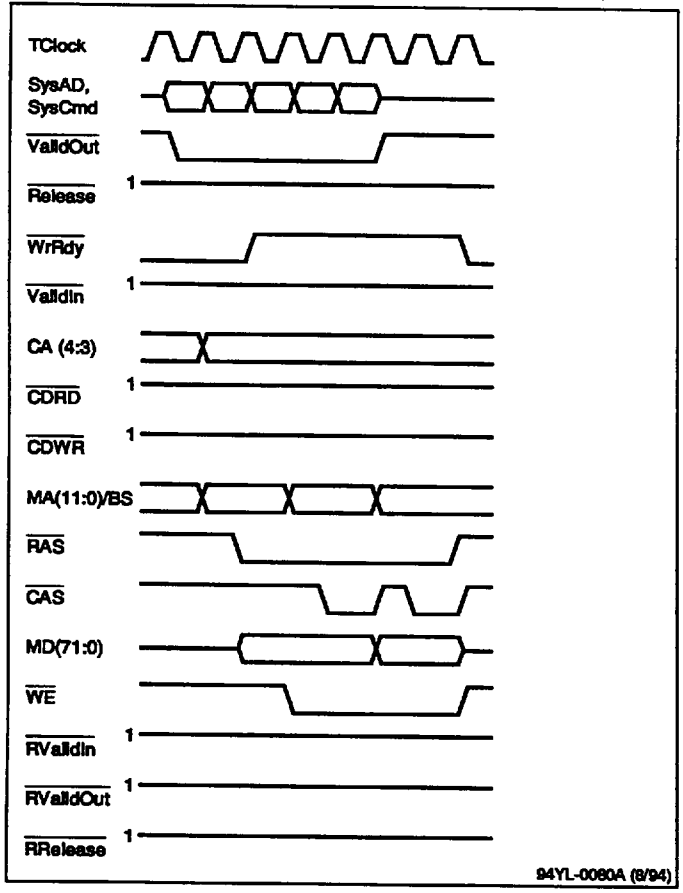


Figure 29. Cache Read Hit

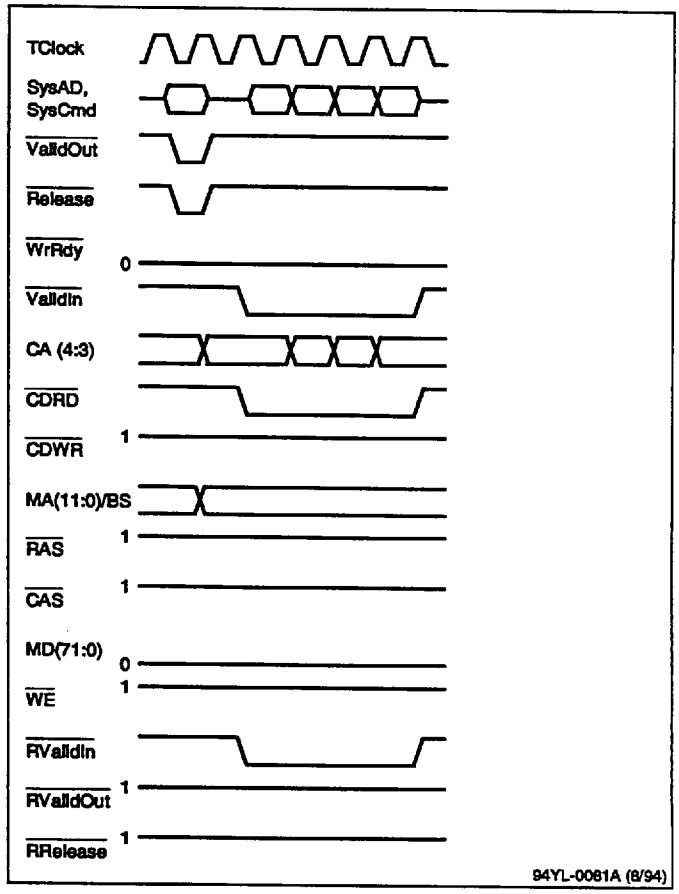


Figure 30. Read With Write Forthcoming Cycles (VR4400SC)

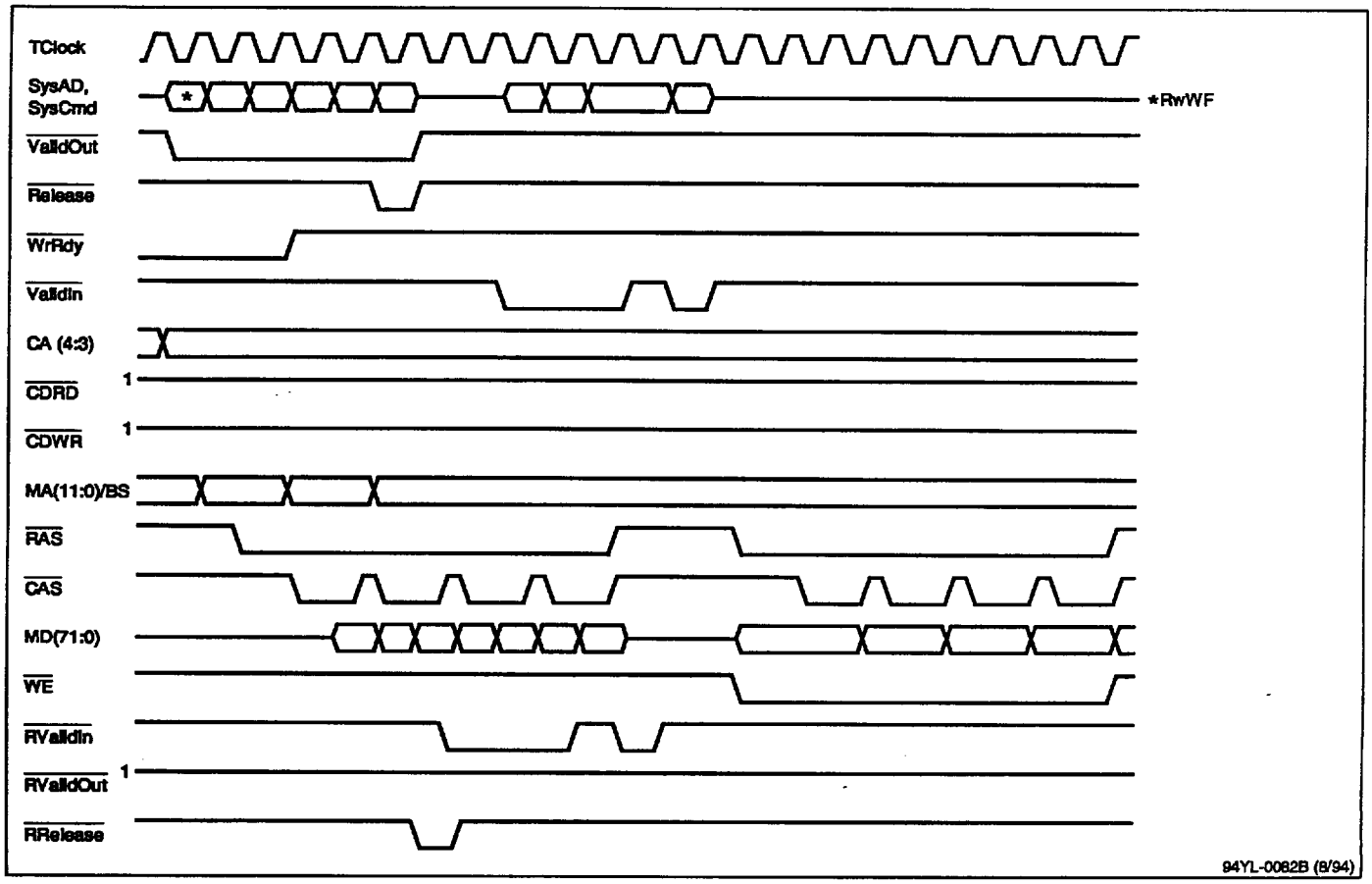


Figure 31. Synchronous DRAM Read (CAS Latency = 2)

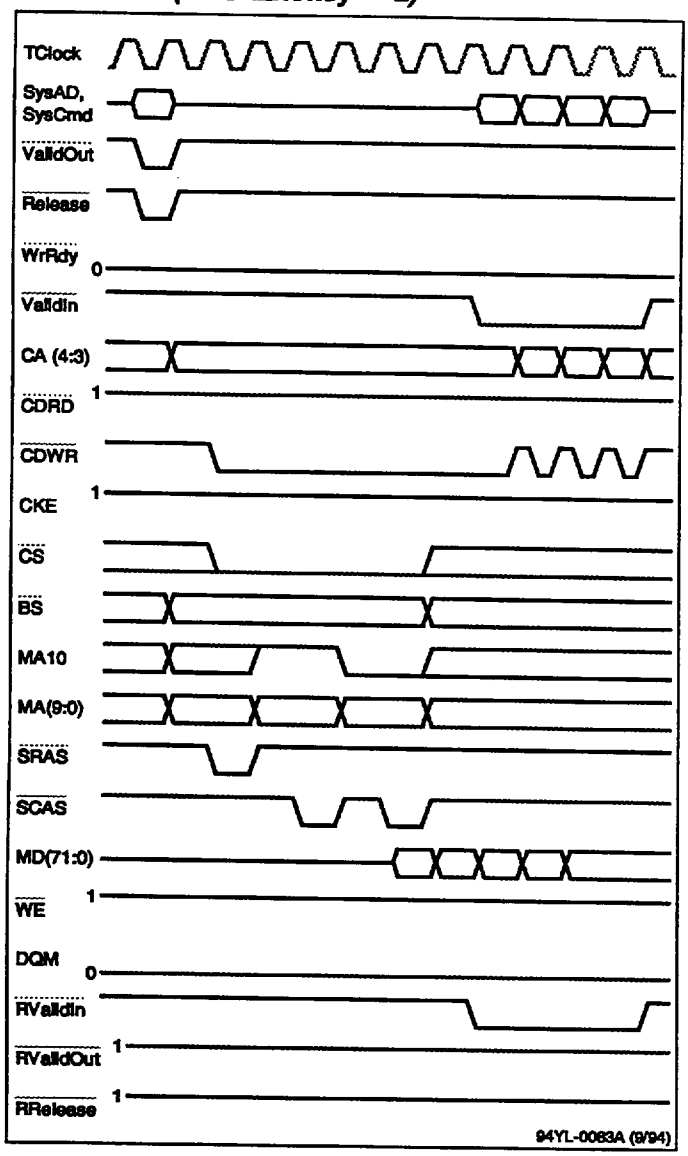
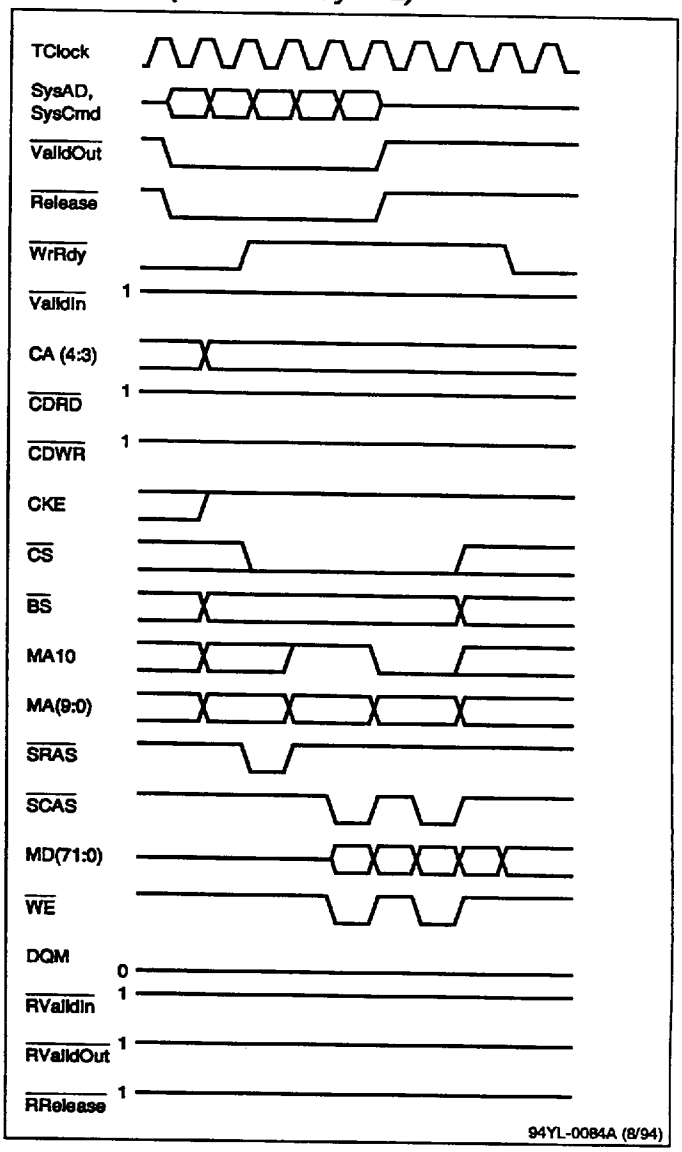


Figure 32. Synchronous DRAM Write (CAS Latency = 2)



ELECTRICAL SPECIFICATIONS

DC Characteristics

Functional operation range: V_{CC} = 3.3 V ±5%; T_C = 0 to +85°C

Parameter	Symbol	Min	Max	Unit	Conditions
CPU interface output voltage, high	V_{OHV}	2.4		V	V_{DD} = minimum; I_{OH} = −3 mA (Note 1)
Memory interface output voltage, high	V_{OHM}	2.4		V	V_{DD} = minimum; I_{OH} = −6 mA (Note 2)
Clock output voltage, high	V_{OHC}	2.7		V	V_{DD} = minimum; I_{OH} = −3 mA (Note 3)
CPU interface output voltage, low	V_{OLV}		0.4	V	V_{DD} = minimum; I_{OL} = 3 mA (Note 1)
Memory interface output voltage, low	V_{OLM}		0.4	V	V_{DD} = minimum; I_{OL} = 6 mA (Note 2)
Input voltage, high	V_{IH}	2.2	V_{DD} + 0.5	V	(Note 4)
Input voltage, low	V_{IL}	−0.5	0.8	V	(Notes 1, 4)
Clock input voltage, high	V_{IHC}	0.8 V_{DD}	V_{DD} + 0.5	V	(Note 5)
Clock input voltage, low	V_{ILC}	−0.5	0.2 V_{DD}	V	(Notes 1, 5)
Input leakage current, high	I_{LIH}		10	μA	V_{DD} = 3.6 V; V = V_{DD}
Input leakage current, low	I_{LIL}		−10	μA	V_{DD} = 3.6 V; V = 0 V
Output leakage current, high	I_{LOH}		20	μA	V_{DD} = 3.6 V; V = V_{DD}
Output leakage current, low	I_{LOL}		−20	μA	V_{DD} = 3.6 V; V = 0 V
Input capacitance	C_{IN}		10	pF	
Operating current	I_{DD}		TBD	mA	V_{DD} = 3.3 V; T_C = 0°C
Output capacitance	C_{OUT}		10	pF	

Notes:

(1) Valid for SysAd(63:0), SysADC(7:0), SysCmd(8:0), $\overline{\text{RValidIn}}$, WrRdy, ValidIn.

(2) Valid for MA(11:0), BS, MD(71:0), $\overline{\text{WE}}$, DQM/$\overline{\text{CAS}}$(3:0), $\overline{\text{CS}}$/$\overline{\text{RAS}}$(3:0), CKE, $\overline{\text{SRAS}}$, $\overline{\text{SCAS}}$, $\overline{\text{CDRD}}$, $\overline{\text{CDWR}}$.

(3) Applies to TClock and RClock outputs.

(4) Except for TClock and RClock inputs.

(5) Valid for TClock and RClock inputs.

AC Characteristics

Functional operation range: V_{CC} = 3.3 V ±5%; T_C = 0 to +85°C

Parameter	Symbol	Min	Max	Unit	Conditions
TClock/RClock period	t_{CkP}	15		ns	Transition ≤ 5 ns
TClock/RClock high	t_{CkLow}	3		ns	Transition ≤ 5 ns
TClock/RClock rise time	t_{CkRise}		4	ns	
TClock/RClock fall time	t_{CkFall}		4	ns	
Reset pulse	t_{LRST}	10		TClock	
CPU data output delay	t_{DOVR}	2	8	ns	
CPU data floating delay	t_{DOVR}	2	8	ns	
CPU data setup time	t_{DSVR}	3		ns	
CPU data hold time	t_{DHVR}	2		ns	
Memory interface data, output delay	t_{DOM}	2	8	ns	
Memory interface data, floating delay	t_{DOM}	2	8	ns	
Memory interface data, setup time	t_{DSM}	3		ns	
Memory interface	t_{DHM}	2		ns	

Notes:

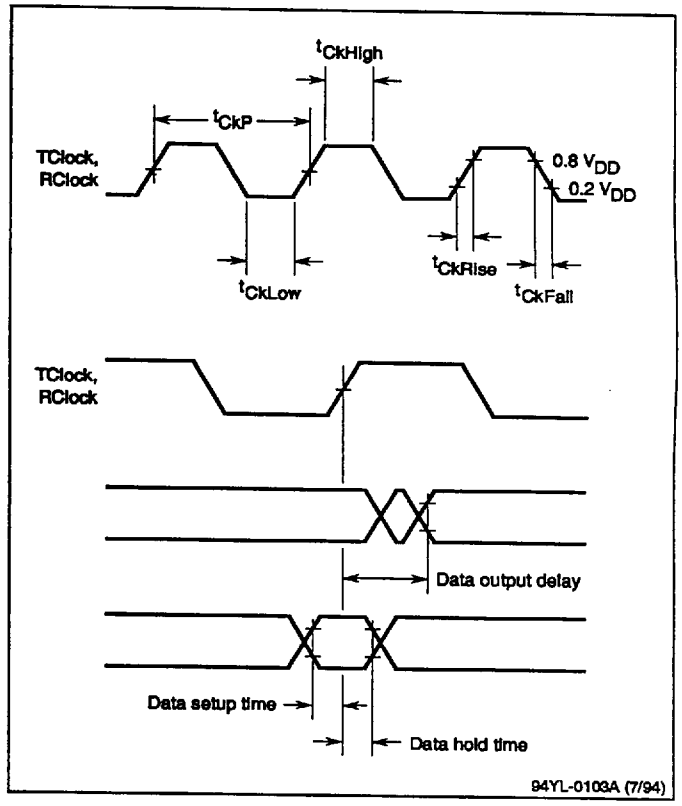
(1) Timing is measured from 1.5 V of TClock or RClock to 1.5 V of the signal.

(2) Capacitive load for all output signals but Status is 50 pF.

(3) Capacitive load derating is 2 ns/25 pF maximum.

(4) RClock and TClock for timing reference.

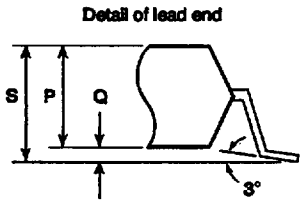
Figure 33. TClock and RClock

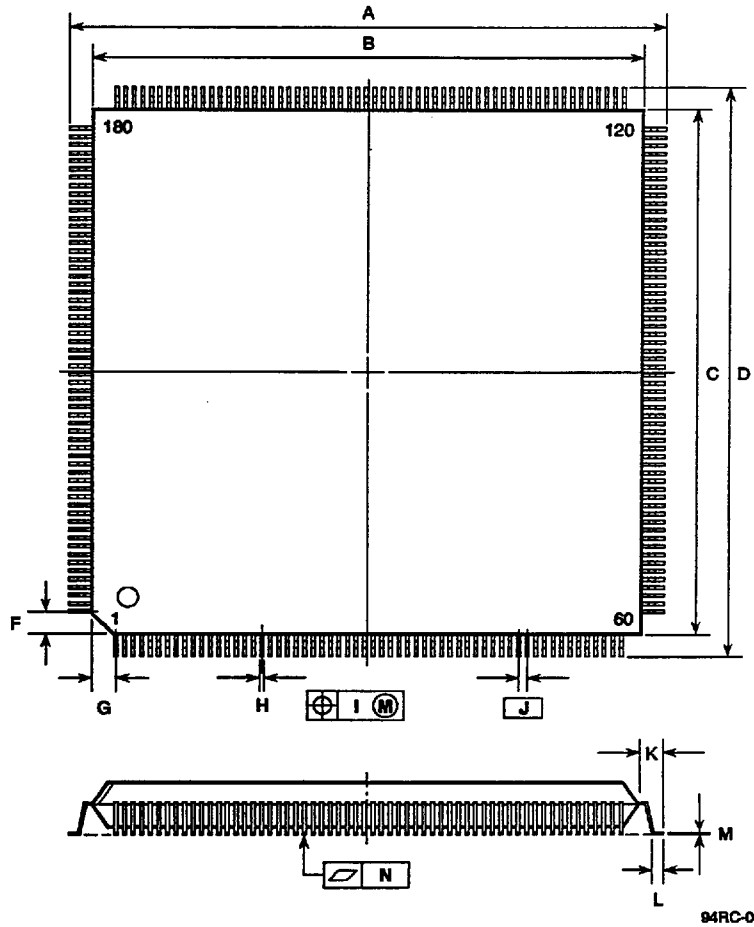


PACKAGE DRAWINGS

240-Pin PQFP

Item	Millimeters	Inches
A	34.6 ± 0.3	1.362 ± .012
B	32.0 ± 0.2	1.260 ± .008
C	32.0 ± 0.2	1.260 ± .008
D	34.6 ± 0.3	1.362 ± .012
F	1.25	.049
G	1.25	.049
H	0.20 ± 0.10	.008 ± .004
I	0.08	.003
J	0.5 (TP)	.020 (TP)
K	1.3 ± 0.2	.051 ± .008
L	0.5 ± 0.2	.020 $^{+.009}_{-.008}$
M	0.15 ± 0.05	.006 ± .002
N	0.10	.004
P	3.2	.126
Q	0.4 ± 0.1	.016 $^{+.004}_{-.005}$
S	3.8 max	.150 max





P240GN-50-LMU

94RC-0068B (6/94)