165-Bump BGA
Commercial Temp
Industrial Temp

18Mb Burst of 4 SigmaQuad SRAM

250 MHz–100 MHz
2.5 V V_{DD}
1.8 V or 1.5 V I/O

Features

- Simultaneous Read and Write SigmaQuad™ Interface
- JEDEC-standard pinout and package
- Dual DoubleData Rate interface
- Byte Write controls sampled at data-in time
- Burst of 4 Read and Write
- 2.5 V +100/–100 mV core power supply
- 1.5 V or 1.8 V HSTL Interface
- Pipelined read operation
- Fully coherent read and write pipelines
- ZQ mode pin for programmable output drive strength
- IEEE 1149.1 JTAG-compliant Boundary Scan
- 165-bump, 13 mm x 15 mm, 1 mm bump pitch BGA package
- Pin-compatible with future 36Mb, 72Mb, and 144Mb devices

SigmaRAM™ Family Overview

GS8180DV18 are built in compliance with the SigmaQuad SRAM pinout standard for Separate I/O synchronous SRAMs. They are18,874,368-bit (18Mb) SRAMs. These are the first in a family of wide, very low voltage HSTL I/O SRAMs designed to operate at the speeds needed to implement economical high performance networking systems.

SigmaQuad SRAMs are offered in a number of configurations. Some emulate and enhance other synchronous separate I/O SRAMs. A higher performance SDR (Single Data Rate) Burst of 2 version is also offered. The logical differences between the protocols employed by these RAMs hinge mainly on various combinations of address bursting, output data registering, and write cueing. Along with the Common I/O family of SigmaRAMs, the SigmaQuad family of SRAMs allows a user to implement the interface protocol best suited to the task at hand.

Clocking and Addressing Schemes

A Burst of 4 SigmaQuad SRAM is a synchronous device. It employs two input register clock inputs, K and $\overline{K}$. K and $\overline{K}$ are independent single-ended clock inputs, not differential inputs to a single differential clock input buffer. The device also allows the user to manipulate the output register clock inputs quasi independently with the C and $\overline{C}$ clock inputs. C and $\overline{C}$ are also independent single-ended clock inputs, not differential inputs. If the C clocks are tied high, the K clocks are routed internally to fire the output registers instead.

Because Separate I/O Burst of 4 RAMs always transfer data in four packets, A0 and A1 are internally set to 0 for the first read or write transfer, and automatically incremented by 1 for the next transfers. Because the LSBs are tied off internally, the address field of a Burst of 4 RAM is always two address pins less than the advertised index depth (e.g., the 1M x 18 has a 256K addressable index).

Parameter Synopsis

	-250	-200	-167	-133	-100
tKHKH	4.0 ns	5.0 ns	6.0 ns	7.5 ns	10 ns
tKHQV	2.1 ns	2.3 ns	2.5 ns	3.0 ns	3.0 ns

1M x 18 SigmaQuad SRAM—Top View (Package D)

	1	2	3	4	5	6	7	8	9	10	11
A	NC	MCL/SA (144Mb)	NC/SA (36Mb)	$\overline{W}$	$\overline{BW1}$	$\overline{K}$	NC	$\overline{R}$	SA	MCL/SA (72Mb)	NC
B	NC	Q9	D9	SA	NC	K	$\overline{BW0}$	SA	NC	NC	Q8
C	NC	NC	D10	V_{SS}	SA	NC	SA	V_{SS}	NC	Q7	D8
D	NC	D11	Q10	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	NC	NC	D7
E	NC	NC	Q11	V_{DDQ}	V_{SS}	V_{SS}	V_{SS}	V_{DDQ}	NC	D6	Q6
F	NC	Q12	D12	V_{DDQ}	V_{DD}	V_{SS}	V_{DD}	V_{DDQ}	NC	NC	Q5
G	NC	D13	Q13	V_{DDQ}	V_{DD}	V_{SS}	V_{DD}	V_{DDQ}	NC	NC	D5
H	NC	V_{REF}	V_{DDQ}	V_{DDQ}	V_{DD}	V_{SS}	V_{DD}	V_{DDQ}	V_{DDQ}	V_{REF}	ZQ
J	NC	NC	D14	V_{DDQ}	V_{DD}	V_{SS}	V_{DD}	V_{DDQ}	NC	Q4	D4
K	NC	NC	Q14	V_{DDQ}	V_{DD}	V_{SS}	V_{DD}	V_{DDQ}	NC	D3	Q3
L	NC	Q15	D15	V_{DDQ}	V_{SS}	V_{SS}	V_{SS}	V_{DDQ}	NC	NC	Q2
M	NC	NC	D16	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	NC	Q1	D2
N	NC	D17	Q16	V_{SS}	SA	SA	SA	V_{SS}	NC	NC	D1
P	NC	NC	Q17	SA	SA	C	SA	SA	NC	D0	Q0
R	TDO	TCK	SA	SA	SA	$\overline{C}$	SA	SA	SA	TMS	TDI

11 x 15 Bump BGA—13 x 15 mm2 Body—1 mm Bump Pitch

Notes:

1. Expansion addresses: A3 for 36Mb, A10 for 72Mb, A2 for 144Mb
2. $\overline{BW0}$ controls writes to D0:D8. $\overline{BW1}$ controls writes to D9:D17.
3. MCL = Must Connect Low
4. It is recommended that H1 be tied low for compatibility with future devices.

Pin Description Table

Symbol	Description	Type	Comments
SA	Synchronous Address Inputs	Input	—
NC	No Connect	—	—
$\overline{R}$	Synchronous Read	Input	Active Low
$\overline{W}$	Synchronous Write	Input	Active Low
$\overline{BW0}$–$\overline{BW1}$	Synchronous Byte Writes	Input	Active Low
K	Input Clock	Input	Active High
$\overline{K}$	Input Clock	Input	Active Low
C	Output Clock	Input	Active High
$\overline{C}$	Output Clock	Input	Active Low
TMS	Test Mode Select	Input	—
TDI	Test Data Input	Input	—
TCK	Test Clock Input	Input	—
TDO	Test Data Output	Output	—
V_{REF}	HSTL Input Reference Voltage	Input	—
ZQ	Output Impedance Matching Input	Input	—
MCL	Must Connect Low	—	—
D0–D17	Synchronous Data Inputs	Input	—
Q0–Q17	Synchronous Data Outputs	Output	—
V_{DD}	Power Supply	Supply	2.5 V Nominal
V_{DDQ}	Isolated Output Buffer Supply	Supply	1.8 or 1.5 V Nominal
V_{SS}	Power Supply: Ground	Supply	—

Note:
NC = Not Connected to die or any other pin

Background

Separate I/O SRAMs, from a system architecture point of view, are attractive in applications where alternating reads and writes are needed. Therefore, the SigmaQuad SRAM interface and truth table are optimized for alternating reads and writes. Separate I/O SRAMs are unpopular in applications where multiple reads or multiple writes are needed because burst read or write transfers from Separate I/O SRAMs can cut the RAM's bandwidth in half.

A SigmaQuad SRAM can begin an alternating sequence of reads and writes with either a read or a write. In order for any separate I/O SRAM that shares a common address between its two ports to keep both ports running all the time, the RAM must implement some sort of burst transfer protocol. The burst must be at least long enough to cover the time the opposite port is receiving instructions on what to do next. The rate at which a RAM can accept a new random address is the most fundamental performance metric for the RAM. Each of the three SigmaQuad SRAMs support similar address rates because random address rate is determined by the internal performance of the RAM and they are all based on the same internal circuits. Differences between the truth tables of the different SigmaQuad SRAMs, or any other Separate I/O SRAMs, follow from differences in how the RAM's

interface is contrived to interact with the rest of the system. Each mode of operation has its own advantages and disadvantages. The user should consider the nature of the work to be done by the RAM to evaluate which version is best suited to the application at hand.

Alternating Read-Write Operations

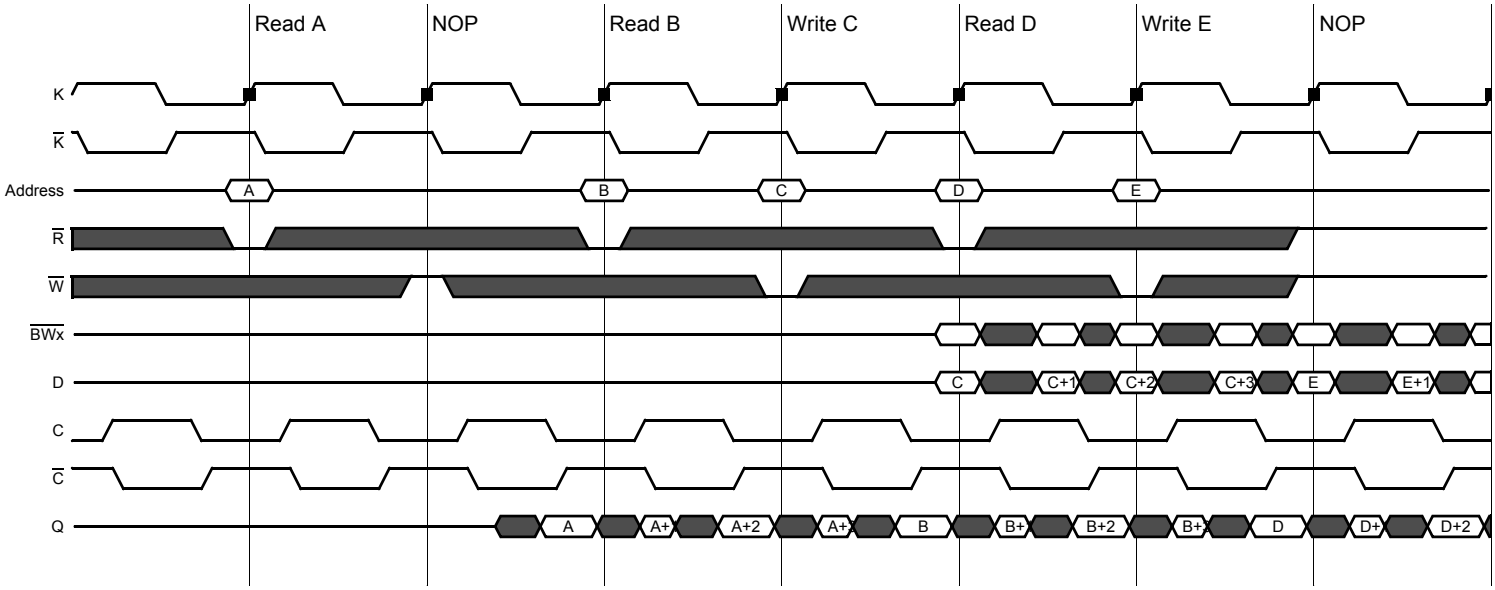
SigmaQuad SRAMs follow a few simple rules of operation.
- Read or Write commands issued on one port are never allowed to interrupt an operation in progress on the other port.
- Read or Write data transfers in progress may not be interrupted and re-started.
- $\overline{R}$ and $\overline{W}$ high always deselects the RAM.
- All address, data, and control inputs are sampled on clock edges.

In order to enforce these rules, each RAM combines present state information with command inputs. See the Truth Table for details.

Burst of 4 SigmaQuad SRAM DDR Read

The status of the Address Input, $\overline{W}$, and $\overline{R}$ pins are sampled at each rising edge of K. $\overline{W}$ and $\overline{R}$ high causes chip disable. A low on the Read Enable-bar pin, $\overline{R}$, begins a read cycle. $\overline{R}$ is always ignored if the previous command loaded was a read command. The four resulting data output transfers begin after the next rising edge of the K clock. Data is clocked out by the next rising edge of the C, the rising edge of $\overline{C}$ after that, the next rising edge of C, and finally by the next rising edge of $\overline{C}$.

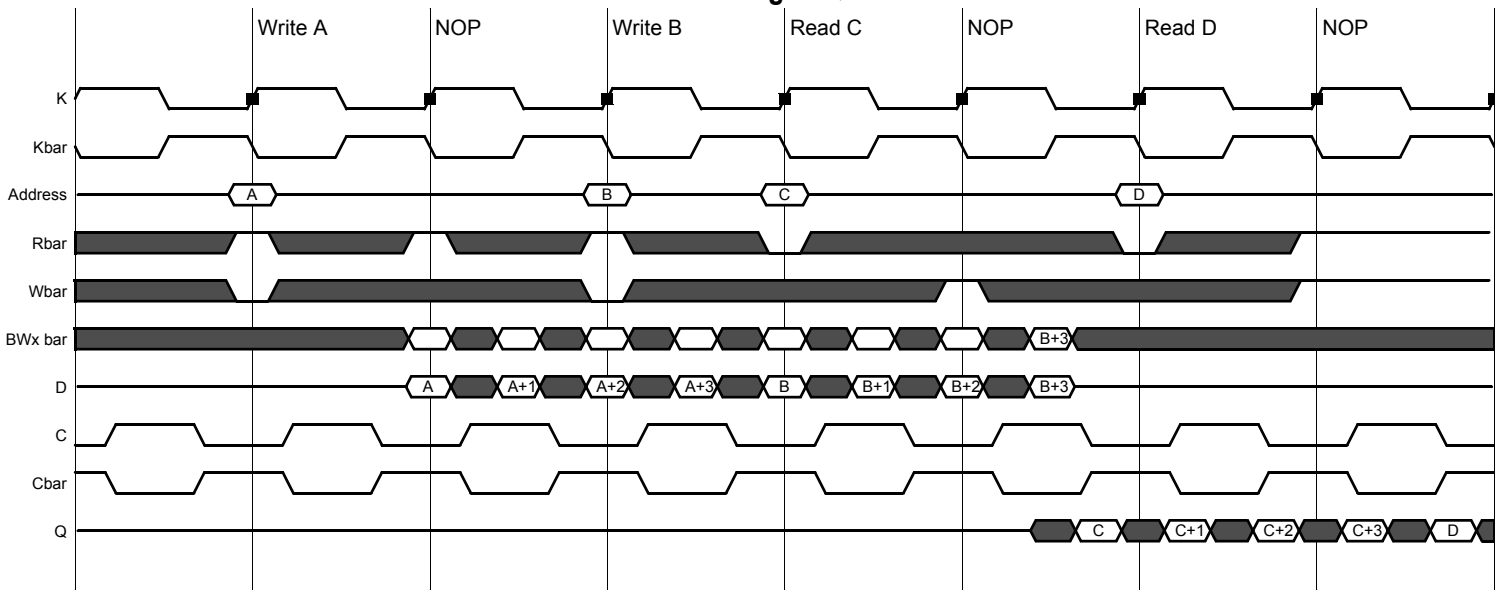
Burst of 4 Double Data Rate SigmaQuad SRAM Read First



Burst of 4 SigmaQuad SRAM DDR Write

The status of the Address Input, $\overline{W}$, and $\overline{R}$ pins are sampled at each rising edge of K. $\overline{W}$ and $\overline{R}$ high causes chip disable. A low on the Write Enable-bar pin, $\overline{W}$, and a high on the Read Enable-bar pin, $\overline{R}$, begins a write cycle. $\overline{W}$ is always ignored if the previous command was a write command. Data is clocked in by the next rising edge of K, the rising edge of $\overline{K}$ after that, the next rising edge of K, and finally by the next rising edge of $\overline{K}$.

Burst of 4 Double Data Rate SigmaQuad SRAM Write First



Special Functions

Byte Write Control

Byte Write Enable pins are sampled at the same time that Data In is sampled. A high on the Byte Write Enable pin associated with a particular byte (e.g., $\overline{BW0}$ controls D0–D8 inputs) will inhibit the storage of that particular byte, leaving whatever data may be stored at the current address at that byte location undisturbed. Any or all of the Byte Write Enable pins may be driven high or low during the data in sample times in a write sequence.

Each write enable command and write address loaded into the RAM provides the base address for a 4 beat data transfer. The x18 version of the RAM, for example, may write 72 bits in association with each address loaded. Any 9-bit byte may be masked in any write sequence.

Example x18 RAM Write Sequence using Byte Write Enables

Data In Sample Time	$\overline{BW0}$	$\overline{BW1}$	D0–D8	D9–D17
Beat 1	0	1	Data In	Don't Care
Beat 2	1	0	Don't Care	Data In
Beat 3	0	0	Data In	Data In
Beat 4	1	0	Don't Care	Data In

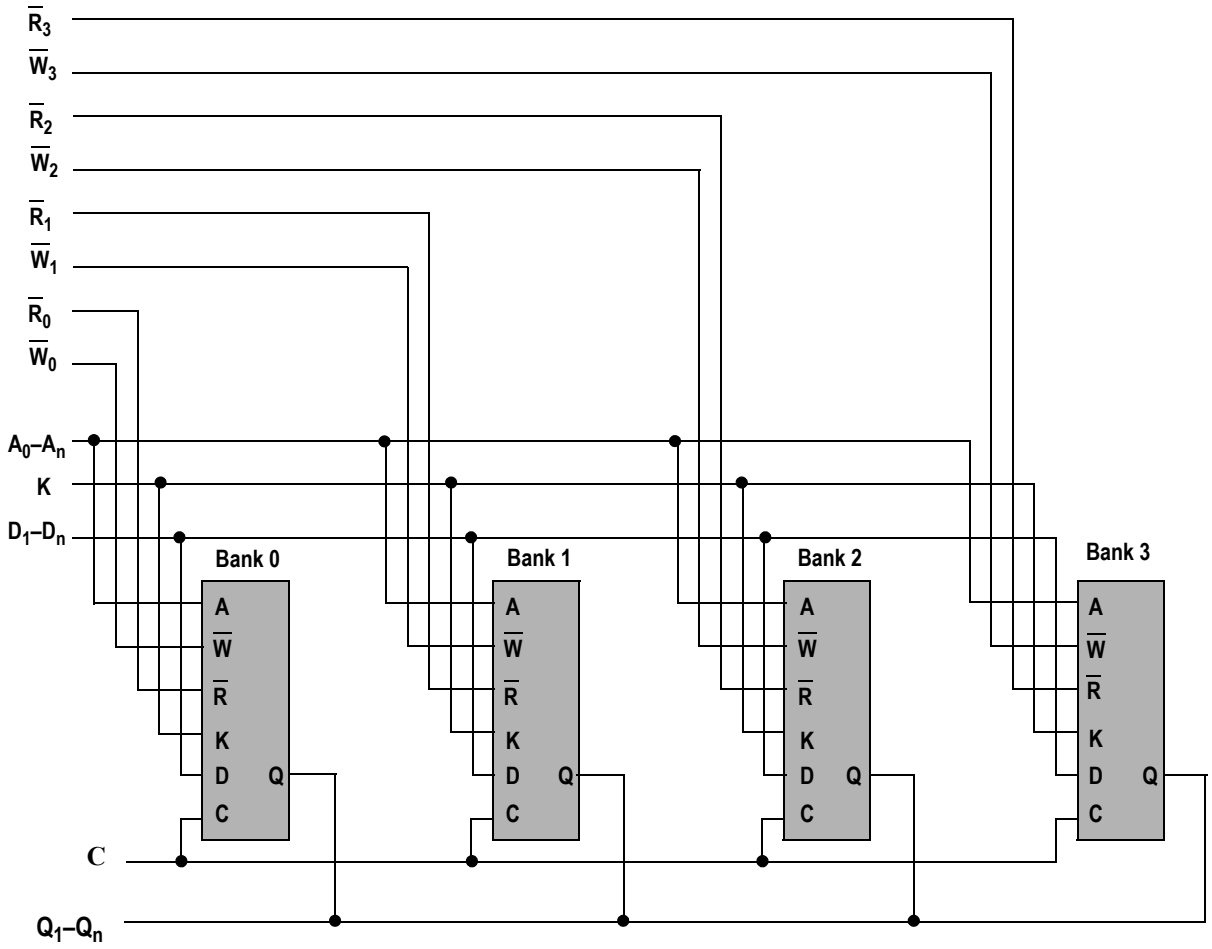
Resulting Write Operation

Beat 1 D0–D8	Beat 1 D9–D17	Beat 2 D0–D8	Beat 2 D9–D17	Beat 3 D0–D8	Beat 3 D9–D17	Beat 4 D0–D8	Beat 4 D9–D17
Written	Unchanged	Unchanged	Written	Written	Written	Unchanged	Written

Output Register Control

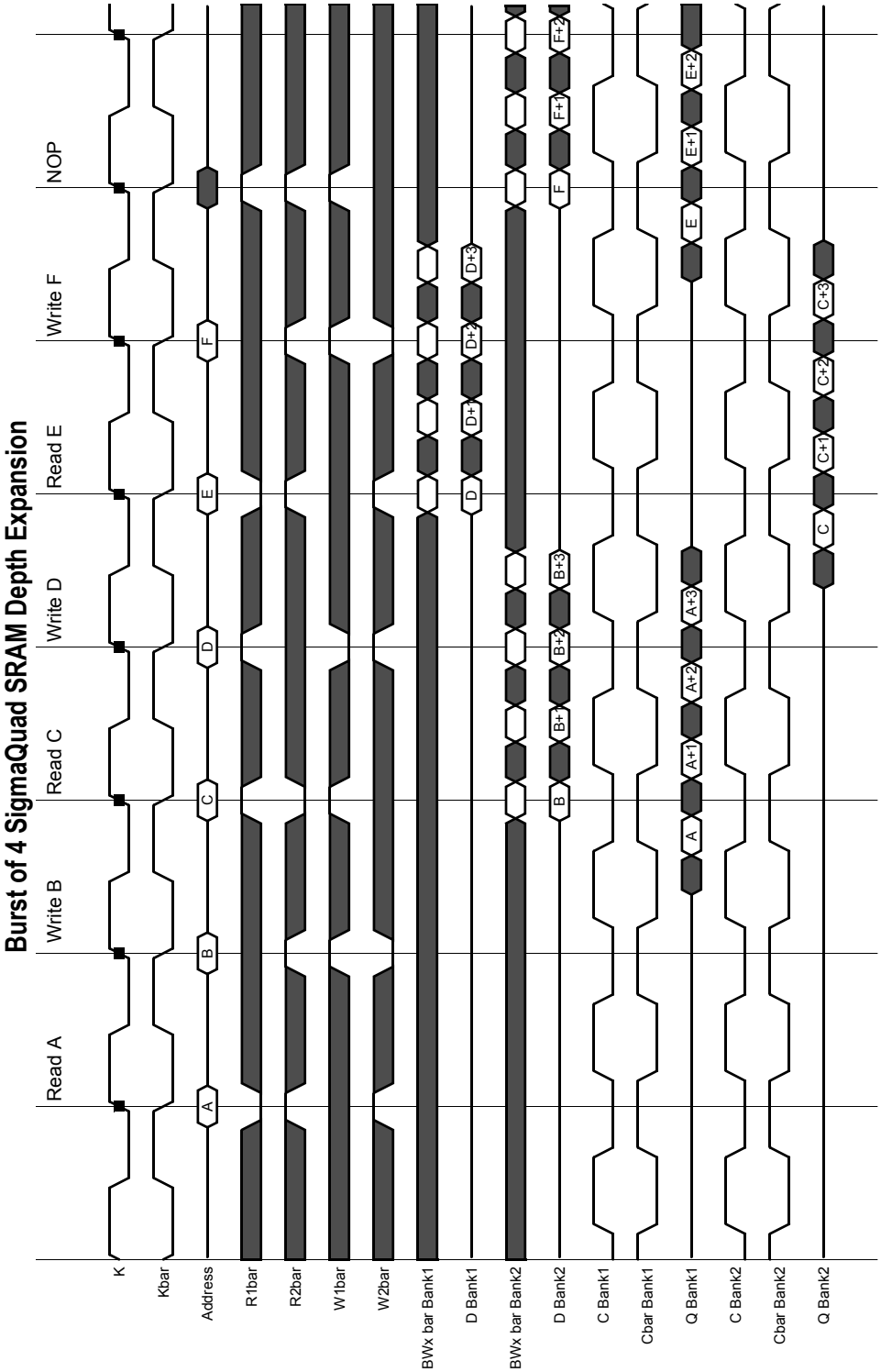
SigmaQuad SRAMs offer two mechanisms for controlling the output data registers. Typically, control is handled by the Output Register Clock inputs, C and $\overline{C}$. The Output Register Clock inputs can be used to make small phase adjustments in the firing of the output registers by allowing the user to delay driving data out as much as a few nanoseconds beyond the next rising edges of the K and $\overline{K}$ clocks. If the C and $\overline{C}$ clock inputs are tied high, the RAM reverts to K and $\overline{K}$ control of the outputs, allowing the RAM to function as a conventional pipelined read SRAM.

Example Four Bank Depth Expansion Schematic



Note: For simplicity $\overline{BWn}$, $\overline{K}$, and $\overline{C}$ are not shown.

Burst of 4 SigmaQuad SRAM Depth Expansion



FLXDrive-II Output Driver Impedance Control

HSTL I/O SigmaQuad SRAMs are supplied with programmable impedance output drivers. The ZQ pin must be connected to V_{SS} via an external resistor, RQ, to allow the SRAM to monitor and adjust its output driver impedance. The value of RQ must be 5X the value of the intended line impedance driven by the SRAM. The allowable range of RQ to guarantee impedance matching with a vendor-specified tolerance is between 150Ω and 300Ω. Periodic readjustment of the output driver impedance is necessary as the impedance is affected by drifts in supply voltage and temperature. A clock cycle counter periodically triggers an impedance evaluation, resets and counts again. Each impedance evaluation may move the output driver impedance level one step at a time towards the optimum level. The output driver is implemented with discrete binary weighted impedance steps. The SRAM requires 32K start-up cycles, selected or deselected, after V_{DD} reaches its operating range to reach its programmed output driver impedance.

Separate I/O Burst of 4 SigmaQuad SRAM Truth Table

A	$\overline{R}$	$\overline{W}$	Previous Operation	Current Operation	D	D	D	D	Q	Q	Q	Q
K↑ (t_n)	K↑ (t_n)	K↑ (t_n)	K↑ (t_{n-1})	K↑ (t_n)	K↑ (t_{n+1})	$\overline{K}$↑ ($t_{n+1½}$)	K↑ (t_{n+2})	$\overline{K}$↑ ($t_{n+2½}$)	K↑ (t_{n+1})	$\overline{K}$↑ ($t_{n+1½}$)	K↑ (t_{n+2})	$\overline{K}$↑ ($t_{n+2½}$)
X	1	1	Deselect	Deselect	X	X	—	—	Hi-Z	Hi-Z	—	—
X	1	X	Write	Deselect	D2	D3	—	—	Hi-Z	Hi-Z	—	—
X	X	1	Read	Deselect	X	X	—	—	Q2	Q3	—	—
V	1	0	Deselect	Write	D0	D1	D2	D3	Hi-Z	Hi-Z	—	—
V	0	X	Deselect	Read	X	X	—	—	Q0	Q1	Q2	Q3
V	X	0	Read	Write	D0	D1	D2	D3	Q2	Q3	—	—
V	0	X	Write	Read	D2	D3	—	—	Q0	Q1	Q2	Q3

Notes:

1. "1" = input "high"; "0" = input "low"; "V" = input "valid"; "X" = input "don't care"
2. "—" indicates that the input requirement or output state is determined by the next operation.
3. Q0, Q1, Q2, and Q3 indicate the first, second, third, and fourth pieces of output data transferred during Read operations.
4. D0, D1, D2, and D3 indicate the first, second, third, and fourth pieces of input data transferred during Write operations.
5. Qs are tristated for one cycle in response to Deselect and Write commands, one cycle after the command is sampled, except when preceded by a Read command.
6. Users should not clock in metastable addresses.

Byte Write Clock Truth Table

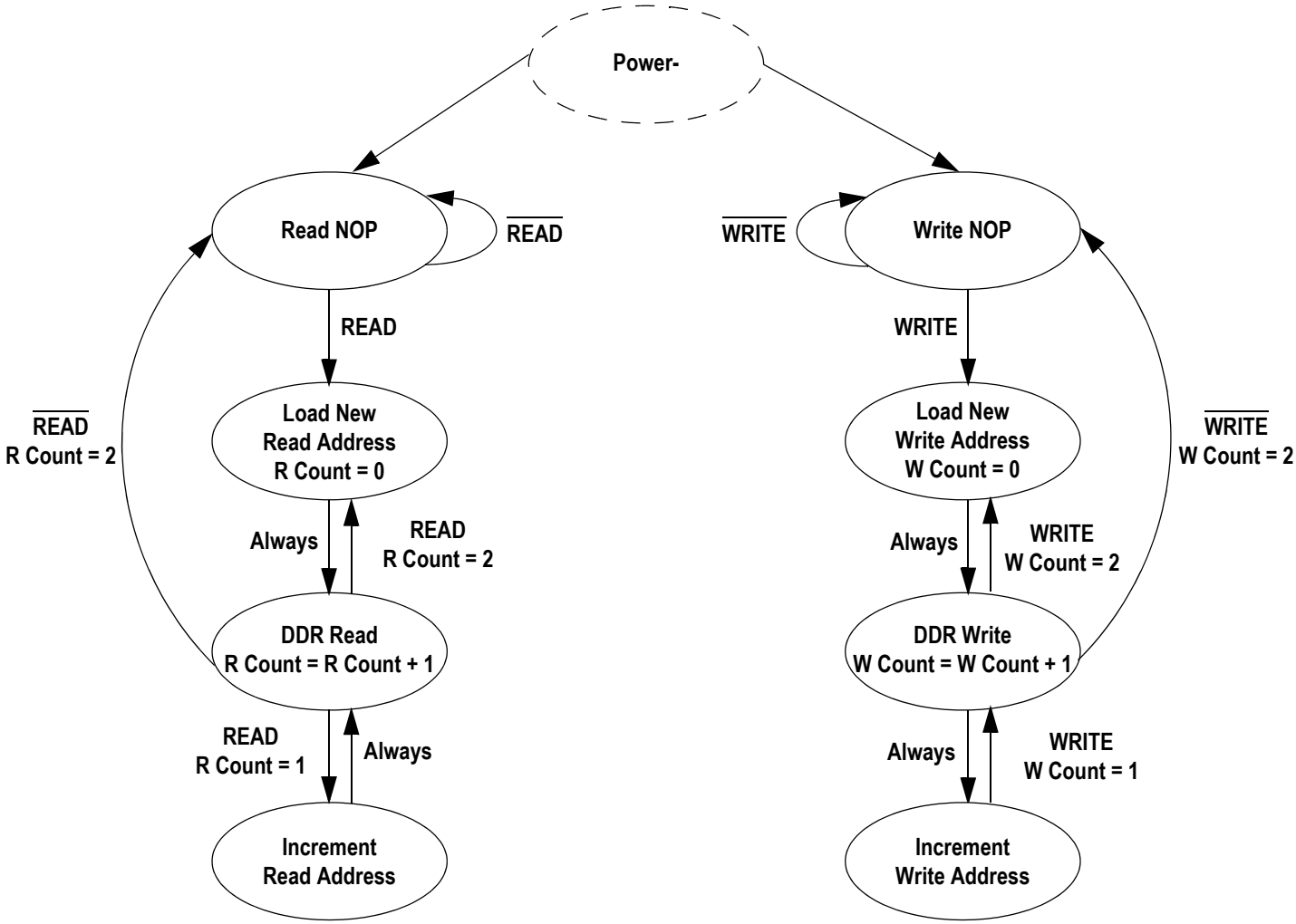
$\overline{BW}$	$\overline{BW}$	$\overline{BW}$	$\overline{BW}$	Current Operation	D	D	D	D
K ↑ (t_{n+1})	$\overline{K}$ ↑ ($t_{n+1½}$)	K ↑ (t_{n+2})	$\overline{K}$ ↑ ($t_{n+2½}$)	K ↑ (t_n)	K ↑ (t_{n+1})	$\overline{K}$ ↑ ($t_{n+1½}$)	K ↑ (t_{n+2})	$\overline{K}$ ↑ ($t_{n+2½}$)
T	T	T	T	Write Dx stored if $\overline{BWn}$ = 0 in all four data transfers	D0	D2	D3	D4
T	F	F	F	Write Dx stored if $\overline{BWn}$ = 0 in 1st data transfer only	D0	X	X	X
F	T	F	F	Write Dx stored if $\overline{BWn}$ = 0 in 2nd data transfer only	X	D1	X	X
F	F	T	F	Write Dx stored if $\overline{BWn}$ = 0 in 3rd data transfer only	X	X	D2	X
F	F	F	T	Write Dx stored if $\overline{BWn}$ = 0 in 4th data transfer only	X	X	X	D3
F	F	F	F	Write Abort No Dx stored in any of the four data transfers	X	X	X	X

Notes:
1. "1" = input "high"; "0" = input "low"; "X" = input "don't care"; "T" = input "true"; "F" = input "false".
2. If one or more $\overline{BWn}$ = 0, then $\overline{BW}$ = "T", else $\overline{BW}$ = "F".

x18 Byte Write Enable ($\overline{BWn}$) Truth Table

$\overline{BW0}$	$\overline{BW1}$	D0–D8	D9–D17
1	1	Don't Care	Don't Care
0	1	Data In	Don't Care
1	0	Don't Care	Data In
0	0	Data In	Data In

State Diagram



Notes:

1. Internal burst counter is fixed as 2-bit linear (i.e., when first address is A0+), next internal burst address is A0+1.
2. "READ" refers to read active status with $\overline{R}$ = Low, "$\overline{READ}$" refers to read inactive status with $\overline{R}$ = High. The same is true for "WRITE" and "$\overline{WRITE}$".
3. Read and write state machine can be active simultaneously.
4. State machine control timing sequence is controlled by K.
5. R Count is the read counter; Burst of 4 must complete 2 DDR reads.
6. W Count is the write counter; Burst of 4 must complete 2 DDR writes.

Absolute Maximum Ratings

(All voltages reference to V_{SS})

Symbol	Description	Value	Unit
V_{DD}	Voltage on V_{DD} Pins	–0.5 to 3.6	V
V_{DDQ}	Voltage in V_{DDQ} Pins	–0.5 to 3.6	V
V_{REF}	Voltage in V_{REF} Pins	–0.5 to V_{DDQ}	V
$V_{I/O}$	Voltage on I/O Pins	–0.5 to V_{DDQ} +0.5 (≤ 3.6 V max.)	V
V_{IN}	Voltage on Other Input Pins	–0.5 to V_{DDQ} +0.5 (≤ 3.6 V max.)	V
I_{IN}	Input Current on Any Pin	+/–100	mA dc
I_{OUT}	Output Current on Any I/O Pin	+/–100	mA dc
T_J	Maximum Junction Temperature	125	°C
T_{STG}	Storage Temperature	–55 to 125	°C

Note:
Permanent damage to the device may occur if the Absolute Maximum Ratings are exceeded. Operation should be restricted to Recommended Operating Conditions. Exposure to conditions exceeding the Recommended Operating Conditions, for an extended period of time, may affect reliability of this component.

Recommended Operating Conditions

Power Supplies

Parameter	Symbol	Min.	Typ.	Max.	Unit	Notes
Supply Voltage	V_{DD}	2.4	2.5	2.6	V	
1.8 V I/O Supply Voltage	V_{DDQ}	1.7	1.8	1.95	V	1
1.5 V I/O Supply Voltage	V_{DDQ}	1.4	1.5	1.6	V	1
Ambient Temperature (Commercial Range Versions)	T_A	0	25	70	°C	2
Ambient Temperature (Industrial Range Versions)	T_A	–40	25	85	°C	2

Notes:
1. Unless otherwise noted, all performance specifications quoted are evaluated for worst case at both 1.4 V ≤ V_{DDQ} ≤ 1.6 V (i.e., 1.5 V I/O) and 1.7 V ≤ V_{DDQ} ≤ 1.95 V (i.e., 1.8 V I/O) and quoted at whichever condition is worst case.
2. The power supplies need to be powered up simultaneously or in the following sequence: V_{DD}, V_{DDQ}, V_{REF}, followed by signal inputs. The power down sequence must be the reverse. V_{DDQ} must not exceed V_{DD}.
3. Most speed grades and configurations of this device are offered in both Commercial and Industrial Temperature ranges. The part number of Industrial Temperature Range versions end the character "I". Unless otherwise noted, all performance specifications quoted are evaluated for worst case in the temperature range marked on the device.

HSTL I/O DC Input Characteristics

Parameter	Symbol	Min	Max	Units	Notes
DC Input Logic High	V_{IH} (dc)	V_{REF} + 200		mV	1
DC Input Logic Low	V_{IL} (dc)		V_{REF} – 200	mV	1
V_{REF} DC Voltage	V_{REF} (dc)	V_{DDQ} (min)/2	V_{DDQ} (max)/2	V	1

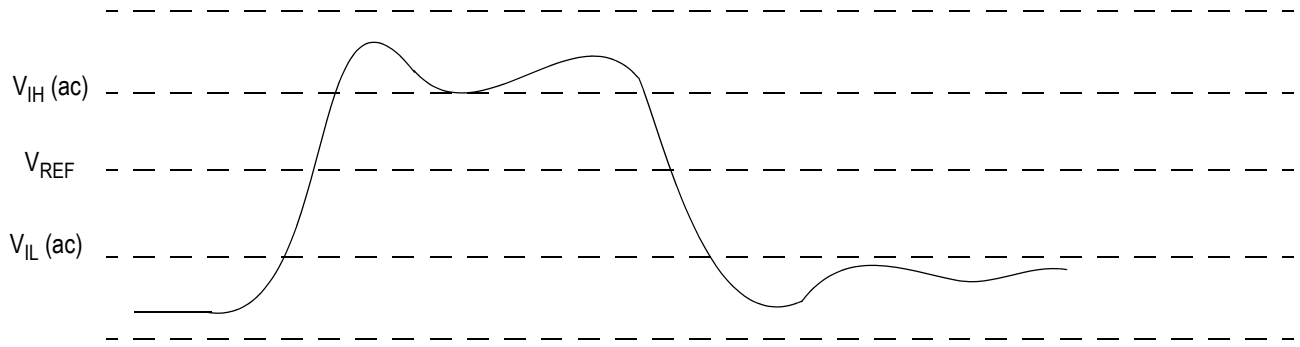
Note:
Compatible with both 1.8 V and 1.5 V I/O drivers

HSTL I/O AC Input Characteristics

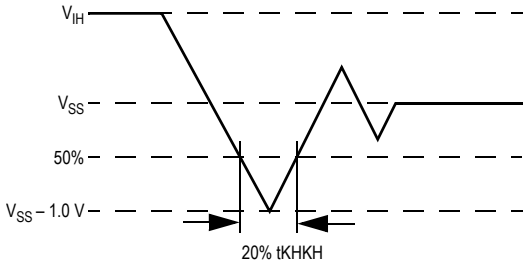
Parameter	Symbol	Min	Max	Units	Notes
AC Input Logic High	V_{IH} (ac)	V_{REF} + 400		mV	3,4
AC Input Logic Low	V_{IL} (ac)		V_{REF} – 400	mV	3,4
V_{REF} Peak to Peak AC Voltage	V_{REF} (ac)		5% V_{REF} (DC)	mV	1

Notes:
1. The peak to peak AC component superimposed on V_{REF} may not exceed 5% of the DC component of V_{REF}.
2. To guarantee AC characteristics, V_{IH},V_{IL}, Trise, and Tfall of inputs and clocks must be within 10% of each other.
3. For devices supplied with HSTL I/O input buffers. Compatible with both 1.8 V and 1.5 V I/O drivers.
4. See AC Input Definition drawing below.

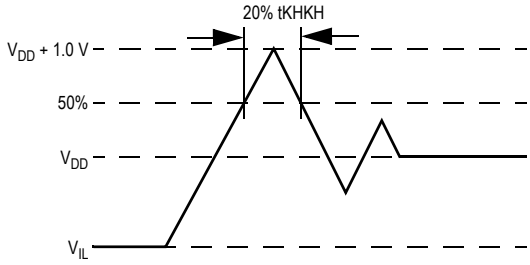
HSTL I/O AC Input Definitions



Undershoot Measurement and Timing



Overshoot Measurement and Timing



Capacitance

(T_A = 25°C, f = 1 MHz, V_{DD} = 3.3 V)

Parameter	Symbol	Test conditions	Typ.	Max.	Unit
Input Capacitance	C_{IN}	V_{IN} = 0 V	4	5	pF
Output Capacitance	C_{OUT}	V_{OUT} = 0 V	6	7	pF

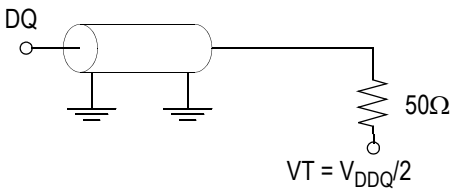
Note:
This parameter is sample tested.

AC Test Conditions

Parameter	Conditions
Input high level	V_{DDQ}
Input low level	0 V
Max. input slew rate	2 V/ns
Input reference level	$V_{DDQ}/2$
Output reference level	$V_{DDQ}/2$

Notes:
Test conditions as specified with output loading as shown unless otherwise noted.

AC Test Load Diagram



RQ = 250 Ω (HSTL I/O)
V_{REF} = 0.75 V

Input and Output Leakage Characteristics

Parameter	Symbol	Test Conditions	Min.	Max	Notes
Input Leakage Current (except mode pins)	I_{IL}	V_{IN} = 0 to V_{DD}	–2 uA	2 uA	
Output Leakage Current	I_{OL}	Output Disable, V_{OUT} = 0 to V_{DDQ}	–2 uA	2 uA	

Programmable Impedance HSTL Output Driver DC Electrical Characteristics

Parameter	Symbol	Min.	Max.	Units	Notes
Output High Voltage	V_{OH1}	$V_{DDQ}/2$	V_{DDQ}	V	1, 3
Output Low Voltage	V_{OL1}	Vss	$V_{DDQ}/2$	V	2, 3
Output High Voltage	V_{OH2}	V_{DDQ} – 0.2	V_{DDQ}	V	4, 5
Output Low Voltage	V_{OL2}	Vss	0.2	V	4, 6

Notes:

1. I_{OH} = (V_{DDQ}/2) / (RQ/5) +/– 15% @ V_{OH} = V_{DDQ}/2 (for: 175Ω ≤ RQ ≤ 350Ω).
2. I_{OL} = (V_{DDQ}/2) / (RQ/5) +/– 15% @ V_{OL} = V_{DDQ}/2 (for: 175Ω ≤ RQ ≤ 350Ω).
3. Parameter tested with RQ = 250Ω and V_{DDQ} = 1.5 V or 1.8 V
4. Minimum Impedance mode, ZQ = V_{SS}
5. I_{OH} = –1.0 mA
6. I_{OL} = 1.0 mA

Operating Currents

Parameter	Org	Symbol	-250		-200		-167		-133		-100		Test Conditions
			0°C to 70°C	–40°C to +85°C	0°C to 70°C	–40°C to +85°C	0°C to 70°C	–40°C to +85°C	0°C to 70°C	–40°C to +85°C	0°C to 70°C	–40°C to +85°C	
Operating Current	x18	IDD	TBD	TBD	460 mA	TBD	400 mA	TBD	340 mA	TBD	280 mA	TBD	$\overline{R}$ and $\overline{W}$ ≤ V_{IL} Max. tKHKH ≥ tKHKH Min. All other inputs V_{IN} ≤ V_{IL} Max. or V_{IN} ≥ V_{IH} Min.
		IDDQ	TBD	TBD	95 mA	TBD	85 mA	TBD	70 mA	TBD	65 mA	TBD	
Chip Disable Current	x18	ISB1	TBD	TBD	130 mA	TBD	120 mA	TBD	115 mA	TBD	110 mA	TBD	$\overline{R}$ and $\overline{W}$ ≥ V_{IH} Min. tKHKH ≥ tKHKH Min. All other inputs V_{IN} ≤ V_{IL} Max. or V_{IN} ≥ V_{IH} Min.
		ISBQ1	TBD	TBD	5 mA	TBD	5 mA	TBD	5 mA	TBD	5 mA	TBD	

Note:
Power measured with output pins floating.

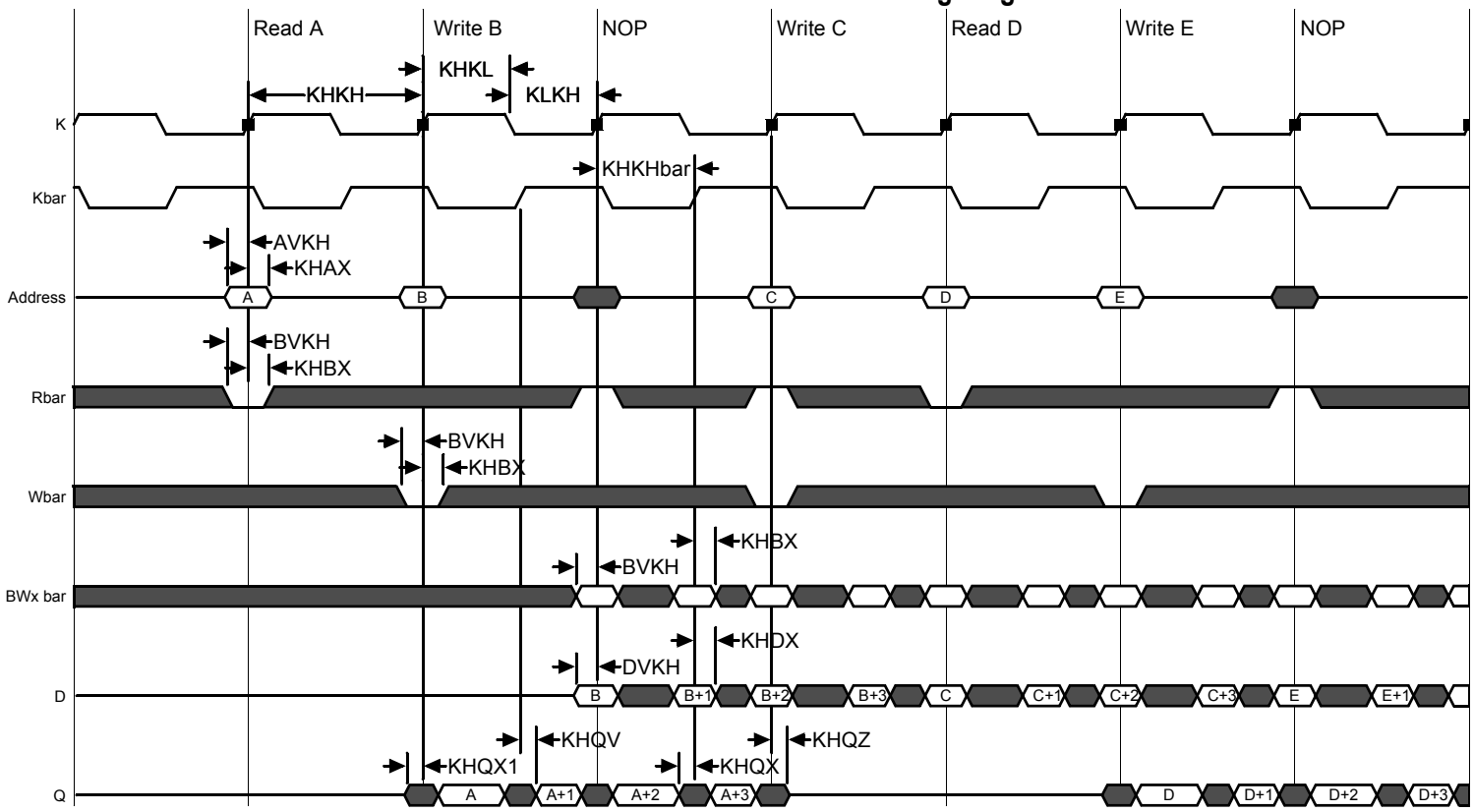
AC Electrical Characteristics

Parameter	Symbol	-250		-200		-167		-133		-100		Units	Notes
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
K, $\overline{K}$ Clock Cycle Time C, $\overline{C}$ Clock Cycle Time	t_{KHKH} t_{CHCH}	4.0	—	5.0	—	6.0	—	7.5	—	10	—	ns	
K, $\overline{K}$ Clock High Pulse Width C, $\overline{C}$ Clock High Pulse Width	t_{KHKL} t_{CHCL}	1.5	—	1.9	—	2.4	—	3.0	—	3.0	—	ns	
K, $\overline{K}$ Clock Low Pulse Width C, $\overline{C}$ Clock Low Pulse Width	t_{KLKH} t_{CLCH}	1.5	—	1.9	—	2.4	—	3.0	—	3.0	—	ns	
K Clock High to $\overline{K}$ Clock High C Clock High to $\overline{C}$ Clock High	$t_{KH\overline{K}H}$ $t_{CH\overline{C}H}$	1.8		2.2		2.7	—	3.4	—	4.6		ns	4
$\overline{K}$ Clock High to K Clock High $\overline{C}$ Clock High to C Clock High	$t_{\overline{K}HKH}$ $t_{\overline{C}HCH}$	1.8		2.2		2.7	—	3.4	—	4.6		ns	
K, $\overline{K}$ Clock High to C, $\overline{C}$ Clock High	t_{KHCH}	0	1.8	0	2.3	0	2.0	0	2.5	0	3.0	ns	
Address Input Setup Time	t_{AVKH}	0.5	—	0.6	—	0.7	—	0.8	—	1.0	—	ns	
Address Input Hold Time	t_{KHAX}	0.5	—	0.6	—	0.7	—	0.8	—	1.0	—	ns	
Control Input Setup Time	t_{BVKH}	0.5	—	0.6	—	0.7	—	0.8	—	1.0	—	ns	1
Control Input Hold Time	t_{KHBX}	0.5	—	0.6	—	0.7	—	0.8	—	1.0	—	ns	1
Data and Byte Write Input Setup Time	t_{DVKH}	0.5	—	0.6	—	0.7	—	0.8	—	1.0	—	ns	
Data and Byte Write Input Hold Time	t_{KHDX}	0.5	—	0.6	—	0.7	—	0.8	—	1.0	—	ns	
K, $\overline{K}$ Clock High to Data Output Valid C, $\overline{C}$ Clock High to Data Output Valid	t_{KHQV} t_{CHQV}	—	2.1	—	2.2	—	2.5	—	3.0	—	3.0	ns	
K, $\overline{K}$ Clock High to Data Output Hold C, $\overline{C}$ Clock High to Data Output Hold	t_{KHQX} t_{CHQX}	0.5	—	1.0	—	1.2	—	1.2	—	1.2	—	ns	2
K Clock High to Data Output Low-Z C Clock High to Data Output Low-Z	t_{KHQX1} t_{CHQX1}	0.5	—	1.0	—	1.2	—	1.2	—	1.2	—	ns	2,3
K Clock High to Data Output High-Z C Clock High to Data Output High-Z	t_{KHQZ} t_{CHQZ}	0.5	2.1	—	2.2	—	2.5	—	3.0	—	3.0	ns	2,3

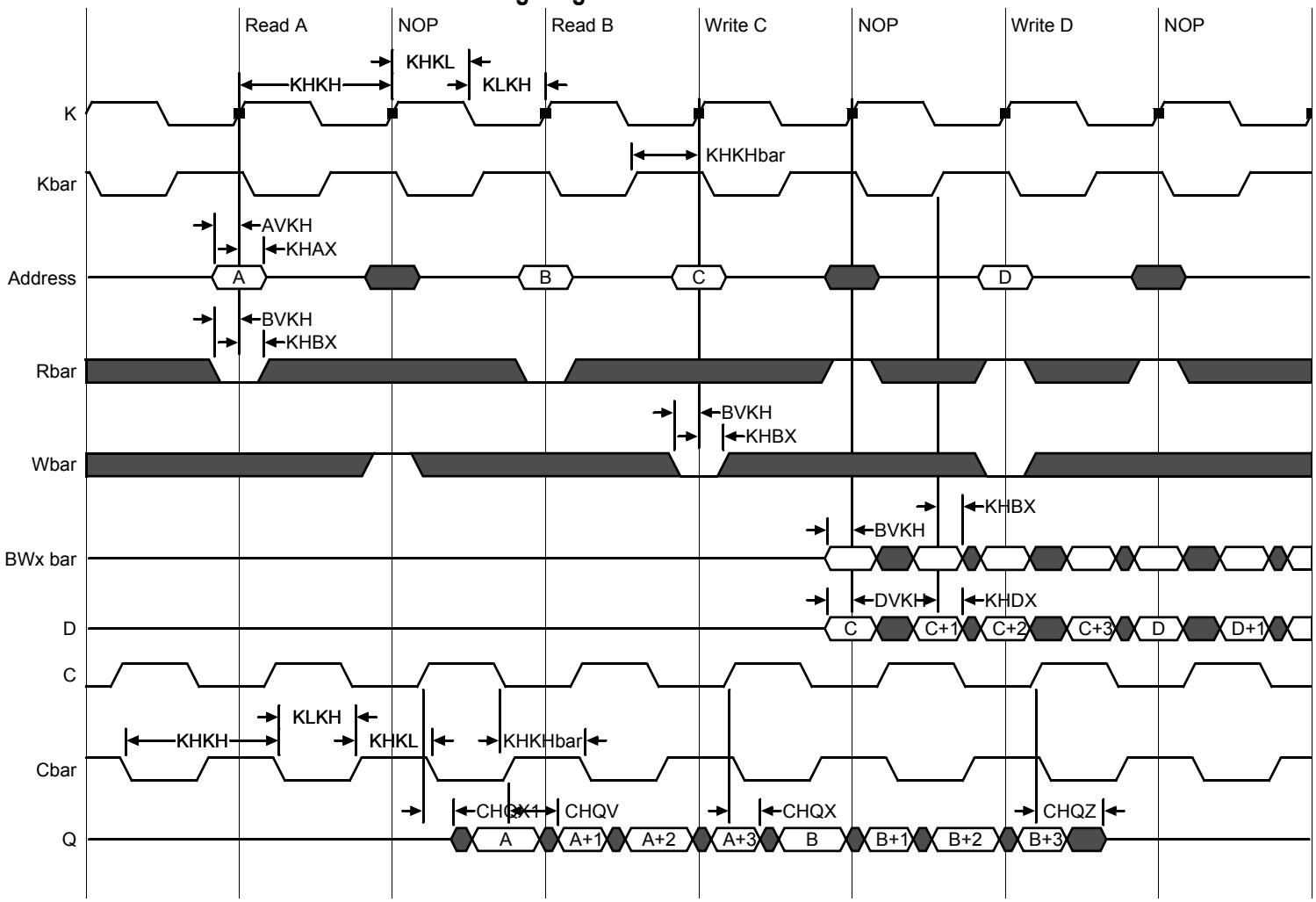
Notes:

1. These parameters apply to control inputs $\overline{R}$ and $\overline{W}$.
2. These parameters are guaranteed by design and characterization. Not 100% tested.
3. These parameters are measured at ±50mV from steady state voltage.
4. $t_{KH\overline{K}H}$ Max is specified by $t_{\overline{K}HKH}$ Min. $t_{CH\overline{C}H}$ Max is specified by $t_{\overline{C}HCH}$ Min.

K and $\overline{K}$ Controlled Read-Write-Read Timing Diagram



C and $\overline{C}$ Controlled Read-Write-Read Timing Diagram



JTAG Port Operation

Overview

The JTAG Port on this RAM operates in a manner that is compliant with IEEE Standard 1149.1-1990, a serial boundary scan interface standard (commonly referred to as JTAG). The JTAG Port input interface levels scale with V_{DD}. The JTAG output drivers are powered by V_{DDQ}.

Disabling the JTAG Port

It is possible to use this device without utilizing the JTAG port. The port is reset at power-up and will remain inactive unless clocked. TCK, TDI, and TMS are designed with internal pull-up circuits.To assure normal operation of the RAM with the JTAG Port unused, TCK, TDI, and TMS may be left floating or tied to either V_{DD} or V_{SS}. TDO should be left unconnected.

JTAG Port Registers

JTAG Pin Descriptions

Pin	Pin Name	I/O	Description
TCK	Test Clock	In	Clocks all TAP events. All inputs are captured on the rising edge of TCK and all outputs propagate from the falling edge of TCK.
TMS	Test Mode Select	In	The TMS input is sampled on the rising edge of TCK. This is the command input for the TAP controller state machine. An undriven TMS input will produce the same result as a logic one input level.
TDI	Test Data In	In	The TDI input is sampled on the rising edge of TCK. This is the input side of the serial registers placed between TDI and TDO. The register placed between TDI and TDO is determined by the state of the TAP Controller state machine and the instruction that is currently loaded in the TAP Instruction Register (refer to the TAP Controller State Diagram). An undriven TDI pin will produce the same result as a logic one input level.
TDO	Test Data Out	Out	Output that is active depending on the state of the TAP state machine. Output changes in response to the falling edge of TCK. This is the output side of the serial registers placed between TDI and TDO.

Note:
This device does not have a TRST (TAP Reset) pin. TRST is optional in IEEE 1149.1. The Test-Logic-Reset state is entered while TMS is held high for five rising edges of TCK. The TAP Controller is also reset automaticly at power-up.

Overview

The various JTAG registers, refered to as Test Access Port orTAP Registers, are selected (one at a time) via the sequences of 1s and 0s applied to TMS as TCK is strobed. Each of the TAP Registers is a serial shift register that captures serial input data on the rising edge of TCK and pushes serial data out on the next falling edge of TCK. When a register is selected, it is placed between the TDI and TDO pins.

Instruction Register

The Instruction Register holds the instructions that are executed by the TAP controller when it is moved into the Run, Test/Idle, or the various data register states. Instructions are 3 bits long. The Instruction Register can be loaded when it is placed between the TDI and TDO pins. The Instruction Register is automatically preloaded with the IDCODE instruction at power-up or whenever the controller is placed in Test-Logic-Reset state.

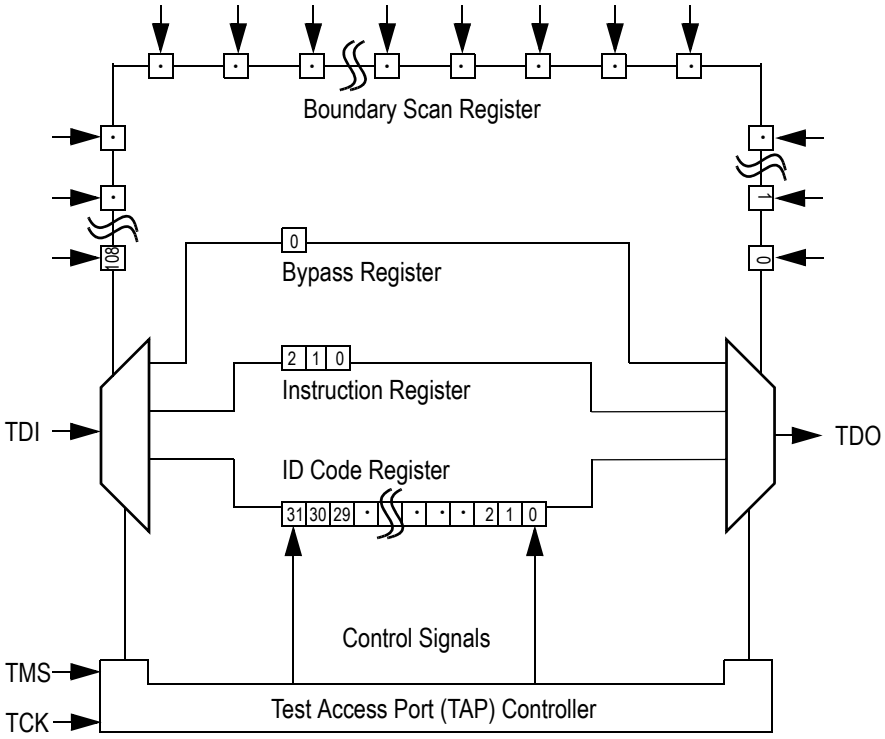
Bypass Register

The Bypass Register is a single bit register that can be placed between TDI and TDO. It allows serial test data to be passed through the RAM's JTAG Port to another device in the scan chain with as little delay as possible.

Boundary Scan Register

The Boundary Scan Register is a collection of flip flops that can be preset by the logic level found on the RAM's input or I/O pins. The flip flops are then daisy chained together so the levels found can be shifted serially out of the JTAG Port's TDO pin. The Boundary Scan Register also includes a number of place holder flip flops (always set to a logic 1). The relationship between the device pins and the bits in the Boundary Scan Register is described in the Scan Order Table following. The Boundary Scan Register, under the control of the TAP Controller, is loaded with the contents of the RAMs I/O ring when the controller is in Capture-DR state and then is placed between the TDI and TDO pins when the controller is moved to Shift-DR state. SAMPLE-Z, SAMPLE/PRELOAD and EXTEST instructions can be used to activate the Boundary Scan Register.

JTAG TAP Block Diagram



Identification (ID) Register

The ID Register is a 32-bit register that is loaded with a device and vendor specific 32-bit code when the controller is put in Capture-DR state with the IDCODE command loaded in the Instruction Register. The code is loaded from a 32-bit on-chip ROM. It describes various attributes of the RAM as indicated below. The register is then placed between the TDI and TDO pins when the controller is moved into Shift-DR state. Bit 0 in the register is the LSB and the first to reach TDO when shifting begins.

Tap Controller Instruction Set

ID Register Contents

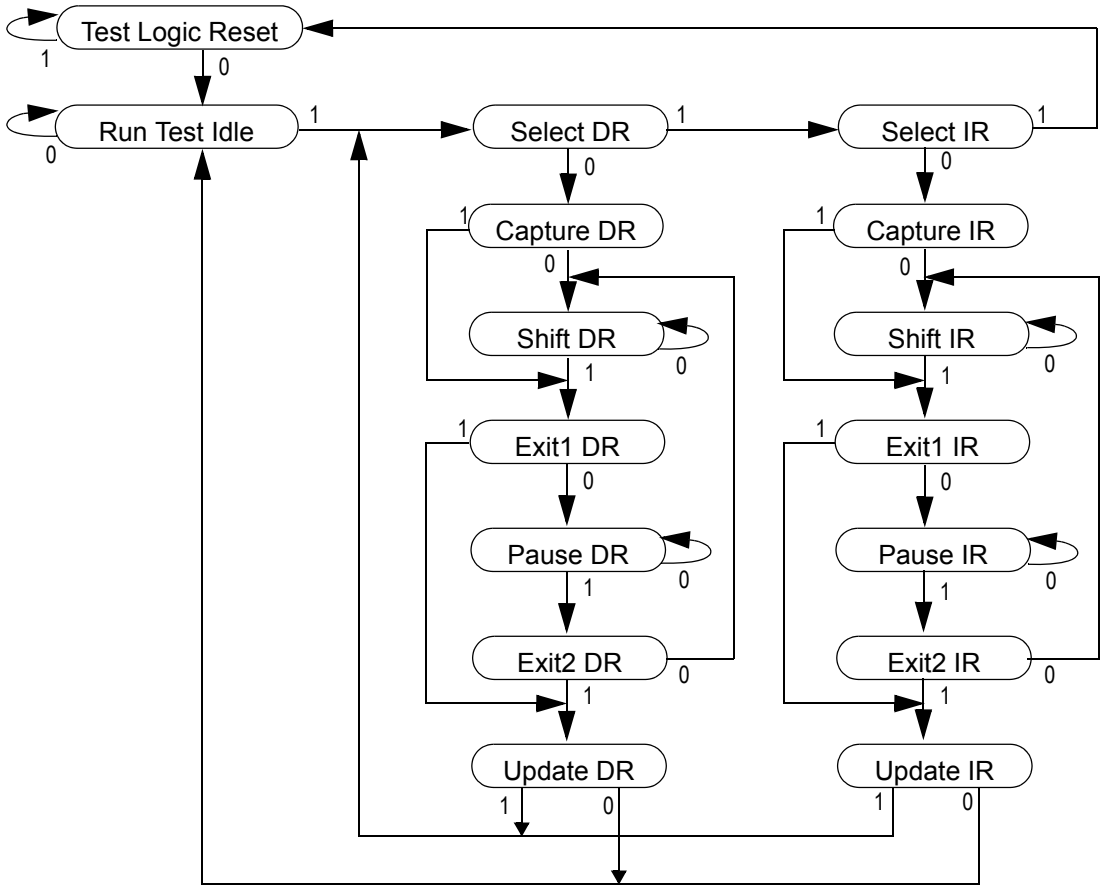
	Die Revision Code				Not Used												I/O Configuration				GSI Technology JEDEC Vendor ID Code											Presence Register
Bit #	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
x18	X	X	X	X	0	0	0	X	1	0	0	1	0	0	0	0	1	0	1	0	0	0	0	1	1	0	1	1	0	0	1	1

Overview

There are two classes of instructions defined in the Standard 1149.1-1990; the standard (Public) instructions, and device specific (Private) instructions. Some Public instructions are mandatory for 1149.1 compliance. Optional Public instructions must be implemented in prescribed ways. The TAP on this device may be used to monitor all input and I/O pads, and can be used to load address, data or control signals into the RAM or to preload the I/O buffers.

When the TAP controller is placed in Capture-IR state the two least significant bits of the instruction register are loaded with 01. When the controller is moved to the Shift-IR state the Instruction Register is placed between TDI and TDO. In this state the desired instruction is serially loaded through the TDI input (while the previous contents are shifted out at TDO). For all instructions, the TAP executes newly loaded instructions only when the controller is moved to Update-IR state. The TAP instruction set for this device is listed in the following table.

JTAG Tap Controller State Diagram



Instruction Descriptions

BYPASS

When the BYPASS instruction is loaded in the Instruction Register the Bypass Register is placed between TDI and TDO. This occurs when the TAP controller is moved to the Shift-DR state. This allows the board level scan path to be shortened to facilitate testing of other devices in the scan path.

SAMPLE/PRELOAD

SAMPLE/PRELOAD is a Standard 1149.1 mandatory public instruction. When the SAMPLE / PRELOAD instruction is loaded in the Instruction Register, moving the TAP controller into the Capture-DR state loads the data in the RAMs input and I/O buffers into the Boundary Scan Register. Boundary Scan Register locations are not associated with an input or I/O pin, and are loaded with the default state identified in the Boundary Scan Chain table at the end of this section of the datasheet. Because the RAM clock is independent from the TAP Clock (TCK) it is possible for the TAP to attempt to capture the I/O ring contents while the input buffers are in transition (i.e. in a metastable state). Although allowing the TAP to sample metastable inputs will not harm the device, repeatable results cannot be expected. RAM input signals must be stabilized for long enough to meet the TAPs input data capture set-up plus hold time (tTS plus tTH). The RAMs clock inputs need not be paused for any other TAP operation except capturing the I/O ring contents into the Boundary Scan Register. Moving the controller to Shift-DR state then places the boundary scan register between the TDI and TDO pins.

EXTEST

EXTEST is an IEEE 1149.1 mandatory public instruction. It is to be executed whenever the instruction register is loaded with all logic 0s. The EXTEST command does not block or override the RAM's input pins; therefore, the RAM's internal state is

still determined by its input pins.

Typically, the Boundary Scan Register is loaded with the desired pattern of data with the SAMPLE/PRELOAD command. Then the EXTEST command is used to output the Boundary Scan Register's contents, in parallel, on the RAM's data output drivers on the falling edge of TCK when the controller is in the Update-IR state.

Alternately, the Boundary Scan Register may be loaded in parallel using the EXTEST command. When the EXTEST instruction is selected, the sate of all the RAM's input and I/O pins, as well as the default values at Scan Register locations not associated with a pin, are transferred in parallel into the Boundary Scan Register on the rising edge of TCK in the Capture-DR state, the RAM's output pins drive out the value of the Boundary Scan Register location with which each output pin is associated.

IDCODE

The IDCODE instruction causes the ID ROM to be loaded into the ID register when the controller is in Capture-DR mode and places the ID register between the TDI and TDO pins in Shift-DR mode. The IDCODE instruction is the default instruction loaded in at power up and any time the controller is placed in the Test-Logic-Reset state.

SAMPLE-Z

If the SAMPLE-Z instruction is loaded in the instruction register, all RAM outputs are forced to an inactive drive state (high-Z) and the Boundary Scan Register is connected between TDI and TDO when the TAP controller is moved to the Shift-DR state.

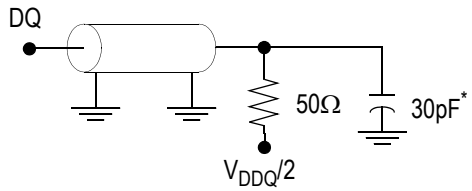
RFU

These instructions are Reserved for Future Use. In this device they replicate the BYPASS instruction.

JTAG Port AC Test Conditions

Parameter	Conditions
Input high level	V_{DD} – 0.2 V
Input low level	0.2 V
Input slew rate	1 V/ns
Input reference level	$V_{DDQ}/2$
Output reference level	$V_{DDQ}/2$

JTAG Port AC Test Load



* Distributed Test Jig Capacitance

Notes:
1. Include scope and jig capacitance.
2. Test conditions as shown unless otherwise noted.

JTAG TAP Instruction Set Summary

Instruction	Code	Description	Notes
EXTEST	000	Places the Boundary Scan Register between TDI and TDO.	1
IDCODE	001	Preloads ID Register and places it between TDI and TDO.	1, 2
SAMPLE-Z	010	Captures I/O ring contents. Places the Boundary Scan Register between TDI and TDO. Forces all RAM output drivers to High-Z.	1
RFU	011	Do not use this instruction; Reserved for Future Use. Replicates BYPASS instruction. Places Bypass Register between TDI and TDO.	1
SAMPLE/ PRELOAD	100	Captures I/O ring contents. Places the Boundary Scan Register between TDI and TDO.	1
GSI	101	GSI private instruction.	1
RFU	110	Do not use this instruction; Reserved for Future Use. Replicates BYPASS instruction. Places Bypass Register between TDI and TDO.	1
BYPASS	111	Places Bypass Register between TDI and TDO.	1

Notes:
1. Instruction codes expressed in binary, MSB on left, LSB on right.
2. Default instruction automatically loaded at power-up and in test-logic-reset state.

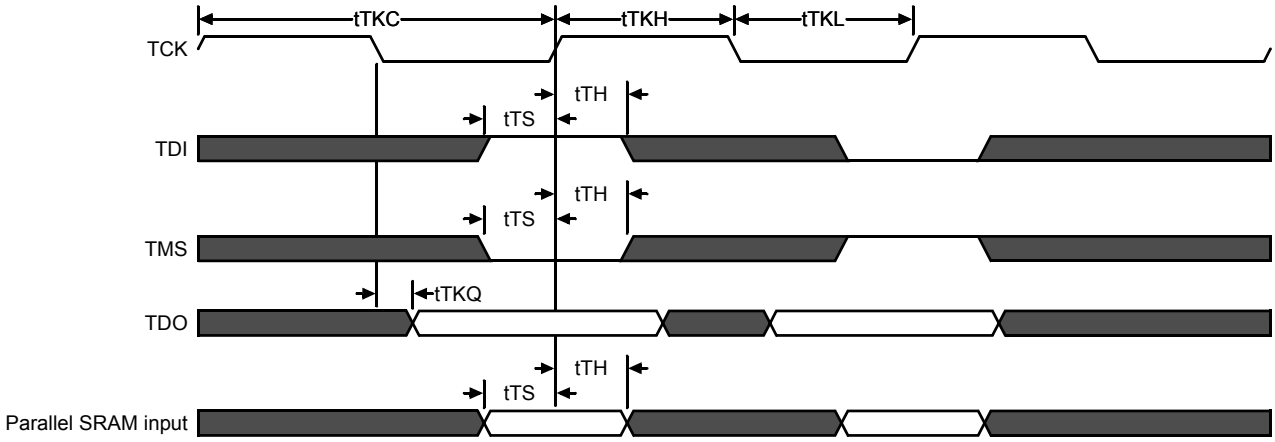
JTAG Port Recommended Operating Conditions and DC Characteristics

Parameter	Symbol	Min.	Max.	Unit	Notes
Test Port Input High Voltage	V_{IHJ}	0.6 * V_{DD}	V_{DD2} +0.3	V	1
Test Port Input Low Voltage	V_{ILJ}	–0.3	0.3 * V_{DD}	V	1
TMS, TCK and TDI Input Leakage Current	I_{INHJ}	–300	1	uA	2
TMS, TCK and TDI Input Leakage Current	I_{INLJ}	–1	100	uA	3
TDO Output Leakage Current	I_{OLJ}	–1	1	uA	4
Test Port Output High Voltage	V_{OHJ}	1.7	—	V	5, 6
Test Port Output Low Voltage	V_{OLJ}	—	0.4	V	5, 7
Test Port Output CMOS High	V_{OHJC}	V_{DDQ} – 100 mV	—	V	5, 8
Test Port Output CMOS Low	V_{OLJC}	—	100 mV	V	5, 9

Notes:

1. Input Under/overshoot voltage must be – V > Vi < V_{DDn} + V not to exceed .6 V maximum, with a pulse width not to exceed 20% tTKC.
2. $V_{ILJ} \leq V_{IN} \leq V_{DDn}$
3. $0\ V \leq V_{IN} \leq V_{ILJn}$
4. Output Disable, V_{OUT} = 0 to V_{DDn}
5. The TDO output driver is served by the V_{DDQ} supply.
6. I_{OHJ} = –4 mA
7. I_{OLJ} = + 4 mA
8. I_{OHJC} = –100 uA
9. I_{OHJC} = +100 uA

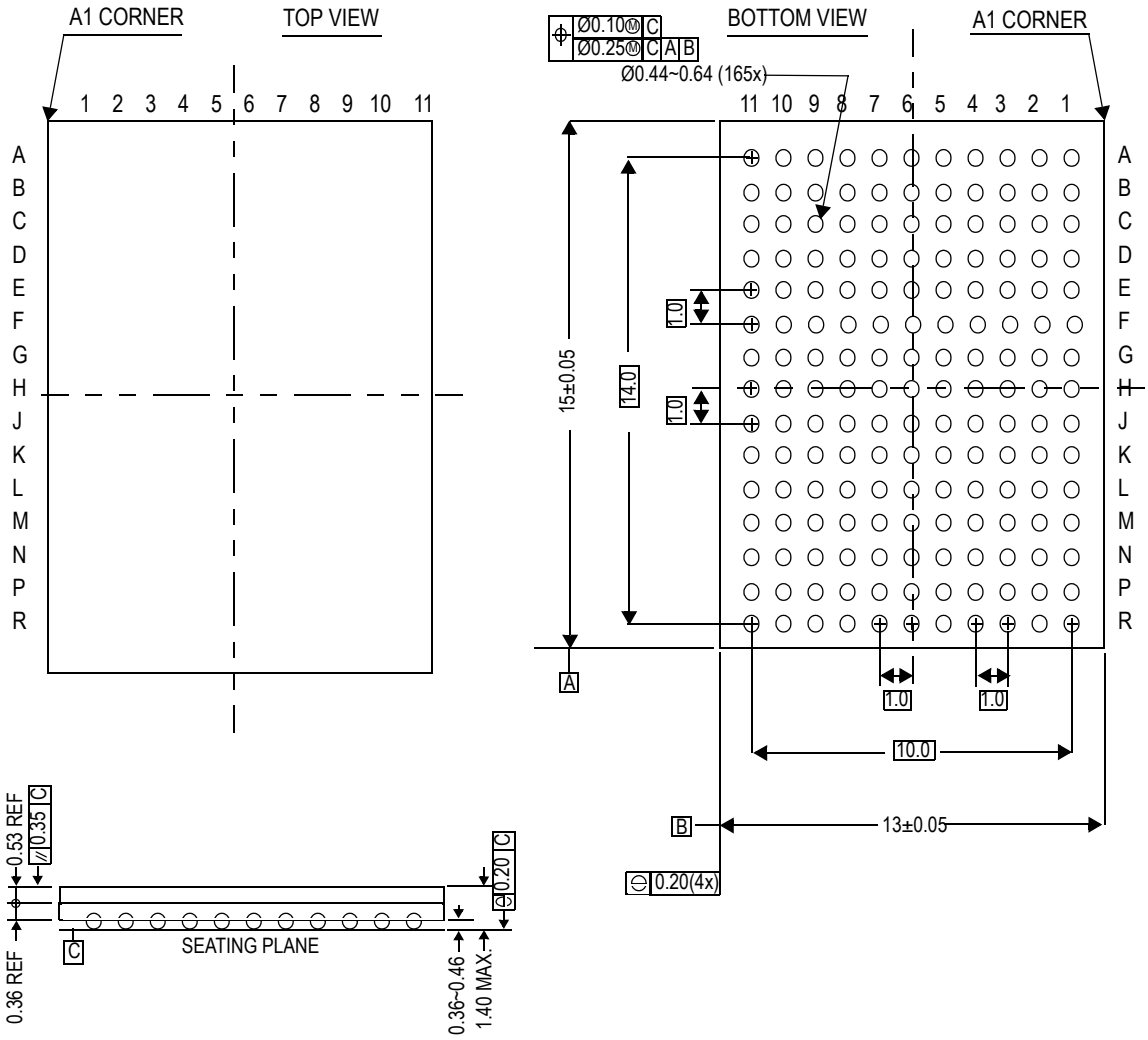
JTAG Port Timing Diagram



JTAG Port AC Electrical Characteristics

Parameter	Symbol	Min	Max	Unit
TCK Cycle Time	tTKC	50	—	ns
TCK Low to TDO Valid	tTKQ	—	20	ns
TCK High Pulse Width	tTKH	20	—	ns
TCK Low Pulse Width	tTKL	20	—	ns
TDI & TMS Set Up Time	tTS	10	—	ns
TDI & TMS Hold Time	tTH	10	—	ns

Package Dimensions—165-Bump FPBGA (Package D; Variation 3)



Ordering Information—GSI SigmaQuad SRAM

Org	Part Number[1]	Type	Package	Speed (MHz)	T_A[3]
1M x 18	GS8180DV18D-250	SigmaQuad SRAM	1 mm Pitch, 165-Pin BGA (var. 3)	250	C
1M x 18	GS8180DV18D-200	SigmaQuad SRAM	1 mm Pitch, 165-Pin BGA (var. 3)	200	C
1M x 18	GS8180DV18D-167	SigmaQuad SRAM	1 mm Pitch, 165-Pin BGA (var. 3)	167	C
1M x 18	GS8180DV18D-133	SigmaQuad SRAM	1 mm Pitch, 165-Pin BGA (var. 3)	133	C
1M x 18	GS8180DV18D-100	SigmaQuad SRAM	1 mm Pitch, 165-Pin BGA (var. 3)	100	C
1M x 18	GS8180DV18D-250I	SigmaQuad SRAM	1 mm Pitch, 165-Pin BGA (var. 3)	250	I
1M x 18	GS8180DV18D-200I	SigmaQuad SRAM	1 mm Pitch, 165-Pin BGA (var. 3)	200	I
1M x 18	GS8180DV18D-167I	SigmaQuad SRAM	1 mm Pitch, 165-Pin BGA (var. 3)	167	I
1M x 18	GS8180DV18D-133I	SigmaQuad SRAM	1 mm Pitch, 165-Pin BGA (var. 3)	133	I
1M x 18	GS8180DV18D-100I	SigmaQuad SRAM	1 mm Pitch, 165-Pin BGA (var. 3)	100	I

Notes:

1. Customers requiring delivery in Tape and Reel should add the character “T” to the end of the part number. Example: GS818x18D-200T.
2. T_A = C = Commercial Temperature Range. T_A = I = Industrial Temperature Range.

