AN1578
Application Note

MECL 10H™ SPICE Kit
for Berkeley SPICE (PSPICE)

Prepared by
Andrea Diermeier
Cleon Petty
Motorola Logic Applications Engineering

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MECL 10H SPICE Kit for Berkeley SPICE (PSPICE)

The purpose of this application note is to present spice parameters and schematics for a particular set of MC10H MECL logic devices. The devices to be presented are the:

MC10H101, H102, H103, H104, H105,H116,
H131, H188, H189, H210, and H211.

This file is intended for Berkeley SPICE Type simulators (e.g. PSPICE). A similar file is available for H–SPICE. Those are the most used simulators.

MC10H is a Motorola ECL family that features a 100% speed improvement over the standard 10K family, and still maintains the same gate power. The family has been designed with voltage compensation to keep both DC and AC parameters constant over a ±5% power supply variation, with a 75% improvement in noise margin as a result. The 10H family is a pin for pin duplicate of many of the MECL 10K devices, is compatible with 10K, MECL lll,and Motorola's new MC10E and MC10EL ECLinPS and E–Lite families.The devices, like all single supply ECL devices, are usable in a PECL (Positive Emitter Coupled Logic) mode and will suffer no AC or DC performance degradation if treated as prescribed in a Motorola Application Note "*Designing with PECL (ECL at +5.0V)*" (AN1406/D). AN1406 can be found in the new "*High Performance ECL Data Book*" (DL140/D) or it can be obtained through the Motorola Literature Distribution Center.

Family Specifications are located in the MECL DATA book DL122/D. Section 2 presents the temperature and power supply variations that can be expected from the family. The typical delay is 1.0ns, Tr/Tf is 1Ns, measured at the 20–80% points of the edges, Typical VOH is VCC–890MV, Typical VOL is VCC–1750MV, Typical VBB is VCC–1295MV, and 50 ohms to VTT (VCC–2.0v) is the max load recommended.

The following are netlists of the MC10H devices and will include the necessary typical resistor parasitics. The schematics of the netlist are included in the paper to allow the user the ease of seeing the function and follow the netlist more easily. There are no ESD models for the devices since the MC10H family has none.

The Global nodes will be:

(VCC)	Top rail power supply
(VCCO)	Top Rail Power supply for Emitter Follower Output Transistors
(VEE)	Bottom Rail Power Supply
(VBB)	Switching Bias Voltage (VCC–1295MV)
(VBBP)	Reference–Voltage (VCC–2095MV)
(VBBPP)	Reference–Voltage (VCC–2895MV)
(VCS)	Current Source Base Voltage (VEE + 1.3V)
(VTT)	Termination sink supply (VCC – 2.0V)
(IN)	Input
(INB)	Inverted input
(OR)	Or Output
(NOR)	Nor output
(CLK)	Clock Input
(CLKB)	Clock Bar Input

```
*********************************************************************
*                  THE FOLLOWING IS A PIN MODEL FOR THE              *
**********                  Package Models ( )               **********
*********************************************************************
*  Package Models: (8-lead SOIC)                                    *
*                  (16-lead DIP) CENTER PIN                         *
*                  (16-lead DIP) END PIN                            *
*                  (20-Lead PLCC)                                   *
*                  (20-Lead SOIC Center Pin)                        *
*                  (20-Lead SOIC End Pin)                           *
*                  (28-lead PLCC)                                   *
*  EXT = THE END CONNECTED TO EXTERNAL NODE                         *
*  INT = THE END CONNECTED TO THE CIRCUIT INSIDE PACKAGE            *
*********************************************************************
***** (8-LEAD SOIC PACKAGE)
.SUBCKT PKG8  EXT INT
    X   EXT INT  PKG params: C=0.8P R1=750 R2=0.1 L=1.5N
.ENDS   PKG8
***** (16-LEAD DIP PACKAGE CENTER PIN)
.SUBCKT PKG16CP  EXT INT
    X   EXT INT  PKG params: C=0.7P R1=750 R2=0.1 L=2.5N
.ENDS   PKG16CP
***** (16-LEAD DIP PACKAGE END PIN)
.SUBCKT DIP16EP  EXT INT
    X   EXT INT  PKG params: C=1.3P R1=750 R2=0.1 L=5.5N
.ENDS   DIP16EP
***** (20-LEAD PLCC PACKAGE)
.SUBCKT PKG20  EXT INT
    X   EXT INT  PKG params: C=0.65P R1=750 R2=0.2 L=0.9N
.ENDS   PKG20
***** (20-LEAD SOIC PACKAGE CENTER PIN)
.SUBCKT SC20CP  EXT INT
    X   EXT INT  PKG params: C=0.6P R1=750 R2=0.2 L=1.9N
.ENDS   SC20CP
***** (20-LEAD SOIC PACKAGE END PIN)
.SUBCKT SC20EP  EXT INT
    X   EXT INT  PKG params: C=0.8P R1=750 R2=0.2 L=3.0N
.ENDS   SC20EP
***** (28-LEAD PLCC PACKAGE)
.SUBCKT PKG28  EXT INT
    X   EXT INT  PKG params: C=0.8P R1=750 R2=0.2 L=1.1N
.ENDS   PKG28
*********************************************************************
*NOTE NODES SIN=STROBE IN. SOUT=STROBE PIN TO OTHER UNITS IN PACKAGE*
*********************************************************************
.SUBCKT H101  VCC VCCO VBB VCS VEE IN SIN OR NOR
    Q1    3 1 5 VEE       T08I3
    Q2    3 2 5 VEE       T08I3
    Q3    4 VBB 5 VEE     T08I3
    Q4    5 VCS 6 VEE     T12B1
    Q5    VCCO 4 OR VEE   T5406
    Q6    VCCO 3 NOR VEE  T5406
    XR1   VCC 3 VCC       RES params: R=276
    XR2   VCC 4 VCC       RES params: R=276
    XR3   6 VEE VCC       RES params: R=127
    XRB1  IN 1 VCC        RES params: R=50
    XRB2  SIN 2 VCC       RES params: R=50
    XRP1  IN VEE VCC      RPD params: R=50K
    XRP2  SIN VEE VCC     RPD params: R=50K
.ENDS H101
```

```
*********************************************************************
* THERE ARE TWO SUBCIRCUITS IN THE MC10H102 ONE FOR THE THREE NOR   *
* ONLY GATES (H102N) AND ONE FOR THE OR/NOR GATE (H102NO).          *
*********************************************************************
.SUBCKT H102N  VCC VCCO VBB VCS VEE IN1 IN2 NOR1
    Q1    3 1 4 VEE       T08I3
    Q2    3 2 4 VEE       T08I3
    Q3    VCC VBB 4 VEE   T08I3
    Q4    4 VCS 5 VEE     T12B1
    Q5    VCCO 3 NOR1 VEE T5406
    XR1   VCC 3 VCC       RES params: R=276
    XR2   5 VEE VCC       RES params: R=127
    XRB1  IN1 1 VCC       RES params: R=50
    XRB2  IN2 2 VCC       RES params: R=50
    XRP1  IN1 VEE VCC     RPD params: R=50K
    XRP2  IN2 VEE VCC     RPD params: R=50K
.ENDS H102N
*********************************************************************
.SUBCKT H102NO  VCC VCCO VBB VCS VEE IN3 IN4 OR NOR2
    Q6    8 6 10 VEE      T08I3
    Q7    8 7 10 VEE      T08I3
    Q8    9 VBB 10 VEE    T08I3
    Q9    10 VCS 11 VEE   T12B1
    Q10   VCCO 9 OR VEE   T5406
    Q11   VCCO 8 NOR2 VEE T5406
    XR4   VCC 8 VCC       RES params: R=276
    XR5   VCC 9 VCC       RES params: R=276
    XR6   11 VEE VCC      RES params: R=127
    XRB3  IN3 6 VCC       RES params: R=50
    XRB4  IN4 7 VCC       RES params: R=50
    XRP3  IN3 VEE VCC     RPD params: R=50K
    XRP4  IN4 VEE VCC     RPD params: R=50K
.ENDS H102NO
*********************************************************************
* THERE ARE TWO SUBCIRCUITS IN THE MC10H103 ONE FOR THE THREE OR    *
* ONLY GATES (H103O) AND ONE FOR THE OR/NOR GATE (H103NO)           *
*********************************************************************
.SUBCKT H103O  VCC VCCO VBB VCS VEE IN1 IN2 NOR1
    Q1    VCC 1 4 VEE     T08I3
    Q2    VCC 2 4 VEE     T08I3
    Q3    3 VBB 4 VEE     T08I3
    Q4    4 VCS 5 VEE     T12B1
    Q5    VCCO 3 NOR1 VEE T5406
    XR1   VCC 3 VCC       RES params: R=276
    XR2   5 VEE VCC       RES params: R=127
    XRB1  IN1 1 VCC       RES params: R=50
    XRB2  IN2 2 VCC       RES params: R=50
    XRP1  IN1 VEE VCC     RPD params: R=50K
    XRP2  IN2 VEE VCC     RPD params: R=50K
.ENDS H103O
*********************************************************************
.SUBCKT H103NO  VCC VCCO VBB VCS VEE IN3 IN4 OR NOR2
    Q6    8 6 10 VEE      T08I3
    Q7    8 7 10 VEE      T08I3
    Q8    9 VBB 10 VEE    T08I3
    Q9    10 VCS 11 VEE   T12B1
    Q10   VCCO 9 OR VEE  T5406
    Q11   VCCO 8 NOR2 VEE  T5406
    XR4   VCC 8 VCC       RES params: R=276
    XR5   VCC 9 VCC       RES params: R=276
    XR6   11 VEE VCC      RES params: R=127
```

```
    XRB3  IN3 6 VCC       RES params: R=50
    XRB4  IN4 7 VCC       RES params: R=50
    XRP3  IN3 VEE VCC     RPD params: R=50K
    XRP4  IN4 VEE VCC     RPD params: R=50K
.ENDS H103NO
*************************************************************************
* The MC10H104 is a Quad 2-Input AND/NAND gate.                         *
*                                                                       *
*************************************************************************
.SUBCKT H104  VCC VCCO VBB VBBPP VCS VEE IN1 IN2 OUT OUTB
    Q1     VCC 1 2 VEE     T08I3
    Q2     2 2 3 VEE       T08I3
    Q3     VCC VBBPP 3 VEE T08I3
    Q4     3 VCS 4 VEE     T12B1
    Q5     6 5 7 VEE       T08I3
    Q6     8 VBB 7 VEE     T08I3
    Q7     8 VBB 9 VEE     T08I3
    Q8     7 3 10 VEE      T08I3
    Q9     9 VBBPP 10 VEE   T08I3
    Q10    10 VCS 11 VEE   T12B1
    Q11    VCCO 6 OUTB VEE T5406
    Q12    VCCO 8 OUT VEE  T5406
    XR1    VCC 6 VCC       RES params: R=281
    XR2    VCC 8 VCC       RES params: R=281
    XR3    4 VEE VCC       RES params: R=377
    XR4    11 VEE VCC      RES params: R=128
    XRb1   IN2 1 VCC       RES params: R=50
    XRb2   IN1 5 VCC       RES params: R=50
    XRP1   IN1 VEE VCC     RPD params: R=50K
    XRP2   IN2 VEE VCC     RPD params: R=50K
    XRXCX1 VCC 1 VEE       RXCX1
.ENDS H104
*************************************************************************
* THERE ARE TWO SUBCIRCUITS IN THE MC10H105 ONE FOR THE TWO TWO         *
* INPUT OR/NOR GATES (H1052) AND ONE FOR THE THREE INPUT OR/NOR         *
* GATE (H1053)                                                          *
*************************************************************************
.SUBCKT H1052  VCC VCCO VBB VCS VEE IN1 IN2 OR1 NOR1
    Q1    3 1 5 VEE       T08I3
    Q2    3 2 5 VEE       T08I3
    Q3    4 VBB 5 VEE     T08I3
    Q4    5 VCS 6 VEE     T12B1
    Q5    VCCO 4 OR1 VEE  T5406
    Q6    VCCO 3 NOR1 VEE T5406
    XR1   VCC 3 VCC       RES params: R=276
    XR2   VCC 4 VCC       RES params: R=276
    XR3   6 VEE VCC       RES params: R=127
    XRB1  IN1 1 VCC       RES params: R=50
    XRB2  IN2 2 VCC       RES params: R=50
    XRP1  IN1 VEE VCC     RPD params: R=50K
    XRP2  IN2 VEE VCC     RPD params: R=50K
.ENDS H1052
*************************************************************************
.SUBCKT H1053  VCC VCCO VBB VCS VEE IN3 IN4 IN5 OR2 NOR2
     Q7    10 7 12 VEE      T08I3
     Q8    10 8 12 VEE      T08I3
     Q9    10 9 12 VEE      T08I3
     Q10   11 VBB 12 VEE    T08I3
     Q11   12 VCS 13 VEE    T12B1
     Q12   VCCO 11 OR2 VEE  T5406
     Q13   VCCO 10 NOR2 VEE T5406
```

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     XR4   VCC 10 VCC       RES params: R=276
     XR5   VCC 11 VCC       RES params: R=276
     XR6   13 VEE VCC       RES params: R=127
     XRB3  IN3 7 VCC        RES params: R=50
     XRB4  IN4 8 VCC        RES params: R=50
     XRB5  IN5 9 VCC        RES params: R=50
     XRP3  IN3 VEE VCC      RPD params: R=50K
     XRP4  IN4 VEE VCC      RPD params: R=50K
     XRP5  IN5 VEE VCC      RPD params: R=50K
.ENDS H1053
*********************************************************************
* THE MC10H116 LINE RECEIVER (H116) HAS THREE GATES IN A PACKAGE    *
* AND NO PULLDOWNS TO VEE                                           *
*********************************************************************
.SUBCKT H116  VCC VCCO VCS VEE IN INB OUT OUTB
    Q1    2 1 4 VEE       T08I3
    Q2    3 6 4 VEE       T08I3
    Q3    4 VCS 5 VEE     T12B1
    Q4    VCCO 2 OUTB VEE T5406
    Q5    VCCO 3 OUT VEE  T5406
    XR1   VCC 2 VCC       RES params: R=289
    XR2   VCC 3 VCC       RES params: R=289
    XR3   5 VEE VCC       RES params: R=127
    XRB1  IN 1 VCC        RES params: R=50
    XRB2  INB 6 VCC       RES params: R=50
.ENDS H116
*********************************************************************
* THE MC10H131 IS A DUAL D FLIP FLOP WITH SET AND RESET.            *
* CC=COMMON CLOCK, CE=INDIV CLOCK IN, DIN=DATA IN, SE=SET IN,       *
* RES=RESET, Q=TRUE OUT, QB=INV OUT,VBBP=VBB -.82V                  *
*********************************************************************
.SUBCKT H131  VCC VCCO VBB VBBP VCS VEE DIN CC CE SE RE Q QB
    Q1     VCC 29 33 VEE  T08I2
    Q2     VCC 30 33 VEE  T08I2
    Q3     VCC 31 33 VEE  T08I2
    Q4     VCC 32 33 VEE  T08I2
    Q5     34 VCS 35 VEE  T12B4
    Q6     2 1 5 VEE      T05I3
    Q7     4 VBB 5 VEE    T05I3
    Q8     5 VBBP 6 VEE   T05I3
    Q9     6 VCS 7 VEE    T12B4
    Q10    8 VCS 9 VEE    T06B1
    Q11    11 33 6 VEE    T05I3
    Q12    2 10 11 VEE    T05I3
    Q13    2 8 11 VEE     T05I3
    Q14    VCC 4 8 VEE    T05I2
    Q15    VCC 2 13 VEE   T05I2
    Q16    4 13 11 VEE    T05I3
    Q17    4 12 11 VEE    T05I3
    Q18    13 VCS 14 VEE  T06B1
    Q19    16 13 19 VEE   T08I3
    Q20    16 15 19 VEE   T08I3
    Q21    19 33 20 VEE   T08I3
    Q22    20 VCS 21 VEE  T12B4
    Q23    23 VCS 22 VEE  T12B1
    Q24    17 18 19 VEE   T08I3
    Q25    17 8 19 VEE    T08I3
    Q26    VCC 17 24 VEE  T08I2
    Q27    16 23 25 VEE   T08I3
    Q28    25 VBBP 20 VEE T08I3
    Q29    27 VCS 28 VEE  T12B1
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    Q30    17 27 25 VEE   T08I3
    Q31    VCC 16 26 VEE  T08I2
    Q32    VCCO 17 QB VEE T5406
    Q33    VCCO 16 Q VEE  T5406
    QD1    33 33 34 VEE   T08I3
    QD2    24 24 23 VEE   T08I3
    QD3    26 26 27 VEE   T08I3
    XRXCX1 VCC 29 VEE     RXCX1
    XRXCX2 VCC 30 VEE     RXCX1
    XRXCX3 VCC 31 VEE     RXCX1
    XRXCX4 VCC 32 VEE     RXCX1
    XR1    35 VEE VCC     RES params: R=130
    XR2    3 2 VCC        RES params: R=203
    XR3    3 4 VCC        RES params: R=203
    XR4    7 VEE VCC      RES params: R=236
    XR5    9 VEE VCC      RES params: R=480
    XR6    14 VEE VCC     RES params: R=480
    XR7    VCC 16 VCC     RES params: R=235
    XR8    VCC 17 VCC     RES params: R=235
    XR9    21 VEE VCC     RES params: R=110
    XR10   22 VEE VCC     RES params: R=232
    XR11   28 VEE VCC     RES params: R=232
    XR12   VCC 3 VCC      RES params: R=203
    XRB1   CE 29 VCC      RES params: R=50
    XRB2   CC 30 VCC      RES params: R=50
    XRB3   SE 31 VCC      RES params: R=50
    XRB4   RE 32 VCC      RES params: R=50
    XRB5   DIN 1 VCC      RES params: R=50
    XRB6   SE 10 VCC      RES params: R=50
    XRB7   RE 12 VCC      RES params: R=50
    XRB8   RE 15 VCC      RES params: R=50
    XRB9   SE 18 VCC      RES params: R=50
    XRP1   CE VEE VCC     RPD params: R=50K
    XRP2   CC VEE VCC     RPD params: R=50K
    XRP3   SE VEE VCC     RPD params: R=50K
    XRP4   RE VEE VCC     RPD params: R=50K
    XRP5   DIN VEE VCC    RPD params: R=50K
.ENDS H131
*****************************************************************************
* THE MC10H188 IS A HEX BUFFER WITH COMMON ENABLE INPUT. THE ENABLE *
* INPUT IS ATTACHED TO TWO EMITTER FOLLOWERS WHICH DRIVE THREE      *
* BUFFERS EACH.                                                     *
* EIN=ENABLE INPUT, DIN=DATA IN, OUT=OUTPUT                         *
*****************************************************************************
.SUBCKT H188  VCC VCCO VBB VBBP VCS VEE EIN DIN OUT
    Q1     VCC 1 2 VEE    T05I2
    Q2     VCC VBBP 2 VEE T04I1
    Q3     2 VCS 3 VEE    T12B1
    Q4     5 2 7 VEE      T08I3
    Q5     7 VCS 8 VEE    T12B1
    Q6     6 VBBP 7 VEE   T08I3
    Q7     VCC 4 6 VEE    T08I2
    Q8     5 VBB 6 VEE    T08I2
    Q9     VCCO 5 OUT VEE T5406
    XR1    3 VEE VCC      RES params: R=121
    XR2    8 VEE VCC      RES params: R=130
    XR3    VCC 5 VCC      RES params: R=286
    XR4    6 VBBP VCC     RESK params: R=16k
    XRXCX1 VCC 1 VEE      RXCX1
    XRB1   EIN 1 VCC      RES params: R=75
    XRB2   DIN 4 VCC      RES params: R=75
```

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    XRP1   EIN VEE VCC    RPD params: R=50K
    XRP2   DIN VEE VCC    RPD params: R=50K
.ENDS H188
*****************************************************************
* THE MC10H189 IS A HEX INVERTER WITH COMMON ENABLE INPUT. THE  *
* ENABLE INPUT IS ATTACHED TO TWO EMITTER FOLLOWERS WHICH DRIVE *
* THREE BUFFERS EACH.                                           *
* EIN=ENABLE INPUT, DIN=DATA IN, OUT=OUTPUT                     *
*****************************************************************
.SUBCKT H189  VCC VCCO VBB VBBP VCS VEE EIN DIN OUT
    Q1     VCC 1 2 VEE    T05I2
    Q2     VCC VBBP 2 VEE T04I1
    Q3     2 VCS 3 VEE    T12B1
    Q4     5 2 7 VEE      T08I3
    Q5     7 VCS 8 VEE    T12B1
    Q6     6 VBBP 7 VEE   T08I3
    Q7     5 4 6 VEE      T08I2
    Q8     VCC VBB 6 VEE  T08I2
    Q9     VCCO 5 OUT VEE T5406
    XR1    3 VEE VCC      RES params: R=121
    XR2    8 VEE VCC      RES params: R=130
    XR3    VCC 5 VCC      RES params: R=286
    XR4  6 VBBP VCC      RESK params: R=16k
    XRXCX1 VCC 1 VEE      RXCX1
    XRB1   EIN 1 VCC      RES params: R=75
    XRB2   DIN 4 VCC      RES params: R=75
    XRP1   EIN VEE VCC    RPD params: R=50K
    XRP2   DIN VEE VCC    RPD params: R=50K
.ENDS H189
*****************************************************************
* THE MC10H210 IS A DUAL 3 INPUT 3 OUTPUT OR GATE. IN1,2,3=DATA IN, *
* OR1,2,3=OR OUTPUTS                                            *
*****************************************************************
.SUBCKT H210  VCC VCCO VBB VCS VEE IN1 IN2 IN3 OR1 OR2 OR3
    Q1    1 5 3 VEE       T32I5
    Q2    1 6 3 VEE       T32I5
    Q3    1 7 3 VEE       T32I5
    Q4    2 VBB 3 VEE     T32I5
    Q5    3 VCS 4 VEE     T30B9
    Q6    VCCO 2 OR3 VEE  T5406
    Q7    VCCO 2 OR2 VEE  T5406
    Q8    VCCO 2 OR1 VEE  T5406
    XR1   VCC 1 VCC       RES params: R=80
    XR2   VCC 2 VCC       RES params: R=80
    XR3   4 VEE VCC       RES params: R=32
    XRB1  IN1 5 VCC       RES params: R=50
    XRB2  IN2 6 VCC       RES params: R=50
    XRB3  IN3 7 VCC       RES params: R=50
    XRP1  IN1 VEE VCC     RPD params: R=50K
    XRP2  IN2 VEE VCC     RPD params: R=50K
    XRP3  IN3 VEE VCC     RPD params: R=50K
.ENDS H210
*****************************************************************
* THE MC10H211 IS A DUAL 3 INPUT 3 OUTPUT NOR GATE. IN1,2,3=DATA IN,*
* OR1,2,3=NOR OUTPUTS                                           *
*****************************************************************
.SUBCKT H211  VCC VCCO VBB VCS VEE IN1 IN2 IN3 NOR1 NOR2 NOR3
    Q1    1 5 3 VEE       T32I5
    Q2    1 6 3 VEE       T32I5
    Q3    1 7 3 VEE       T32I5
    Q4    2 VBB 3 VEE     T32I5
```

```
    Q5    3 VCS 4 VEE      T30B9
    Q6    VCCO 1 NOR3 VEE  T5406
    Q7    VCCO 1 NOR2 VEE  T5406
    Q8    VCCO 1 NOR1 VEE  T5406
    XR1   VCC 1 VCC        RES params: R=80
    XR2   VCC 2 VCC        RES params: R=80
    XR3   4 VEE VCC        RES params: R=32
    XRB1  IN1 5 VCC        RES params: R=50
    XRB2  IN2 6 VCC        RES params: R=50
    XRB3  IN3 7 VCC        RES params: R=50
    XRP1  IN1 VEE VCC      RPD params: R=50K
    XRP2  IN2 VEE VCC      RPD params: R=50K
    XRP3  IN3 VEE VCC      RPD params: R=50K
.ENDS H211
*************************************************************************
*************************************************************************
* The following is a general model for the Resistor. The termperature*
* Coeifficent is 900PPM with Tc1=900 and TC2=0. Inside the DRES model*
* is a formula for calculation of the resistor parasitic capacitance,*
* if the simulator is capable of using it. Otherwise it will have to *
* be hand calculated and inserted at the proper point in the DRES    *
* diode model.One Calculation is for Resistors <2500Ω assuming a     *
* 100Ω/□ sheet RHO, the other for R> 2500Ω assuming 500Ω/□ sheet RHO*
*                                                                    *
*************************************************************************
.SUBCKT RES  A B VCC  params: R=50
*        Assumes Sheet Rho=100Ω/□, Resistor Width=10U, and Cap in Farads.
*        Use for Resistors up to 2500Ω
    Ra  A 1    {R/2} TC=900,0
    Rb  1 B    {R/2} TC=900,0
    D1  1 VCC  DRES
    .MODEL DRES D
      + (IS=3.7E-16
      +  CJO={4.72E-16*R+58E-16})
.ENDS RES
.SUBCKT RESK  A B VCC  params: R=50
* R IS THE RESISTOR VALUE TO BE MODELED.
* Reistor Model for R> 2.5k Ohm.
*It assumes Sheet Rho=500Ω/□, Resistor Width=5U, and Cap in Farads.
    Ra  A 1    {R/2} TC=900,0
    Rb  1 B    {R/2} TC=900,0
    D1  1 VCC  DRES
    .MODEL DRES D
      + (IS=3.7E-16
      +  CJO={0.265E-16*R+29E-16})
.ENDS RESK
.SUBCKT RPD  A B VCC  params: R=50K
    Ra  A 1    {R/2} TC=900,0
    Rb  1 B    {R/2} TC=900,0
    D1  1 VCC  DRPD
    .MODEL DRPD D
      + (IS=3.7E-16
      +  CJO=0.1149P)
.ENDS RPD
.SUBCKT RXCX1  IN OUT VEE
    Q1  OUT 1 OUT VEE  RXCX
    R1  1 IN           1000
    .MODEL RXCX NPN
        + (IS=4.601E-16  BF=85  CJS=.79E-12  RE=0.5
        +  CJE=.65E-12   BR=5   CJC=3.85E-12 RC=24    RB=7084)
.ENDS RXCX1
```

```
.SUBCKT PKG  EXT INT  params: C=1.5P R1=750 R2=0.2 L=3N
    CPKG   82 0    {C}
    RPKG1  EXT 82  {R1}
    RPKG2  82 83   {R1}
    RPKG3  83 INT  {R2}
    LPKG1  EXT 82  {L}
    LPKG2  82 83   {L}
.ENDS PKG
*********************************************************************
*************** MODEL PARAMETERS FOR THE TRANSISTORS ***************
*********************************************************************
.MODEL T04I1 NPN
  + (IS=17.4E-18   BF=112     BR=5      RE=1.8      IKF=.017
  +  ISE=200E-18   RB=63      RBM=0     IRB=0       IKR=54E-5
  +  ISC=76.5E-18  EG=1.11    RC=31     NC=1.141    NR=.995
  +  CJE=54.2E-15  VJE=1.037  MJE=.57   NF=1.0      XTI=4.7
  +  CJC=79.6E-15  VJC=.45    MJC=.27   NE=2.0      XTB=1.15
  +  CJS=122E-15   VJS=.505   MJS=.35   TR=9.9E-9   PTF=16
  +  TF=35E-12     XTF=2.25   VTF=1.67  ITF=.0081   XCJC=.069
  +  FC=0.8        VAF=42     VAR=3.7)
.MODEL T05I2 NPN
  + (IS=21.2E-18   BF=112     BR=5      RE=1.5      IKF=.021
  +  ISE=250E-18   RB=106     RBM=0     IRB=0       IKR=54E-5
  +  ISC=95.6E-18  EG=1.11    RC=27     NC=1.141    NR=.995
  +  CJE=67.7E-15  VJE=1.037  MJE=.57   NF=1.0      XTI=4.7
  +  CJC=99.6E-15  VJC=.45    MJC=.27   NE=2.0      XTB=1.15
  +  CJS=152E-15   VJS=.505   MJS=.35   TR=9.9E-9   PTF=20
  +  TF=35E-12     XTF=2.25   VTF=1.67  ITF=.0081   XCJC=.069
  +  FC=0.8        VAF=42     VAR=3.7)
.MODEL T05I3 NPN
  + (IS=21.2E-18   BF=112     BR=5      RE=1.5      IKF=.021
  +  ISE=250E-18   RB=212     RBM=111   IRB=1.7E-3  IKR=54E-5
  +  ISC=95.6E-18  EG=1.11    RC=27     NC=1.141    NR=.995
  +  CJE=67.7E-15  VJE=1.037  MJE=.57   NF=1.0      XTI=4.7
  +  CJC=99.6E-15  VJC=.45    MJC=.27   NE=2.0      XTB=1.15
  +  CJS=152E-15   VJS=.505   MJS=.35   TR=9.9E-9   PTF=20
  +  TF=35E-12     XTF=2.25   VTF=1.67  ITF=.0081   XCJC=.069
  +  FC=0.8        VAF=42     VAR=3.7)
.MODEL T06B1 NPN
  + (IS=40.2E-18   BF=112     BR=5      RE=1.33     IKF=.028
  +  ISE=492E-18   RB=267     RBM=133   IRB=1.3E-3  IKR=54E-5
  +  ISC=95.6E-18  EG=1.11    RC=27     NC=1.141    NR=.995
  +  CJE=94.3E-15  VJE=1.037  MJE=.57   NF=1.0      XTI=4.7
  +  CJC=12.2E-15  VJC=.45    MJC=.27   NE=2.0      XTB=1.15
  +  CJS=173E-15   VJS=.505   MJS=.35   TR=9.9E-9   PTF=60
  +  TF=35E-12     XTF=2.25   VTF=1.67  ITF=.0081   XCJC=.069
  +  FC=0.8        VAF=42     VAR=3.7)
.MODEL T08I2 NPN
  + (IS=33.3E-18   BF=112     BR=5      RE=1.33     IKF=.034
  +  ISE=1.0E-15   RB=57      RBM=30    IRB=0.3E-3  IKR=115
  +  ISC=184.7E-18 EG=1.11    RC=23     NC=1.085    NR=.995
  +  CJE=99.3E-15  VJE=1.037  MJE=.57   NF=1.0      XTI=4.7
  +  CJC=124.4E-15 VJC=.45    MJC=.27   NE=2.0      XTB=1.15
  +  CJS=170E-15   VJS=.505   MJS=.35   TR=9.9E-9   PTF=60
  +  TF=35E-12     XTF=2.25   VTF=1.67  ITF=.0081   XCJC=.089
  +  FC=0.8        VAF=42     VAR=3.7)
.MODEL T08I3 NPN
  + (IS=33.3E-18   BF=112     BR=5      RE=1.33     IKF=.034
  +  ISE=1.0E-15   RB=222     RBM=111   IRB=1.7E-3  IKR=115
  +  ISC=184.7E-18 EG=1.11    RC=23     NC=1.085    NR=.995
  +  CJE=99.3E-15  VJE=1.037  MJE=.57   NF=1.0      XTI=4.7
```

```
  +  CJC=124.4E-15 VJC=.45    MJC=.27   NE=2.0      XTB=1.15
  +  CJS=170E-15   VJS=.505   MJS=.35   TR=9.9E-9   PTF=60
  +  TF=35E-12     XTF=2.25   VTF=1.67  ITF=.0081   XCJC=.089
  +  FC=0.8        VAF=42     VAR=3.7)
.MODEL T12B1 NPN
  + (IS=75.2E-18   BF=112     BR=5      RE=4        IKF=.056
  +  ISE=931E-18   RB=77      RBM=77    IRB=2.6E-3  IKR=53E-5
  +  ISC=95.6E-18  EG=1.11    RC=26     NC=1.141    NR=.997
  +  CJE=168.5E-15 VJE=1.037  MJE=.57   NF=1.0      XTI=4.7
  +  CJC=174.5E-15 VJC=.45    MJC=.27   NE=2.0      XTB=1.15
  +  CJS=211E-15   VJS=.505   MJS=.35   TR=9.9E-9   PTF=100
  +  TF=35E-12     XTF=2.25   VTF=1.67  ITF=.0081   XCJC=.059
  +  FC=0.8        VAF=42     VAR=3.7)
.MODEL T12B4 NPN
  +  (IS=75.2E-18  BF=112     BR=5      RE=4        IKF=.056
  +  ISE=931E-18   RB=17      RBM=17    IRB=2.6E-3  IKR=53E-5
  +  ISC=95.6E-18  EG=1.11    RC=26     NC=1.141    NR=.997
  +  CJE=168.5E-15 VJE=1.037  MJE=.57   NF=1.0      XTI=4.7
  +  CJC=174.5E-15 VJC=.45    MJC=.27   NE=2.0      XTB=1.15
  +  CJS=211E-15   VJS=.505   MJS=.35   TR=9.9E-9   PTF=100
  +  TF=35E-12     XTF=2.25   VTF=1.67  ITF=.0081   XCJC=.059
  +  FC=0.8        VAF=42     VAR=3.7)
.MODEL T32I5 NPN
  + (IS=1.33E-16   BF=112     BR=5      RE=16       IKF=.134
  +  ISE=4.0E-15   RB=56      RBM=28    IRB=10.4E-3 IKR=24E-5
  +  ISC=7.4E-16   EG=1.11    RC=6      NC=1.141    NR=.997
  +  CJE=6.74E-13  VJE=1.037  MJE=.57   NF=1.0      XTI=4.7
  +  CJC=4.98E-13  VJC=.45    MJC=.27   NE=2.0      XTB=1.15
  +  CJS=6.8E-13   VJS=.505   MJS=.35   TR=9.9E-9   PTF=100
  +  TF=35E-12     XTF=2.25   VTF=1.67  ITF=.0081   XCJC=.059
  +  FC=0.8        VAF=42     VAR=3.7)
.MODEL T30B9 NPN
  + (IS=1.63E-16   BF=112     BR=5      RE=10       IKF=.141
  +  ISE=2.33E-15  RB=31      RBM=28    IRB=6.4E-3  IKR=53E-5
  +  ISC=2.4E-16   EG=1.11    RC=10.5   NC=1.141    NR=.997
  +  CJE=4.2E-13   VJE=1.037  MJE=.57   NF=1.0      XTI=4.7
  +  CJC=4.4E-13   VJC=.45    MJC=.27   NE=2.0      XTB=1.15
  +  CJS=5.28E-13  VJS=.505   MJS=.35   TR=9.9E-9   PTF=100
  +  TF=35E-12     XTF=2.25   VTF=1.67  ITF=.0081   XCJC=.126
  +  FC=0.8        VAF=42     VAR=3.7)
.MODEL T5406 NPN
  + (IS=3.29E-16   BF=112     BR=5      RE=.67      IKF=.372
  +  ISE=4.11E-15  RB=17      RBM=8     IRB=1.0E-2  IKR=53E-5
  +  ISC=95.6E-18  EG=1.11    RC=26     NC=1.141    NR=.997
  +  CJE=7.3E-13   VJE=1.037  MJE=.57   NF=1.0      XTI=4.7
  +  CJC=8.1E-13   VJC=.45    MJC=.27   NE=2.0      XTB=1.15
  +  CJS=6.9E-13   VJS=.505   MJS=.35   TR=9.9E-9   PTF=100
  +  TF=35E-12     XTF=2.25   VTF=1.67  ITF=.0081   XCJC=.126
  +  FC=0.8        VAF=42     VAR=3.7)
.END
```

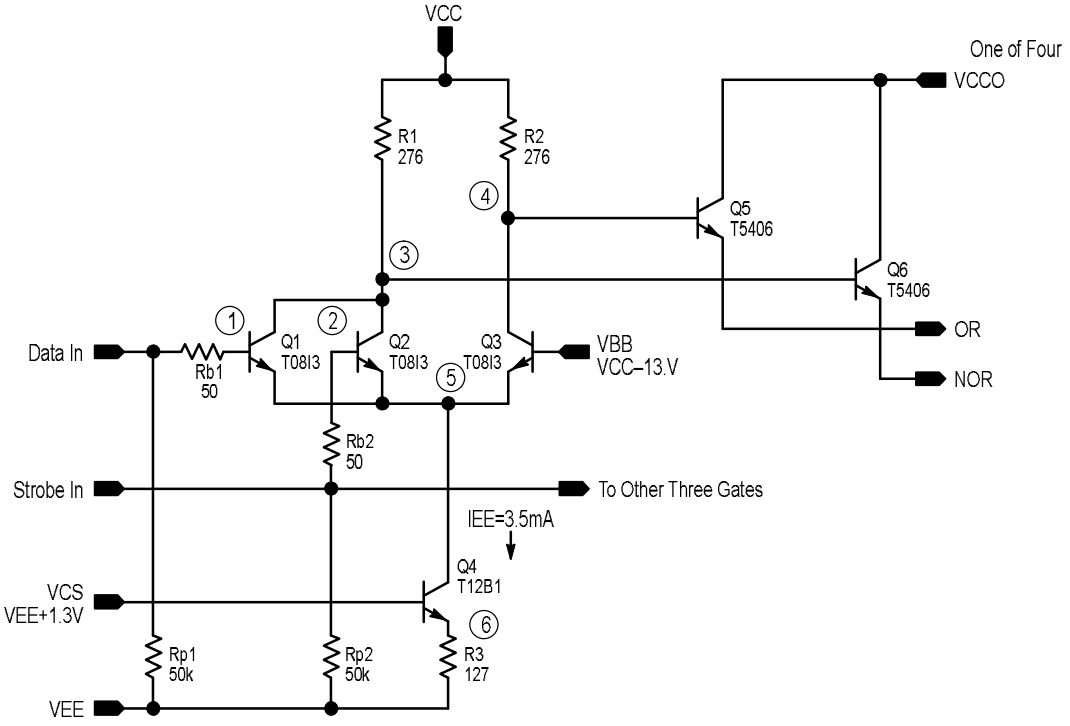

Figure 1. MC10H101 Quad OR/NOR Gate

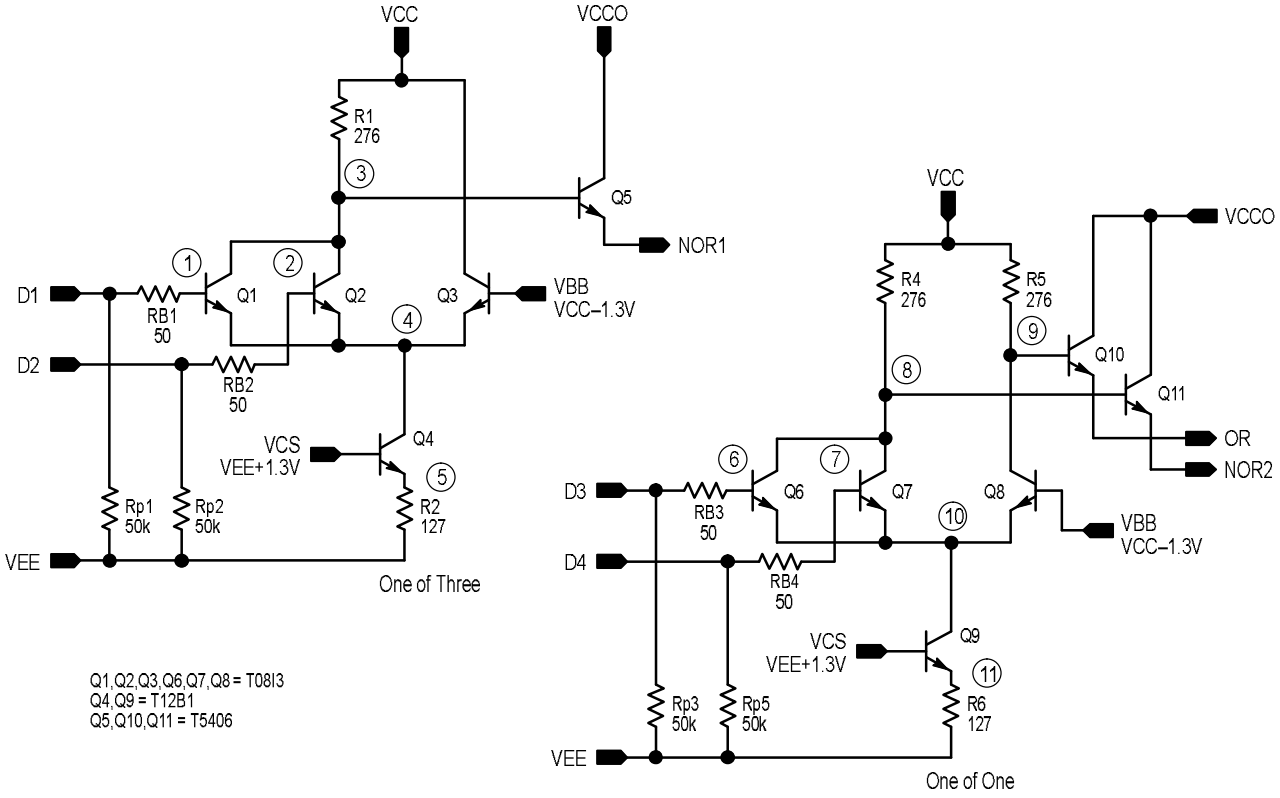

Figure 2. MC10H102 Quad 2–Input NOR Gate

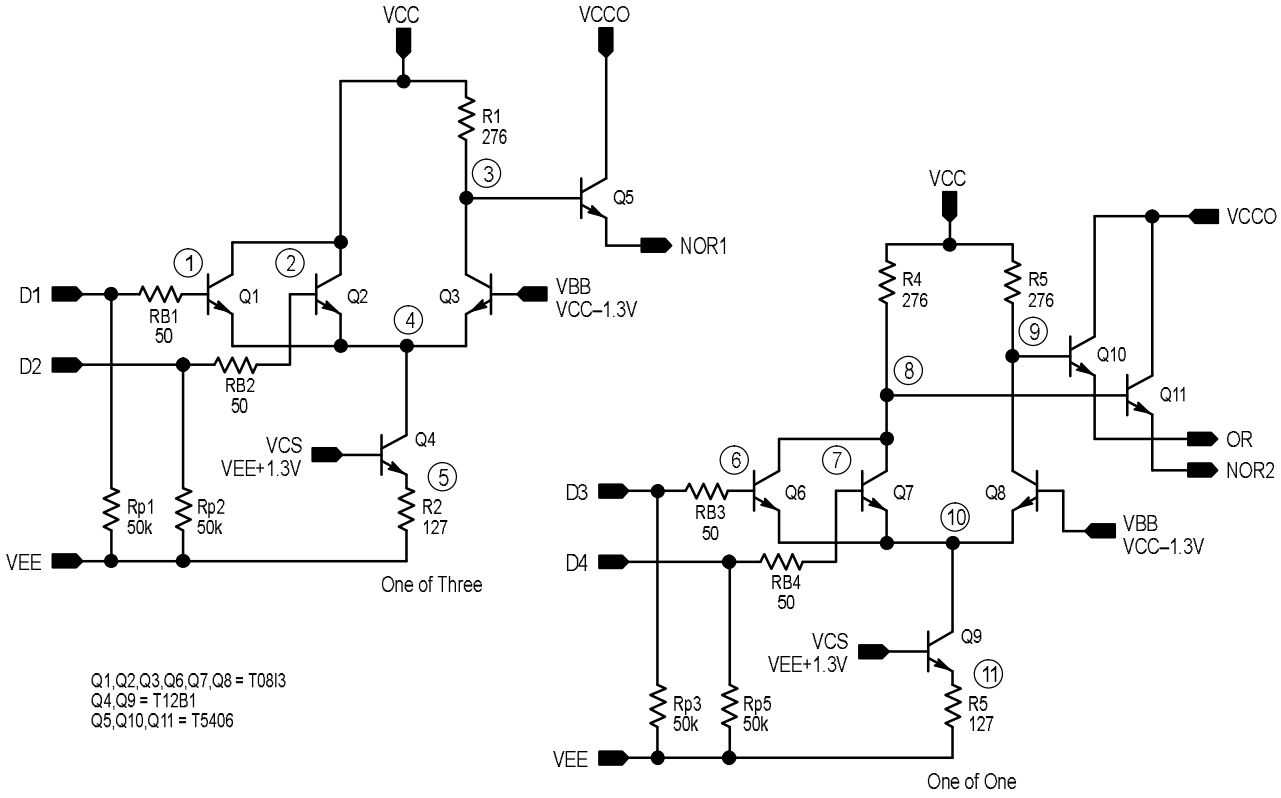

Figure 3. MC10H103 Quad 2–Input OR Gate

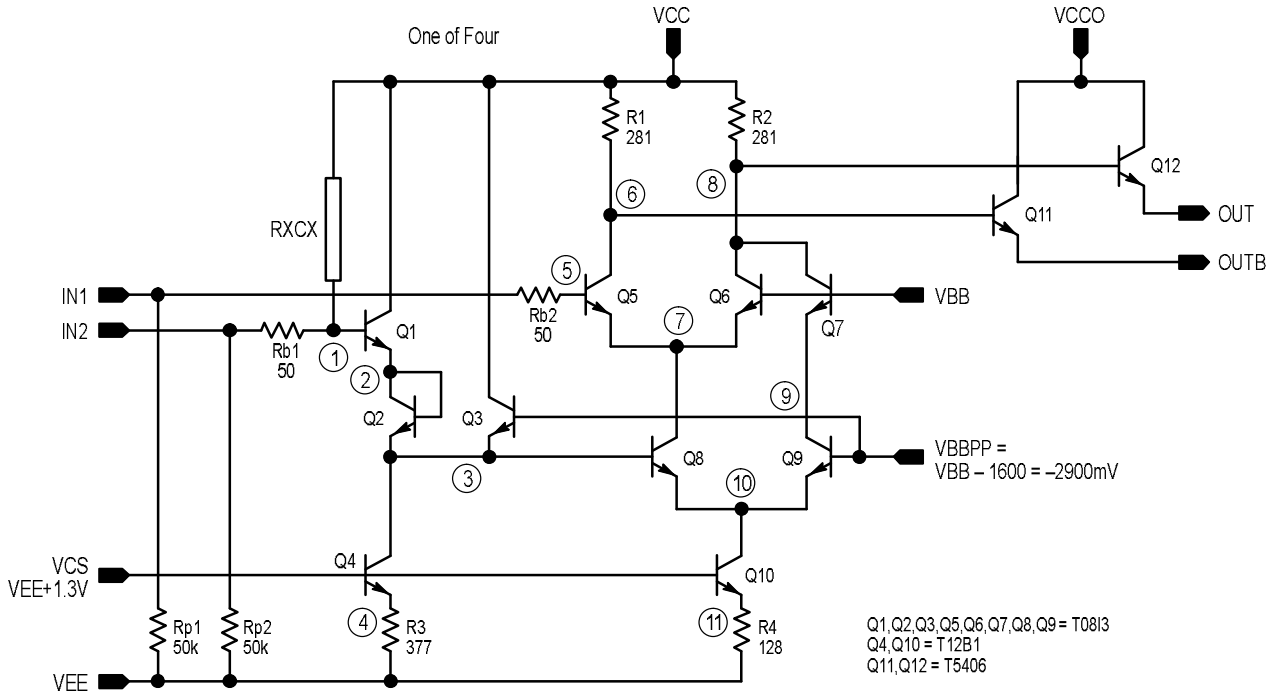

Figure 4. MC10H104 Quad 2–Input AND Gate

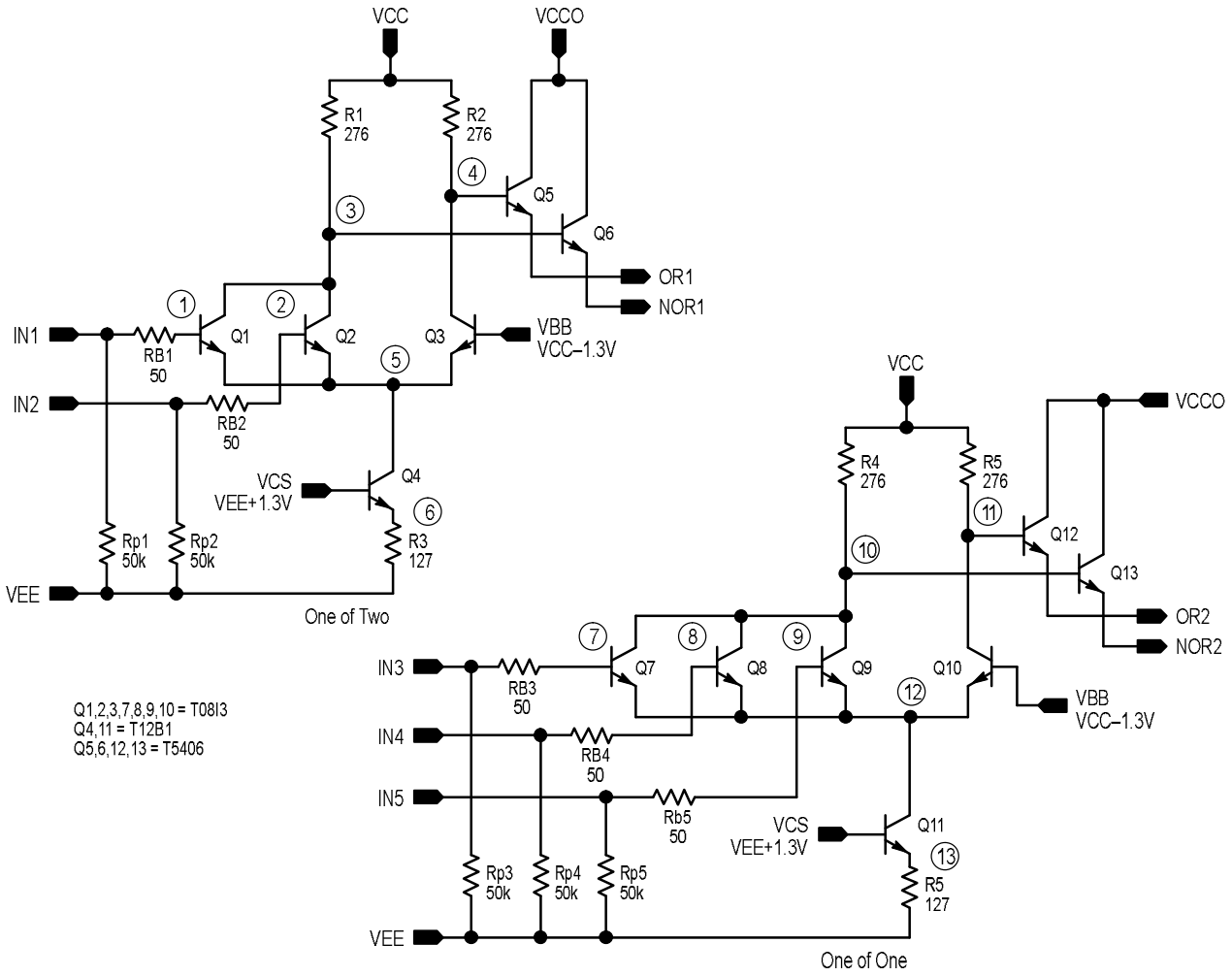

Figure 5. MC10H105 Triple 2–3–2–Input OR/NOR

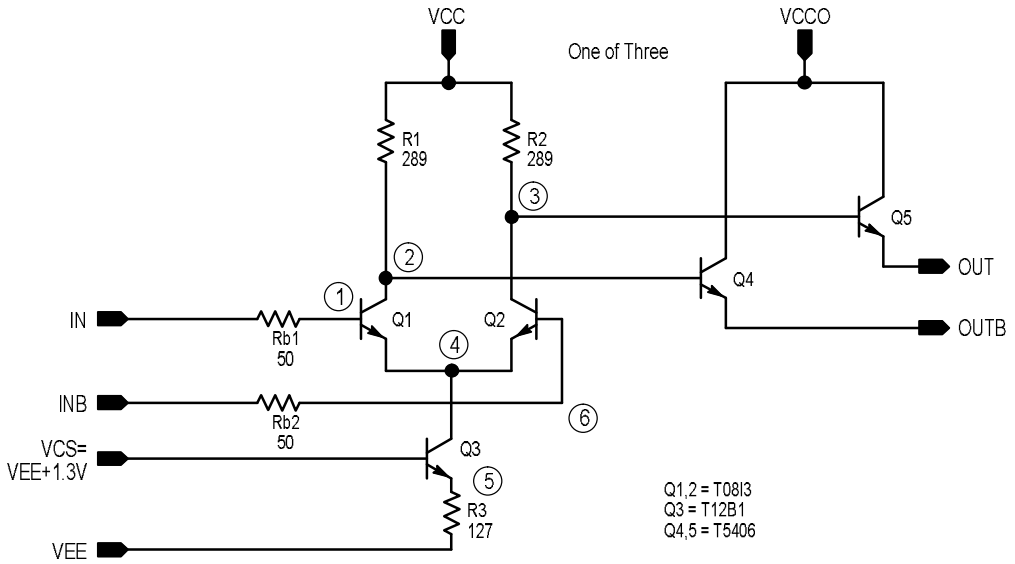

Figure 6. MC10H116 Triple Differential Line Receiver

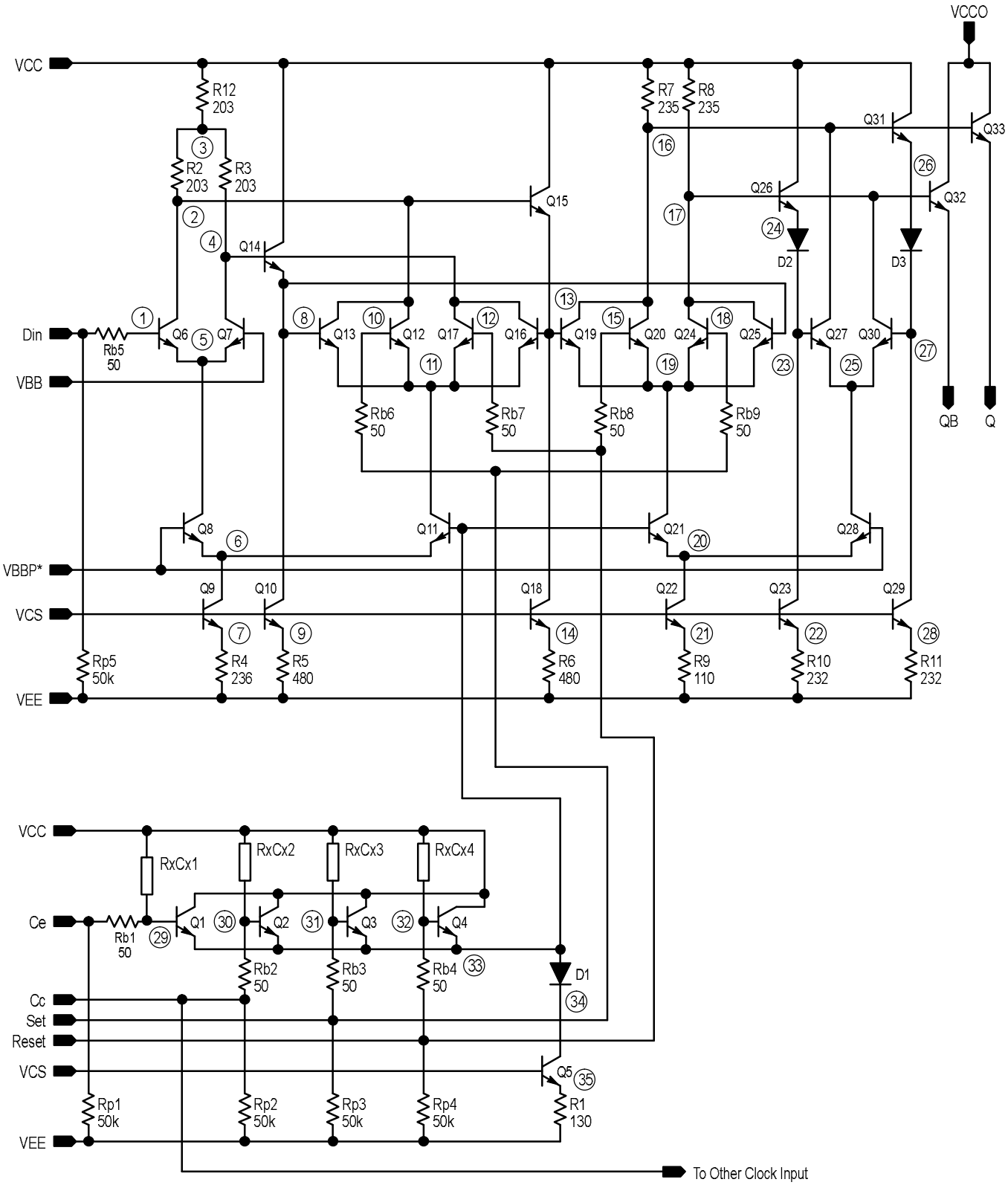

Figure 7. MC10H131 Dual D Flip–Flop

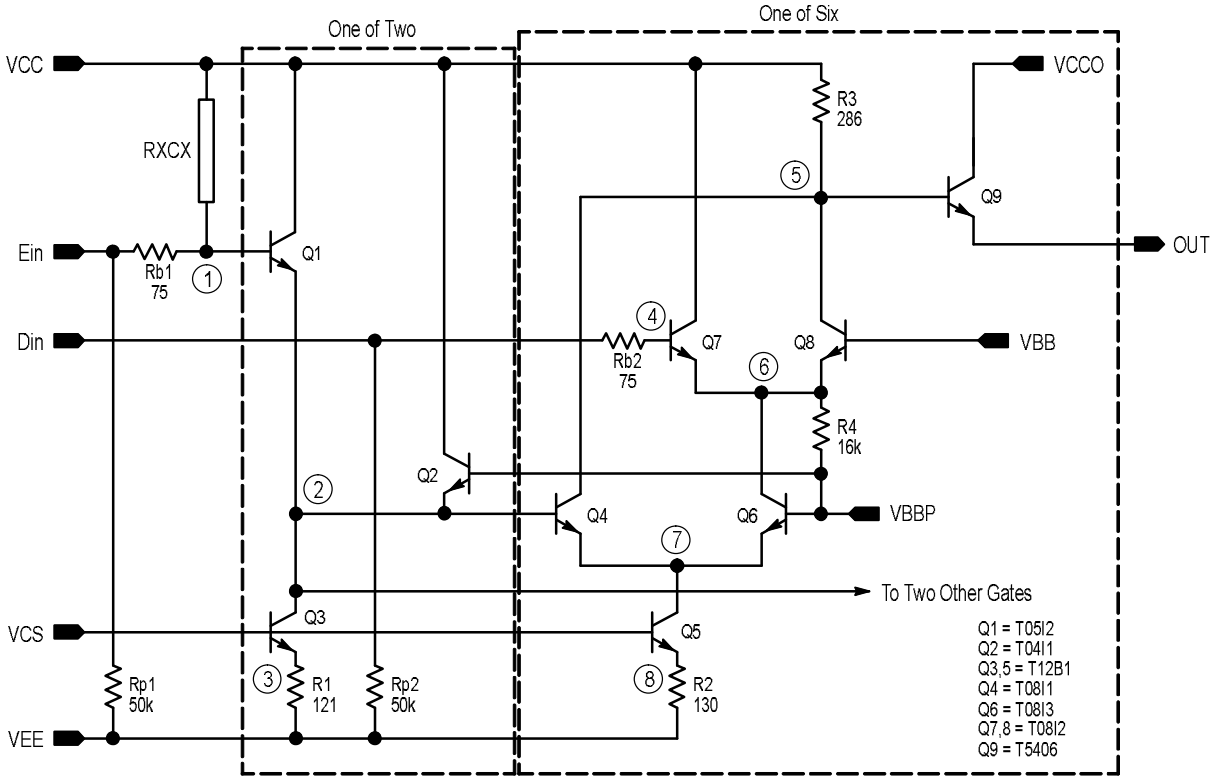

Figure 8. MC10H188

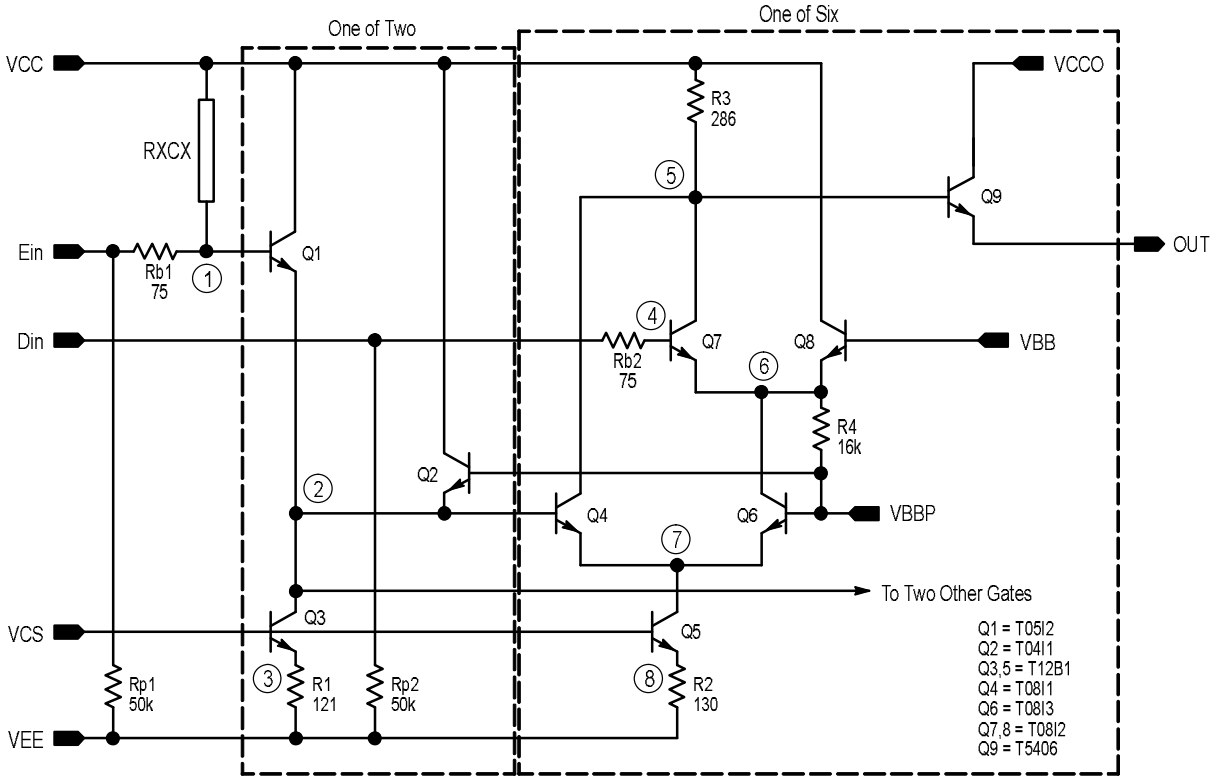

Figure 9. MC10H189

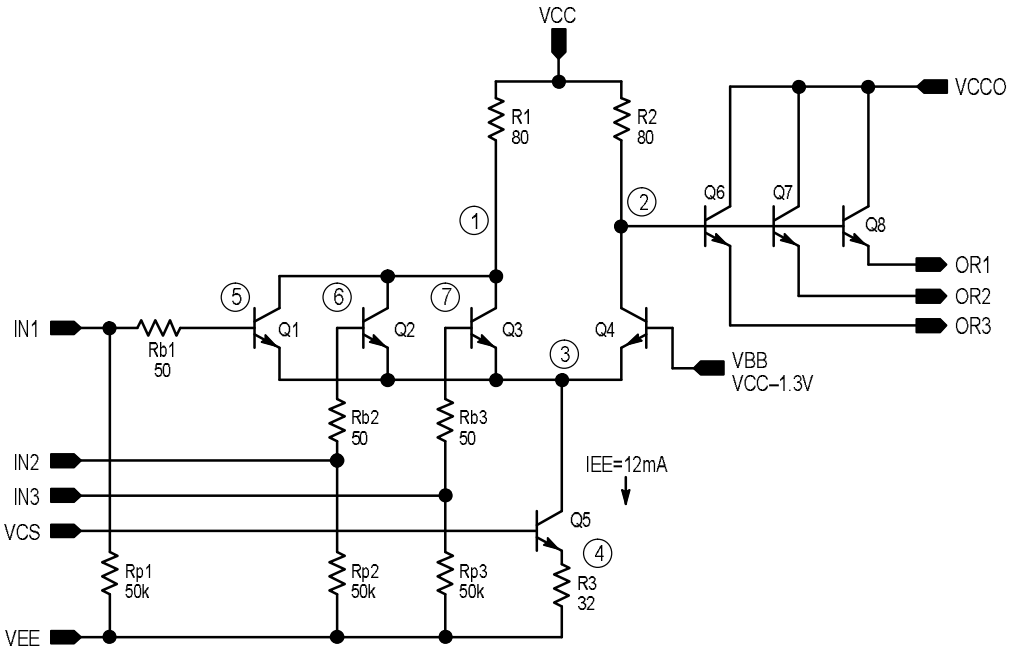

Figure 10. MC10H210 Dual 3–Input/3–Output OR Gate

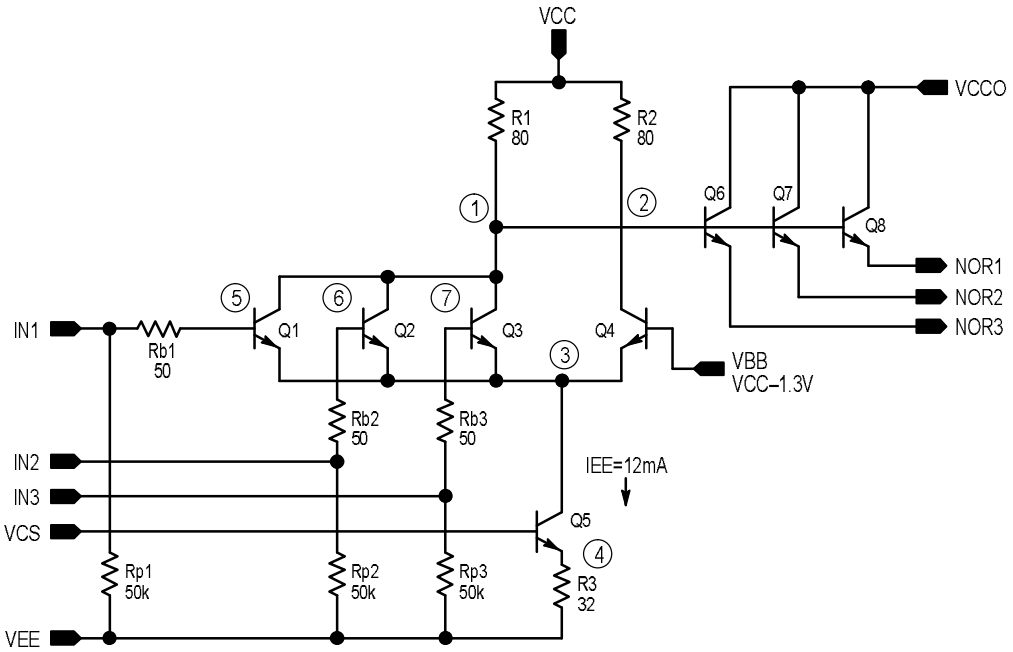

Figure 11. MC10H211 Dual 3–Input/3–Output NOR Gate

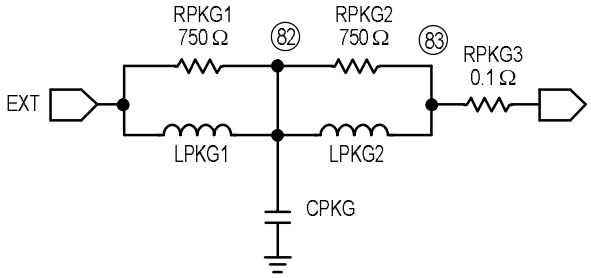

Figure 12. Package Pin Model

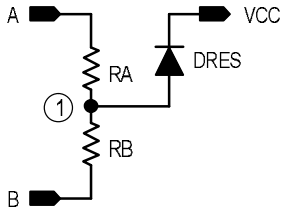

Figure 13. Resistor Model

How to reach us:
USA/EUROPE/Locations Not Listed: Motorola Literature Distribution;
P.O. Box 20912; Phoenix, Arizona 85036. 1–800–441–2447 or 602–303–5454

MFAX: RMFAX0@email.sps.mot.com – TOUCHTONE 602–244–6609
INTERNET: http://Design–NET.com

JAPAN: Nippon Motorola Ltd.; Tatsumi–SPD–JLDC, 6F Seibu–Butsuryu–Center,
3–14–2 Tatsumi Koto–Ku, Tokyo 135, Japan. 03–81–3521–8315

ASIA/PACIFIC: Motorola Semiconductors H.K. Ltd.; 8B Tai Ping Industrial Park,
51 Ting Kok Road, Tai Po, N.T., Hong Kong. 852–26629298