AN569
APPLICATION NOTE

PHASE MEASUREMENT AND CHARACTERIZATION OF RF MICROWAVE POWER TRANSISTORS

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1. ABSTRACT

The continuing efforts to design and produce phased array radar systems have resulted in an increased need for relative insertion phase length data on individual microwave power transistors. The inclusion of insertion phase windows as design specifications for these transistors then becomes necessary to ensure uniform device response.

Until recently, the availability of such phase information on pulsed transistors has not been readily available from device manufacturers. This has been due to the tedious nature of, and inherent errors in, manual phase measurements. With the advent of automated phase instrumentation, the characterization of pulsed transistors can now be performed with a satisfactory degree of confidence, at a rate which will allow high volume testing.

This article outlines an automated method employed for insertion-phase characterization of transistors intended for use in phased array radar systems and presents an overview of some of the phase properties of typical microwave power transistors. The overview of the phase properties includes actual relative insertion phase length data for selected L- and S-band radar transistors.

The phase response to changes in collector bias voltage, input power level, pulsewidth, ambient temperature and operating frequency is presented, and phase sensitivity to a number of fabrication and assembly process parameters is discussed. Much of this phase measurement and analysis work at L-band was funded by the Naval Air Development Center under NADC contracts #N62269-81-C-0829 and #N62269-82-C-0384.

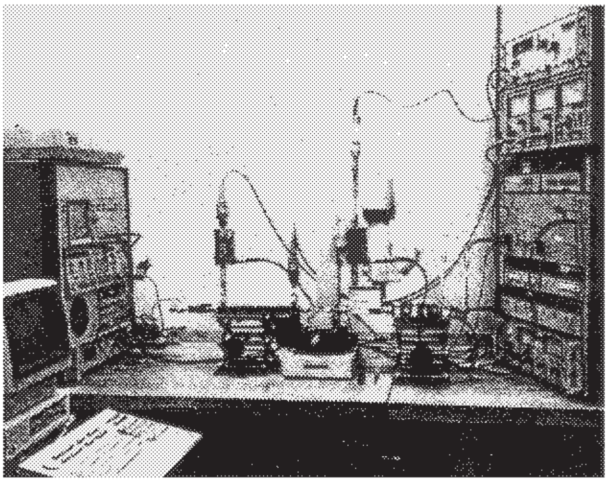
2. INSERTION PHASE MEASUREMENT.

The characterization methods focused on here involve an automated phase measurement system, the heart of which is a state-of-the-art phase discriminator and Hewlett-Packard 9816 computer. The automated system is capable of performing over a frequency range of 500MHz to 4GHz in either a phase-averaging or selective-sampling mode.

In the phase averaging mode, the system allows a rapid measurement of the relative insertion phase during the RF pulse. The instrumentation continually monitors the phase response of the device under test, yielding an average phase value. This measurement technique is sufficient when more detailed information regarding the intra-pulse phase response is not required.

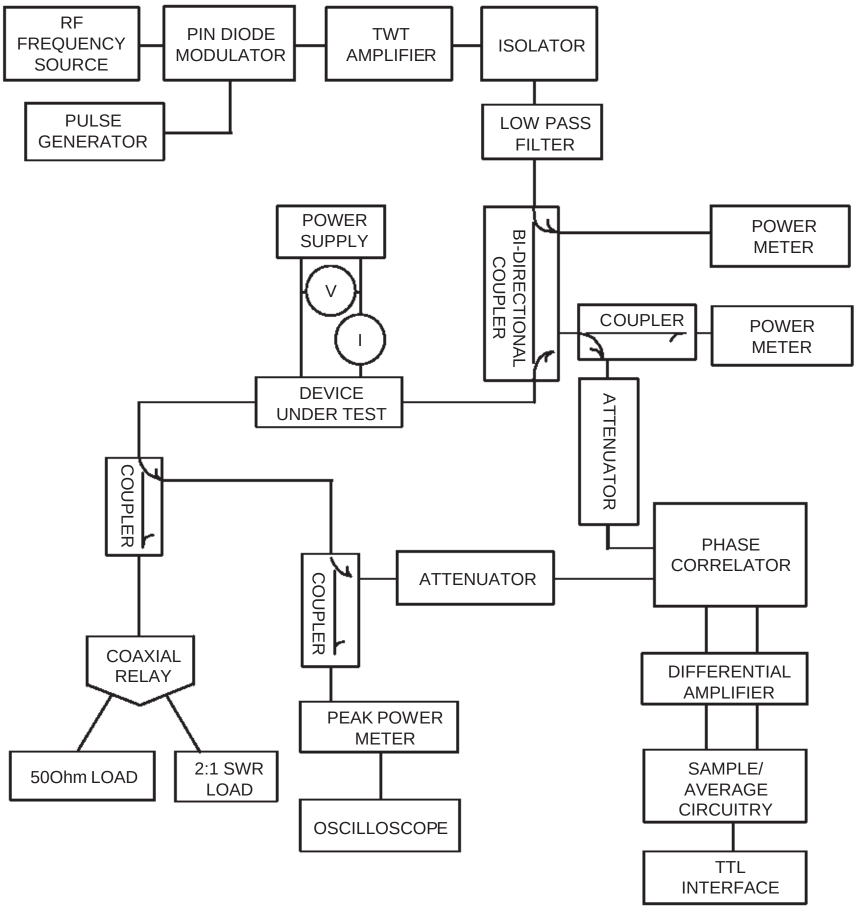
The selective sampling mode permits more detailed analysis of the device’s phase response during the RF pulse. In this mode the phase discriminator is triggered to acquire phase information at specific predetermined points along the RF pulse. A photograph and functional block diagram of one such automated system are shown in figures 1 and 2, respectively (seen on page 2).

Figure 1: A Typical Automated RF Test Set



Note: This RF test set is capable of characterizing a pulsed power microwave transistor. RF power, phase and DC parameters are measured and recorded.

Figure 2: Block Diagram of an Automated RF Test Set



(Please refer to the note on the following page)

Note: The computer-driven setup tests a device over a specified frequency range, recording vital RF and DC data and performing a load pull on the device (if one is required). The TTL interface provides the necessary delay and peak-hold circuitry to allow the computer to instantaneously measure sampled phase information. The software driving the device testing also allows for data to be collected on phase push, with variations in operating conditions and device environment. White equipment blocks in this diagram denote an interface to the controlling HP 9816 computer.

3. PRODUCTION INFLUENCES.

Water processing and assembly parameters must be tightly controlled to ensure a reliable microwave device with consistent power and phase characteristics. This entails, among other things, closely monitored photolithographic and impurity doping techniques and computer-controlled wire bonding of the assembly. The manufacture of the transistor can be broken into two broad categories: wafer fabrication and internal matching/packaging. The relationship between the relative insertion phase length of a transistor and fluctuations in a number of variables, belonging to both categories, is discussed below.

wafer fabrication includes all processes used in transforming a silicon substrate into a useful microwave device. An extensive study (under the NADC contracts mentioned above) was performed on more than 1,000 L-band power transistors (AM81214-060), in an effort to link their phase characteristics to four critical wafer parameters. These were:

- **Donor Concentration:** The doping concentration of the epitaxially-grown layer, which becomes the collector of each device.

- **Collector Epitaxial Layer Thickness:** The thickness of the above region.

- **Electrical Base Width:** A measurement of the sheet resistance of the active base region, which is directly proportional to active base width of the transistor.

- **Emitter Ballast Resistance:** Sheet resistance of the doped polycristalline silicon layer, which forms a distributed series resistance between the emitter junction contact and the metallization in order to ensure uniform power sharing and ruggedness.

Although some phase sensitivity to variations in any and all of the above parameters would be expected, very little correlation was found to exist between them and relative insertion length. This implied transparency is most likely a misleading consequence of the extreme control upon these critical variables.

All the transistors tested were from standard production runs. Current limits on process variations would seem stringent enough to preclude any direct influence they might have on insertion phase from being noted. It can be concluded, therefore, that for an established production process, small variations in wafer fabrication do not result directly in observable deviations in phase length at L-band frequencies. However, a wafer process that is not being adequately controlled, or one that uses procedures that are themselves not reproducible, should be suspected of contributing to phase variations.

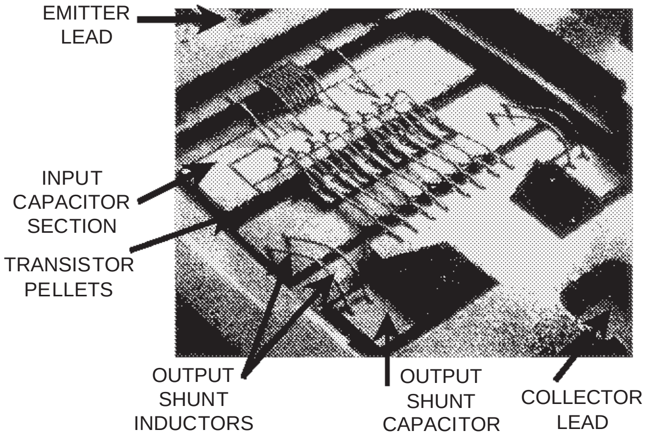
The other aspect of device fabrication, internal matching and packaging, includes the mounting and wire bonding of the individual transistor dice (as many as six single-packaged transistor) and the accompanying matched MOS capacitors within the transistor package.

In the past there has been somewhat of a larger margin for variations in these areas than in wafer processing. If a wafer process parameter is allowed to fall out of an acceptable region, a noticeable, if not catastrophic, change in electrical characteristics would be expected. In such case, the newly-fabricated wafer of transistors would be rejected and scrapped.

In contrast, if an internal mounting were less than perfect, or a bondwire slightly misplaced, the result might appear as a subtle rise in operating temperature from the norm, or as a small shift in terminal impedance of the device in question. Either of these changes might not significantly alter the power-transfer characteristics of the device to the point at which it would fail to meet specifications, but such defects could drastically alter phase characteristics.

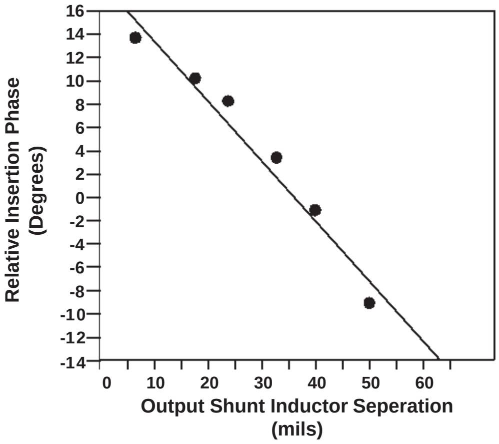
As a case in point, it was found that a ten-mil variation in the spread of the output shunt inductors connecting the collector to an output shunt capacitor in a 60W, L-band device would shift the relative insertion phase length by four to five degrees. A detailed micrograph of the type of transistor used in the study is shown in figure 3.

Figure 3: Photomicrograph of 60W Pulsed L-band Transistor (AM81214-060)



The actual effect of this wirespread variation on the insertion phase for a production L-band transistor is shown in figure 4. Fully automated, programmable computer-wired bonding is able to reduce device-to-device wire-replacement error from device to device to one mil or less, and loop height variation to three mils or less.

Figure 4: Relative Insertion Phase Length vs. Collector Shunt Wire Separation for a Typical Production L-band Transistor (AM81214-060)



Other aspects of transistor assembly considered in this phase study were the placement of the individual piece parts within the package. The locations of input and output MOS capacitor sections, and the transistor pellet, were also measured for the 1,000 L-band transistors.

The absolute and relative variations in the placement of the transistor's components were very slight (typically varying no more than ±1.8mils). No demonstrable correlation to insertion phase could be found.

This accurate, reproducible die-mounting is attributed to the use of in-house designed and built micro-manipulator positioning equipment and experienced operators.

4. OPERATIONAL INFLUENCES.

The transistor in an actual system will not necessarily be operated at optimum design conditions. Under system operation, the transistor bias, input drive level, and possibly the pulse width, may change from the design conditions. To ensure proper phase response of the transistors then requires information on the effect of these parameters.

The shift in the relative insertion phase, as a function of input drive level, transistor bias, and RF modulation is displayed in figures 5, 6 and 7 for a typical S-band power transistor (AM82731-050). As can be seen, the relative insertion phase is more strongly influenced by the input drive level (figure 5) than by the transistor bias (figure 6) or modulation conditions (figure 7).

Figure 5: Relative Insertion Phase Length vs. Input Drive Level for a Typical Production S-band Transistor (AM82731-050)

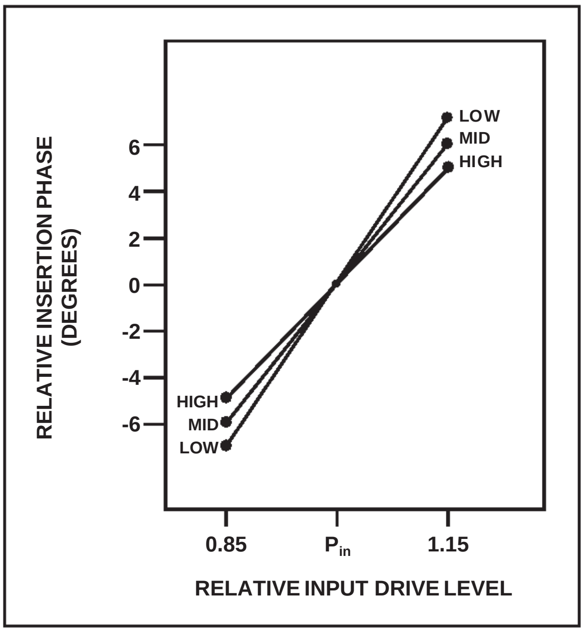


Figure 6: Relative Insertion Phase Length vs. Collector Bias Voltagefor a Typical Production S-band Transistor (AM82731-050)

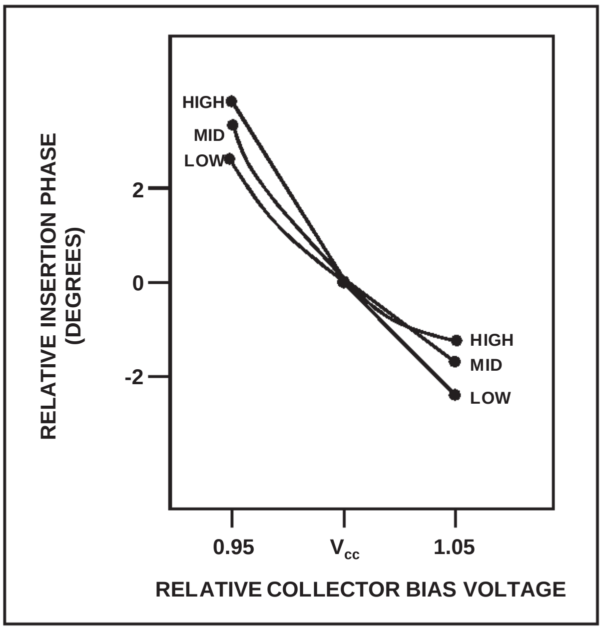


Figure 7: Relative Insertion Phase Length vs. RF Pulse width for a Typical Production S-band transistor (AM82731-050)

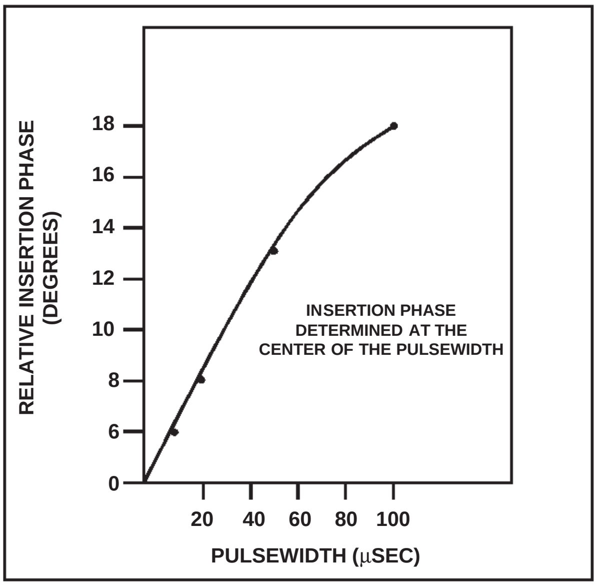
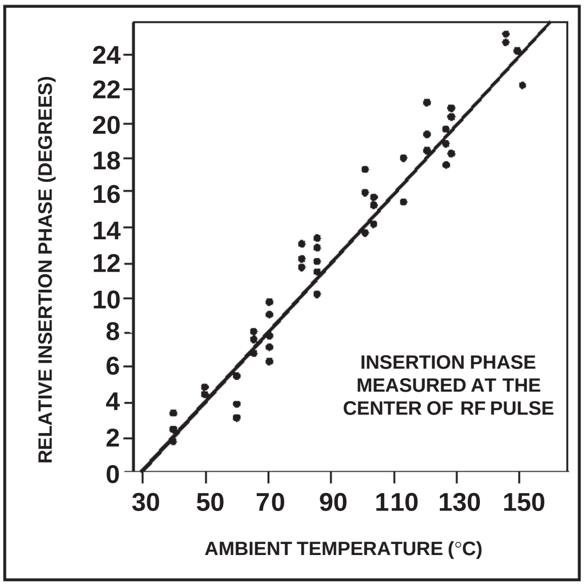


Figure 8: Relative Insertion Phase Length vs. Ambient Temperature for a Typical Production S-band Transistor (AM82731-050)



Preliminary data concerning the phase response over a temperature range, for the same S-band power transistor, is shown in figure 8. The phase, as shown in this figure, changes relatively slowly over temperature (a four-degree phase shift for a 20°C temperature). The phase response indicated no additional sensitivity to changes in the drive level or transistor bias at different ambient temperatures.

The change in the insertion phase during an RF pulse is expressed in terms of the phase settling and phase linearity. The phase settling parameter is a measure of the total change in the insertion phase length from the beginning to the end of the RF pulse. The phase linearity is a measure of the linearity of the phase change, from the beginning to the end of the RF pulse. The fact that the pulse changes during an RF pulse, and that it can be expressed in terms of these two parameters, is attributed to the heating effects in the transistor junction.

As the transistor is turned on, the heat dissipation within the transistor die increases toward a steady state value during the RF pulse. The greatest change in insertion phase during the pulse corresponds to the maximum temperature gradient measured on the transistor die. The maximum temperature and phase gradient both occur in the first ten microsecond point over the remainder of the RF pulse. The abrupt phase shift induced by this transient thermal gradient within the transistor junction should not be confused with the device’s phase response to a shift in the steady-state ambient temperature (discussed in the previous paragraph).

In addition to production variables, the placement and securing of a transistor in a fixture or system can influence the phase response. In a standard transistor fixture, with tolerances of ±2.5mils on a 405-mil channel designed to accept a standard AMPAC, the measured relative insertion phase length can change by as much as three degrees, as a result of transistor position changes upon re-insertion. To minimize this error, care must be taken to uniformly install each transistor in a repeatable fashion, and to keep fixture tolerances (i.e., channel width and depth, board placement and thickness) as controlled as economically feasible.

5. CONCLUSION.

Wafer processes, when closely monitored, and production techniques, with the advent of computer-assisted assembly, can be held to sufficiently tight specifications so as to allow the inclusion of phase as a production test parameter.

The testing of a device by the manufacturer for meeting such a phase specification is now a great deal more practical, due to the use of automated phase-testing equipment. These automated test setups not only increase through-put, but enhance accuracy. The absolute minimum phase window to which a device may be held is going to be dependent upon the particular device geometry in question, as well as on the frequency of operation.

In general, as the frequency increases, so also does the deviation of the relative insertion phase. The phase variation caused by a transistor chip, its associated packaging, and internal matching is generally less than ±15° at each frequency.

This wider phase window is an accommodation for tolerances in external test circuitry and measurement accuracy. However, the system designer must consider the potential phase shifting influences of external circuitry variations, changing bias voltages, and thermal conditions. Naturally, the environment in which a number of phase-matched transistors reside must not itself induce phase variations.

AKNOWLEDGEMENT:

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REFERENCE:

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