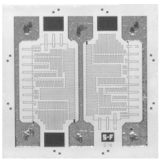
Thin Film Center-Tapped Resistors



Product may not be to scale

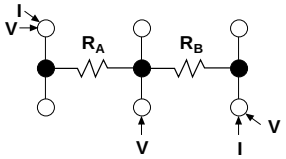
The CTQ series resistor chips offer a wide resistance range with lower shunt capacitance than can be offered with the silicon based resistors but only at a lower power level.
The CTQ offers the designer flexibility in use as either a single value resistor or as two resistor with a center tap feature.
The CTQs six bonding pads allows the user increased layout flexibility.
The CTQs are manufactured using Vishay Electro-Films (EFI) sophisticated thin film equipment and manufacturing technology. The CTQs are 100% electrically tested and visually inspected to MIL-STD-883.

APPLICATIONS

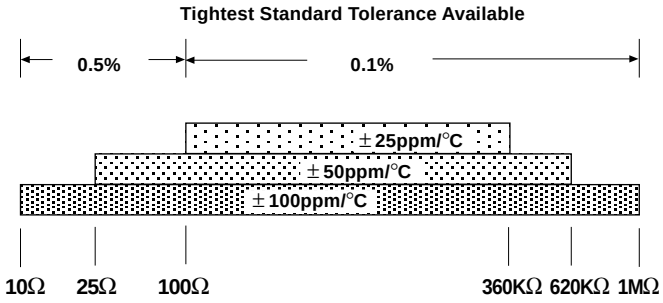
The CTQ center-tapped resistor chips are used mainly in feedback circuits of amplifiers where ratio matching, low shunt capacitance and tracking between two resistors is critical.
For low values, the resistance of the six bonding pad configuration can vary, depending on the method of measurement used. Vishay EFI measures low-value resistors by the four-wire Kelvin technique.

FEATURES

- Center tap feature
- Chip size: 0.030 inches square
- Resistance range total: 10Ω to 1MΩ
- Resistor material: Tantalum nitride, self-passivating
- Moisture resistant
- Quartz substrate
- Low shunt capacitance < 0.1pF



TEMPERATURE COEFFICIENT OF RESISTANCE, VALUES AND TOLERANCES



PROCESS CODE	
CLASS H*	CLASS K*
102	132
100	130
101	131

*MIL-PRF-38534

STANDARD ELECTRICAL SPECIFICATIONS

PARAMETER	
TCR tracking between halves (R_A, R_B)	± 2ppm/°C*
Center tap ratio, R_A/R : Tolerance	1 ± 1% standard
Noise, MIL-STD-202, Method 308 100Ω - 250kΩ < 100Ω or > 251kΩ	 - 35dB typical - 20dB typical
Moisture resistance, MIL-STD-202, Method 106	± 0.5% maximum ΔR/R
Stability, 1000 hours, + 125°C, 30mW	± 0.25% maximum ΔR/R
Operating temperature range	- 55°C to + 125°C
Thermal shock, MIL-STD-202, Method 107, Test condition F	± 0.1% maximum ΔR/R
High temperature exposure, + 150°C, 100 hours	± 0.2% maximum ΔR/R
Dielectric voltage breakdown	400V
Insulation resistance	10^{12} minimum
Operating voltage	200V
DC power rating at + 70°C (derated to zero at + 175°C)	60mW
5 x rated power short-time overload, + 25°C, 5 seconds	± 0.25% maximum ΔR/R

*5ppm/°C for R < 100. 20ppm/°C for R < 20

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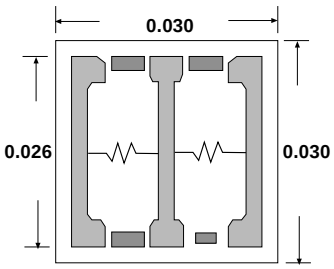
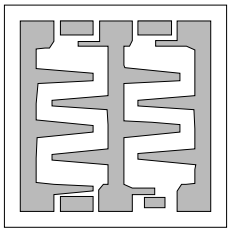
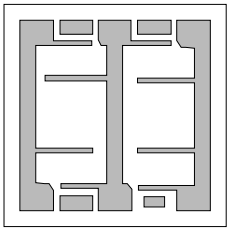
DIMENSIONS in inches



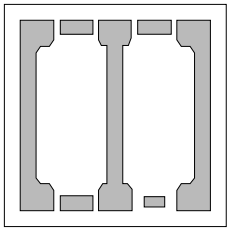
STANDARD CONFIGURATION
Six locations. All pads 0.005 x 0.005 inches



TYPICAL RANGE
10Ω - 26.9Ω



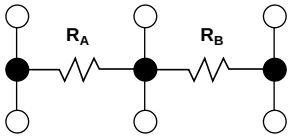
TYPICAL RANGE
27Ω - 99Ω



TYPICAL RANGE
100Ω - 1MΩ

SCHEMATIC

$R_T = R_A + R_B$



MECHANICAL SPECIFICATIONS in inches	
PARAMETER	
Chip size	0.030 x 0.030 ± 0.002 (0.762 x 0.762 ± 0.05mm)
Chip thickness	0.010 ± 0.003 (0.254 ± 0.05mm)
Chip substrate material	Quartz
Resistor material	Tantalum Nitride, self-passivating
Bonding pad size	0.005 x 0.005 (0.127 x 0.127mm)
Number of pads	6
Pad material	10kÅ minimum aluminum
Backing	None, lapped quartz

OPTIONS: Alphanumeric part marking, up to six characters
Gold bonding pads, 15kÅ minimum
Center-tap ratio tolerances to 0.05%
1 to 10 ohm values available
Contact Applications Engineer

ORDERING INFORMATION

Example: 100% visualled, 10kΩ, ± 1%, ± 100ppm/°C TCR, Aluminum Pads, Class H

P/N:	**W**	**CTQ**	**101**	**1000**	**1**	**F**
	INSPECTION /PACKAGING	PRODUCT FAMILY	PROCESS CODE	RESISTANCE VALUE	MULTIPLIER CODE	TOLERANCE CODE
	W = 100% visually inspected parts per MIL-STD-883 loaded in matrix tray **X** = Sample, visually inspected loaded in matrix trays (4% AQL)		See Process Code table	Use first 4 significant digits of resistance (Rt)	**D** = 0.0001 **C** = 0.001 **B** = 0.01 **A** = 0.1 **0** = 1 **1** = 10 **2** = 100 **3** = 1000 **4** = 10000	**B** =0.1% **C** =0.2% **D** = 0.5% **F** = 1.0% **G** = 2.0% **H** = 2.5% **J** = 5.0% **K** = 10% **M** = 20% **L** = 25%

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