AT&T Microelectronics

LB1013 High-Voltage Dual Op Amp

Features

- Operates from 5 V to 85 V
- Dual or single power supply operation
- Programmable output currents up to ±80 mA
- 90 V minimum breakdown, complementary bipolar monolithic IC
- Operating temperature of –25 °C to +100 °C

Applications

- Transconductance amplifier for telephone line feed or driver
- Medium power audio amplifiers
- Voltage follower/buffer
- Control system solenoid or relay driver
- Telephone line ringing signal generator

Description

The LB1013AD High-Voltage Dual Op Amp is a monolithic silicon integrated circuit that is fabricated in a junction-isolated, complementary bipolar process that provides PNP transistors with symmetric performance to the NPN. The amplifiers are internally compensated for unity-gain stability and designed for operation in the audio band. A programming pin provides access for setting performance levels, power supply consumption, or logic turn-on/turn-off. Positive power supply pins can be tied together or used to supply input and output stages separately, or to power up one amplifier without the other.

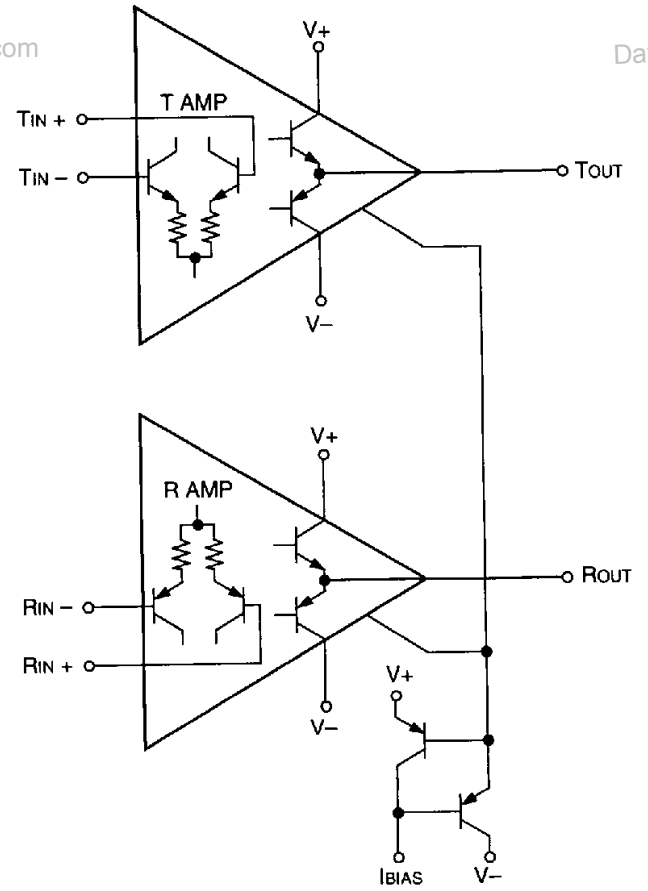


Figure 1. Functional Diagram

Pin Information

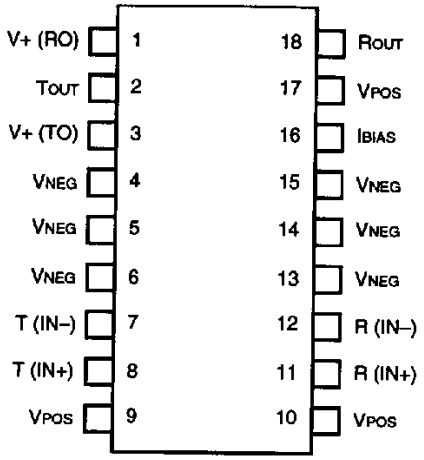


Figure 2. Pin Diagram

Table 1. Positive Supply Pins

Pin	Symbol	Description
1	V+ (RO)	Positive supply to the output stage of R amplifier.
3	V+ (TO)	Positive supply to the output stage of T amplifier.
9	VPOS	Positive supply to T amplifier input stage.
10	VPOS	Positive supply to both T and R amplifier input stages and to programming pin circuitry.
17	VPOS	Positive supply to R amplifier input stage and to programming pin circuitry.

Table 2. Negative Supply/Ground Pins

Pin	Symbol	Description
4, 5, 6, 13, 14, 15	VNEG	These pins provide redundant electrical continuity to the most negative circuit potential. All of these pins should be connected to ensure satisfactory heat dissipation, although only one pin is required to provide electrical continuity.

Table 3. Programming Bias Pin

Pin	Symbol	Description
16	IBIAS	A current source or a suitable value programming resistor (see Figure 7, Note 2) can be connected to this pin. A negative current flow from this pin must be present before the LB1013AD device becomes operational. The peak output current for sinking in the T amplifier and sourcing in the R amplifier is greater than 1000 times IBIAS (see Typical Device Characteristics).

Table 4. Input/Output Pins

Pin	Symbol	Description
2	TOUT	Output of the T amplifier. Peak current through this pin should not exceed 80 mA, source or sink.
7 8	T(IN–) T(IN+)	These pins are the inverting and noninverting inputs, respectively, for the differential input stage of the T amplifier.
11 12	R(IN+) R(IN–)	These pins are the inverting and noninverting inputs, respectively, for the PNP differential input stage of the R amplifier. The LB1013AD uses vertical PNP transistors with ac and dc characteristics well matched to the NPNs.
18	ROUT	Output of the R amplifier. Peak output current through this pin must not exceed 80 mA, source or sink.

Absolute Maximum Ratings (At 25 °C)

Stresses in excess of the Absolute Maximum Ratings can cause permanent damage to the device. These are absolute stress ratings only. Functional operation of the device is not implied at these or any other conditions in excess of those given in the operational sections of the data sheet. Exposure to Absolute Maximum Ratings for extended periods of time can adversely affect device reliability.

Parameter	Symbol	Min	Max	Unit
Ambient Operating Temperature	T_A	–25	+100	°C
Storage Temperature Range	T_{stg}	–40	+125	°C
Pin Soldering Temperature (t = 15 s max)	T_S	—	+300	°C
Voltage (V_{POS} to V_{NEG})	—	—	+85	V
Power Dissipation*	P_{DISS}	—	+2	W
Differential Input Voltage (See Application Precautions.)	—	–5	+5	V

* Care in mounting and environment is required to keep junction operating temperature acceptably low. The package of this device has a thermal resistance (Θjc) of approximately 20 °C/W. The thermal resistance of the wiring board mounting plane to ambient should not exceed 30 °C/W for normal applications. On the printed-circuit board, make the V_{NEG} leads as wide as possible. Also, maximize the amount of printed-circuit board copper in the area of and specifically on the leads connected to this device for the lowest operating temperature. Forced-air circulation or high-thermal conductivity wiring boards may be required.

Typical Device Characteristics (T_A = 25 °C)

Typical values are characteristics of the device and are the results of engineering evaluations. Typical values are for information purposes only and are not part of the testing requirements. Positive current is defined as flowing into the device.

Characteristic	I_{BIAS} = 40 A	I_{BIAS} = 80 µA
Slew Rate	2 V/µs	4 V/µs
Output Current	±40 mA	±80 mA
Power Supply Rejection Ratio (PSRR)	80 dB	80 dB

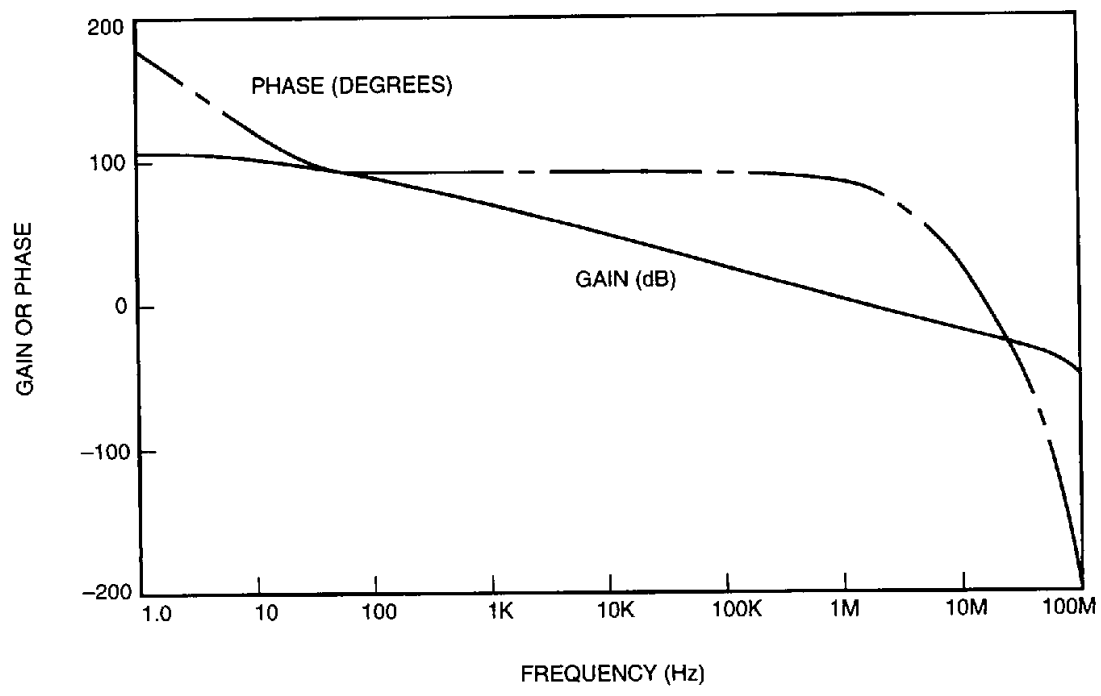


Figure 3. Frequency/Gain Response Curve

Electrical Characteristics

T = 25 °C, V_{POS} = 25 V; V_{POS} = –25 V, I_{BIAS} connects through a 1.25 MΩ resistor to V unless otherwise specified. Minimum and maximum values are testing requirements.

Parameter	Test Condition	Min	Max	Unit
Open-loop Gain	f = 100 Hz	75	—	dB
	f = 1 kHz	55	—	dB
Input Offset Voltage	—	—	±5.0	mV
Input Bias Current	Inverting and noninverting pins	—	±1.0	µA
Input Offset Current	—	—	±1.0	µA
Common-mode Rejection Ratio	V_{POS} = 30 V, V_{NEG} = –30 V, VCM = 0 ±20 V	80	—	dB
Output Voltage Swing T Amplifier:	V_{POS} = 38 V, V_{NEG} = –38 V, noninverting input = Gnd,			
V_{HIGH}	ΔV (inverting input = ±0.5 V),	35.6	—	V
V_{LOW}	I_{BIAS} = 40 µA, R_L = 1 kΩ	–35.4	—	V
Output Voltage Swing R Amplifier:	V_{POS} = 38 V, V_{NEG} = –38 V, noninverting input = Gnd,			
V_{HIGH}	ΔV (inverting input = ±0.5 V),	35.4	—	V
V_{LOW}	I_{BIAS} = 40 µA, R_L = 1 kΩ	–35.6	—	V
Power Supply Currents (amplifiers activated under no-load conditions)	V_{POS} = 35 V, V_{NEG} = 35 V (See Figure 5.)			
	I_{VPOS}	—	1.1	mA
	I_{VNEG}	—	–1.1	mA
Power Supply Leakage Current (amplifiers off)	V_{POS} = 35 V, V_{NEG} = –35 V, I_{BIAS} = open (See Figure 5.)			
	I_{VPOS}	—	±10	µA
	I_{VNEG}	—	±10	µA
Output Leakage Current (amplifiers off)	V_{POS} = 35 V, V_{NEG} = –35 V, I_{BIAS} = open (See Figure 4.)			
	V_{LOAD} = 30 V	—	±10	µA
	V_{LOAD} = 30 V	—	±10	µA
T_{OUT} to V_{POS} Fault Current	V_{LOAD} = 35 V, t = 100 ms (See Figure 6.)	41	47	mA
T_{OUT} to V_{NEG} Fault Current	V_{LOAD} = –35 V, t = 100 ms (See Figure 6.)	–41	–47	mA
R_{OUT} to V_{POS} Fault Current	V_{LOAD} = 35 V, t = 100 ms (See Figure 6.)	41	47	mA
R_{OUT} to V_{NEG} Fault Current	V_{LOAD} = –35 V, t = 100 ms (See Figure 6.)	–41	47	mA

Simplified Test Circuits

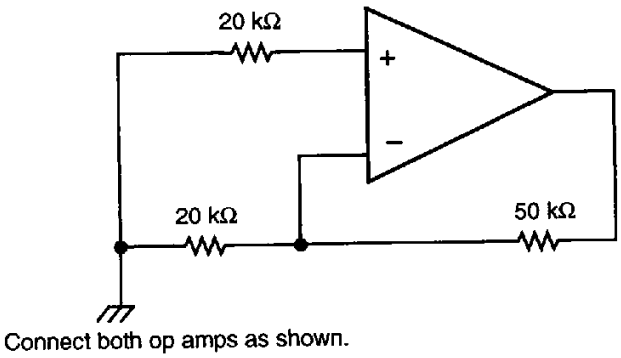


Figure 4. Output Leakage Current

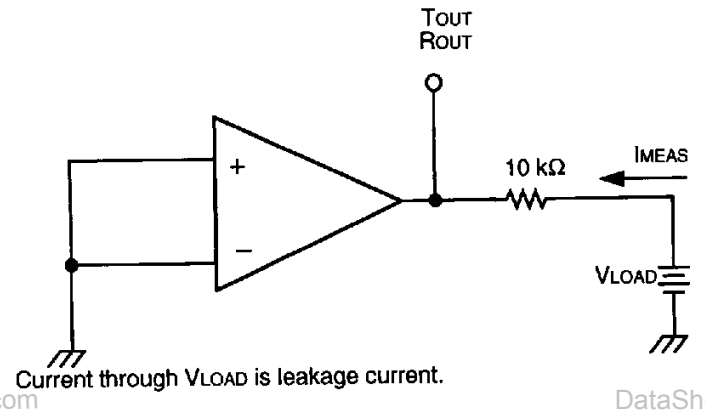


Figure 5. Power-Supply Current

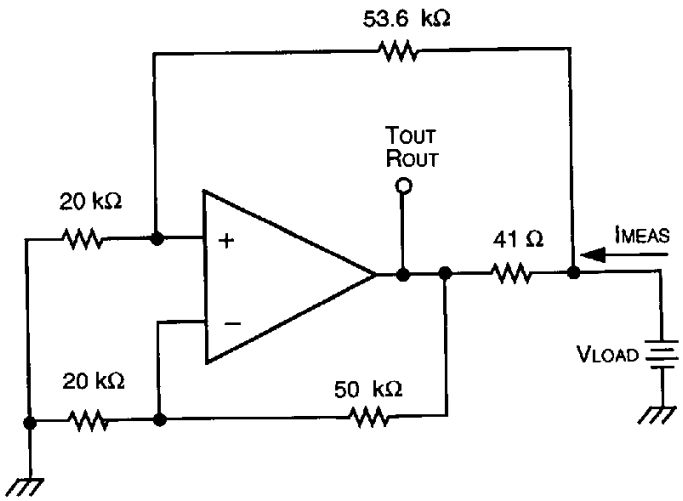
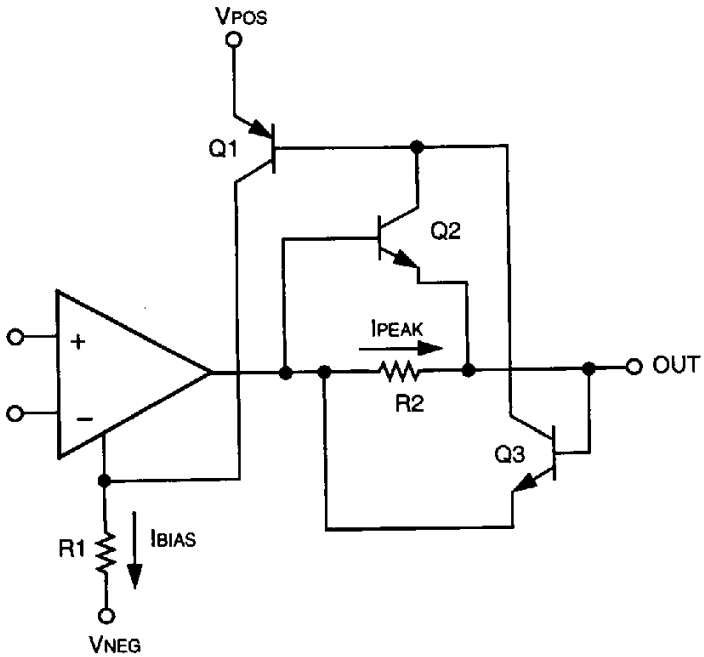


Figure 6. Fault Current

Short-Circuit Protection

The outputs of the LB1013AD device can be protected from short circuits by using the external circuitry shown in Figure 6.



Notes:

1. Q1, Q2, Q3; $V_{(BR)CEO} > 90$ V.
2. $R1 = \frac{V_{POS}\,(Pin17) - V_{NEG} - 1.2\ V}{I_{BIAS}}$.
3. $R2 = \frac{0.6\ V}{I_{PEAK}}$.

Figure 7. External Circuitry

Applications

The simplified schematic outlined in Figure 8 illustrates an application as a transconductance amplifier for a telephone line drive. Other applications include high-voltage/power-voltage followers and audio amplifiers and circuits where high-voltage, high-power op amp capabilities are required. The equations relating to the circuit outlined in Figure 8 are as follows:

For R1 & R2 >> R3

$$I_T = \frac{V_C - V_D}{R1} \times \frac{R2}{R3}$$

$$I_R = -\frac{V_C - V_D}{R1} \times \frac{R2}{R3}$$

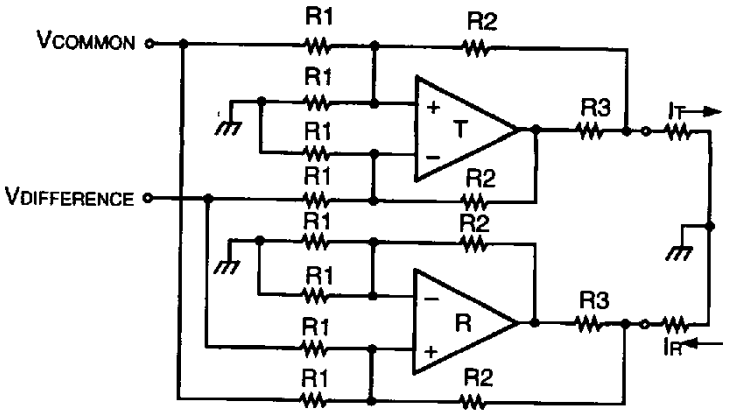


Figure 8. Simplified Line-Feed Operation
(power-supply connection not shown)

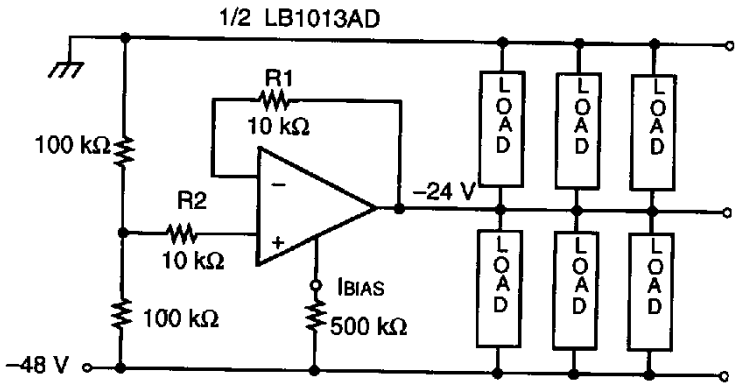


Figure 9. Typical Voltage Follower

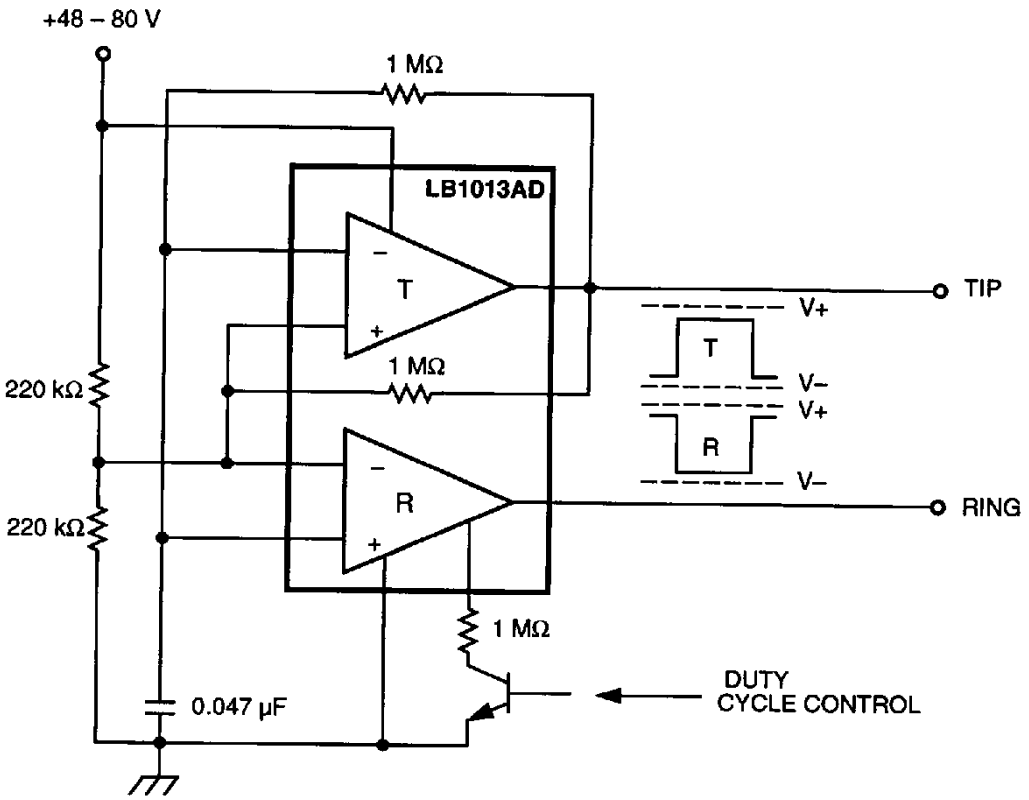


Figure 10. Dual Op Amp Solid-State Differential Signal Generator

Applications (continued)

Certain precautions are necessary to prevent this device from latching and from going into an oscillation-clipping mode.

Latching Prevention

If the differential input voltage exceeds 5.0 V (breaking down the input transistor) and the power-supply voltage exceeds 30 V, the output of the T amplifier can latch to the positive-supply rail and the R amplifier can latch to the negative power-supply rail. This latching can occur in an op amp that is connected in the unity-gain configuration when a voltmeter or load is connected to the output. In this case, the capacitance of the voltmeter or ground can cause a temporary overload of the input, causing the latch to occur. The following practices are recommended for the prevention of latching modes:

1. The power supply voltages should be removed or reduced below 30 V before connections are either made or removed from the LB1013AD device.
2. It is a good practice to place a resistor (R1, Figure 9) between the resistor of equal value (R2, Figure 9) and any external connections. The value of these resistors should be between 1 kΩ and 10 kΩ.
3. Differential input voltage should not exceed ±5.0 V.

Clipping

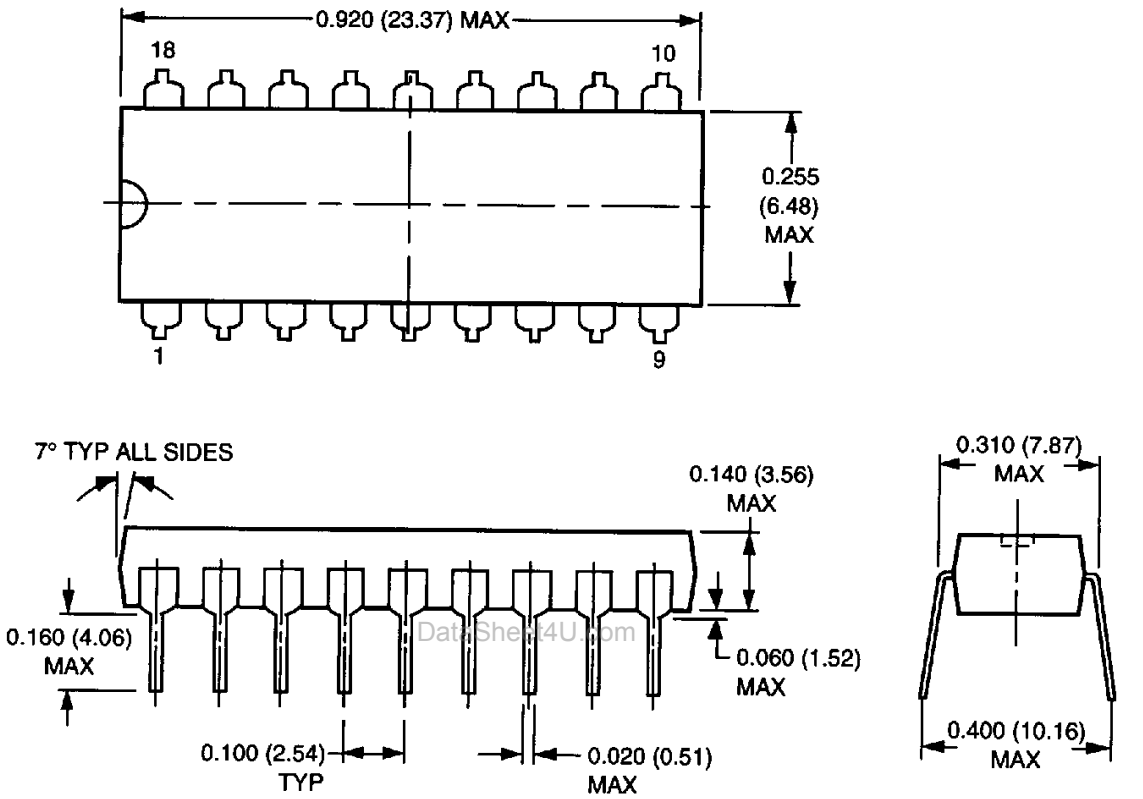
The T amplifier of the LB1013AD device has an NPN input stage, and the R amplifier has a PNP input stage. Thus, the common-mode input voltage range of the two amplifiers is different with the T amplifier being more positive and the R amplifier being more negative. If the outputs of the T and R amplifiers are allowed to come within 3.4 V of the negative and positive supply voltages, respectively, the outputs will begin clipping. The clipped portion of the waveform exhibits an oscillation.

Oscillation will not occur in circuits where the common-mode input voltage of the T amplifier is closer to the positive supply voltage; the common-mode input voltage of the R amplifier is closer to the negative supply voltage, and the signal only causes clipping in one polarity. In this case, clipping starts when the output voltage comes within 2 V of the supply rail.

Outline Drawings

Dimensions are in inches and (millimeters).

18-Pin, Plastic DIP



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Packaging and Ordering Information

Throughout this section the following abbreviations are used:

DIP — Dual in-line package; SOG — Small-outline gull wing; SOJ — Small-outline J-lead; SONB — Small-outline narrow body; PLCC — Plastic leaded chip carrier.

Device Code	Package Type	Temperature
ATTL7551AP	44-Pin PLCC	–40 °C to +85 °C
ATTL7551AF	24-Pin DIP	–40 °C to +85 °C
ATTL7554AP	44-Pin PLCC	–40 °C to +85 °C
ATTL7556AAU	32-Pin PLCC	–40 °C to +85 °C
ATTL7557AAU		
ATTL7561AP	44-Pin PLCC	–40 °C to +85 °C
ATTL7564AP		
ATTL7581AC/BC	16-Pin DIP	–40 °C to +85 °C
ATTL7581AAE/BAE	16-Pin Plastic SOG	–40 °C to +85 °C
ATTL7582AE/BE	16-Pin Plastic DIP	–40 °C to +85 °C
ATTL7582AAE/BAE	16-Pin Plastic SOG	–40 °C to +85 °C
ATTL7583AF/BF	24-Pin Plastic DIP (600 mil)	–40 °C to +85 °C
ATTL7583ACG/BCG	24-Pin Plastic DIP (300 mil)	–40 °C to +85 °C
ATTL7583AAJ/BAJ	28-Pin Plastic SOG	–40 °C to +85 °C
ATTL7590AAF	14-Pin	–40 °C to +85 °C
ATTL7591AB	8-Pin, DIP	–40 °C to +85 °C
ATTL7591AS	8-Pin, SONB	–40 °C to +85 °C
LB1011AB	8-Pin, DIP	–20 °C to +70 °C
LB1013AD	18-Pin, DIP	–25 °C to +85 °C
LB1060AB	8-Pin, DIP	–40 °C to +65 °C
LB1201AB	8-Pin, DIP	–40 °C to +85 °C
LB1201AS	8-Pin, SONB	–40 °C to +85 °C
LB1208AAJ	28-pin SOG	–40 °C to +85 °C
LB1276AP	44-Pin PLCC	–40 °C to +85 °C
LB1276AF	24-Pin DIP	–40 °C to +85 °C
LB1356AF	24-Pin DIP	–40 °C to +85 °C
LH1263AR	20-Pin Plastic DIP	–40 °C to +85 °C
LH1571AB	8-pin Plastic DIP	–40 °C to +85 °C
LH1571AAC	8-pin SOG	–40 °C to +85 °C
T - 7503 - - - EL	20-Pin, SOJ	–40 °C to +85 °C
T - 7503 - - 1EC	20-Pin, SOJ	0 °C to 70 °C
T - 7504 - - - PL	28-Pin, DIP	–40 °C to +85 °C
T - 7504 - - - ML	28-Pin, PLCC	–40 °C to +85 °C
T - 5504 - - - PL	28-Pin, DIP	–40 °C to +85 °C
T - 5504 - - - ML	28-Pin, PLCC	–40 °C to +85 °C
T - 7513B - - EE	20-Pin, SOJ	–40 °C to +85 °C
T - 7513B - - PE	20-Pin, DIP	–40 °C to +85 °C
T - 7517A - - EE	16-Pin, DIP	–40 °C to +85 °C
T - 7517A - - PE	16-Pin, SOJ	–40 °C to +85 °C
T - 7548 - - - ME2	28-Pin, PLCC	0 °C to 85 °C
T - 7570 - - - ML2	28-Pin, PLCC	–40 °C to +85 °C