Logic Design Solutions

M16550

Universal Asynchronous Receiver / Transmitter *MACRO*

Data Sheet

Aug. 99 – **Ver. 2**

Features

- Single-chip synchronous UART in a ORCA 2TA or 3T FPGA
- Functionally based on the National Semiconductor Corporation NS16550 device
- Designed to be included in high-speed and high-performance applications
- System clock up to 85 MHz
- CPU independent interface
- Complete asynchronous communication protocol including :
    - 5,6,7 or 8-bit data transmission
    - Even/Odd or no parity bit generation and detection
    - Start and Stop bit generation and detection
    - Line break generation and detection
    - Receiver Overrun and framing detection
    - Up to 1M baud (system frequency dependent)
- 1 to 65535 divisor generates 16X clock
- Buffered transmit and receive registers
- Transmitter and receiver are buffered with 16 Byte FIFO, plus 3 error bits per data byte on receiver
- Polled or interrupt mode
- Loopback mode

General Description

The macro M16550, based on an ORCA FPGA, implements a synchronous universal asynchronous receiver/transmitter, which provides an interface between a microprocessor and a serial communication channel.
This macro can be customized according to specific needs (microprocessor and application-specific requirement).
The arbiter and decoding logic can be integrated into the FPGA in addition to any other pre-designed functions.
FPGA density and I/O requirements can be defined according to customer specification.

Summary

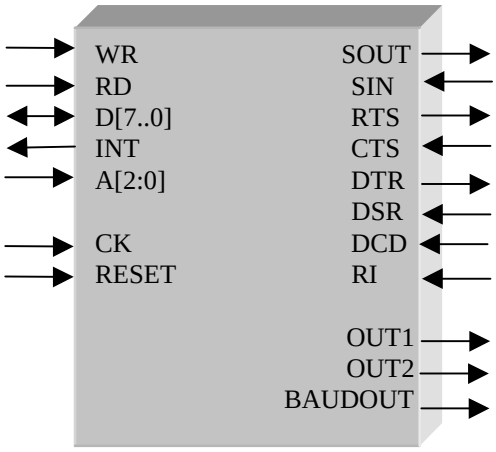
Device Family	2TA	3T
PFUs	127 *	61 *
I/O	27 **	27 **
System Clock	**-5** : up to 58 MHz **-6** : up to 75 MHz **-7** : up to 85 MHz	**-5** : up to 46 MHz **-6** : up to 58 MHz **-7** : up to 74 MHz
Documentation	**VHDL Source code** **VHDL Test Bench** for behavioral and gate level simulation. **Data Sheet** **Design Document :** features, architecture, interfaces and operation. **User's guide :** simulation, synthesis and Place and Route procedures.	
Constraint Files	« .prf » file	
Design Tool Requirement	VHDL synthesis Leonardo Spectrum from Exemplar. VHDL simulation tool. ORCA Foundry from Lucent.	
Support	Support provided by Logic Design Solutions: 90-day e-mail and telephone support included in the Macro price. Support does not cover user Macro modifications. Maintenance Contracts are also available.	

***** Can change according Software revision, Input flip-flop used on 3T Series.
****** Assuming all Macro signals are routed off-chip.

1. Description

1.1 Symbol

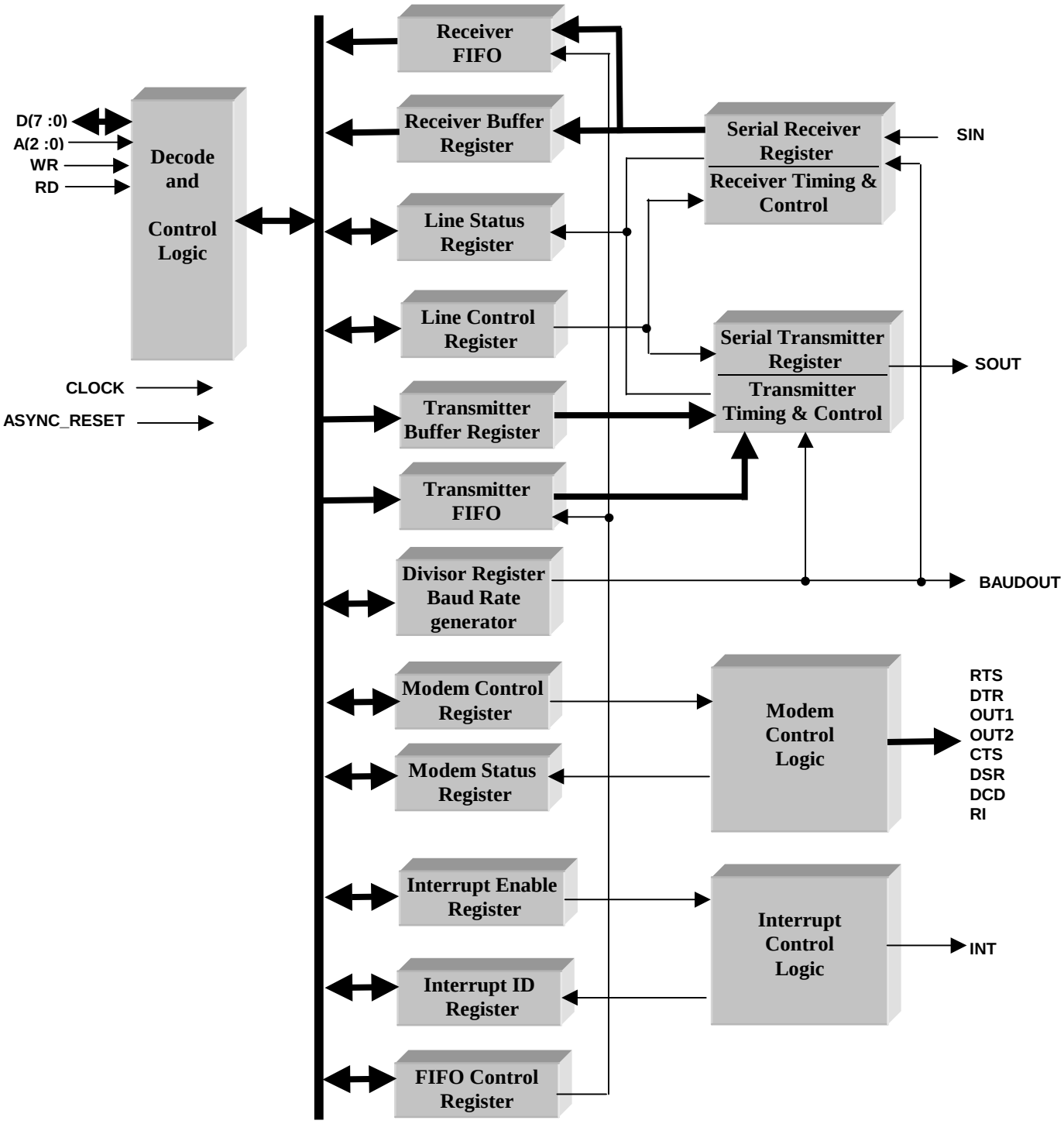
M16550 UART MACRO



1.2 Pin Description

Signal	Type	Activity	Description
CLOCK	Input	-	System clock. Rising edge triggered. Provides the master timing reference.
ASYNC_ RESET	Input	low	System asynchronous reset of the FPGA.
A(2 :0)	Input	-	Address signals to decode the internal registers.
D(7 :0)	I/O	-	Data bus.
RD	Input	high	A read cycle is active until RD is active.
WR	Input	high	The current data on the data bus is written in the internal register with a clock pulse of WR. See Cycle diagram.
INT	Output	high	Interrupt. Indicates that an enabled interrupt condition has been met.
SOUT	Output	low	Output of the Transmitter.
SIN	Input	low	Serial data input of the Receiver.
RTS	Output	low	Request To Send. The UART macro is ready to exchange data. This output is controlled by writing to bit 1 of the modem control register.
CTS	Input	low	Clear To Send. Indicates that the modem is ready to exchange data. A change in input is recorded in bit 0 of the modem status register. If the modem status interrupt is enabled, an interrupt is generated.
DTR	Output	low	Data Terminal Ready. The UART macro is ready to exchange data. This output is controlled by writing to bit 0 of the modem control register.
DSR	Input	low	Data Set Ready. Indicates that the modem is ready to establish the communications link with the UART macro. A change in input is recorded in bit 1 of the modem status register. If the modem status interrupt is enabled, an interrupt is generated.
DCD	Input	low	Data Carrier Detect. Indicates that the modem detected a data carrier. A change in input is recorded in bit 3 of the modem status register. If the modem status interrupt is enabled, an interrupt is generated.
RI	Output	low	Ring Indicator. Indicates that the modem detected the ring signal. A change in input is recorded in bit 2 of the modem status register. If the modem status interrupt is enabled, an interrupt is generated.
OUT1	Output	-	General purpose output 1. This output is controlled by writing to bit 2 of the modem control register.
OUT2	Output	-	General purpose output 2. This output is controlled by writing to bit 3 of the modem control register.

1.3 Functional Description



1.4 Register Address Map

The state of the A[2:0], WR and RD signals determines which internal register the microprocessor addresses.

DIV	WR	RD	A(2:0)	REGISTER
0	0	1	000	Receiver buffer register. (read only)
0	1	0	000	Transmitter buffer register. (write only)
1	1	0	000	Divisor register (LSB).
0	1	0	001	Interrupt enable register.
1	1	0	001	Divisor register (MSB).
x	0	1	010	Interrupt ID register.
x	1	0	010	FIFO control register.
x	1	0	011	Line control register.
x	1	0	100	MODEM control register.
x	0	1	101	Line status register.
x	0	1	110	MODEM status register.
x	x	x	111	Not used.

The DIV bit allows access to the divisor register. The DIV is bit 6 of the line control register.

1.5 Registers

1.5.1 Line Control Register

The line Control Register sets the data and communication formats used by the UART macro.

BIT	DESCRIPTION
1..0	Sets the length of the word associated with the transmitted or received word : 00 : 5 bits | 01 : 6 bits | 10 : 7 bits | 11 : 8 bits |
2	Controls the number of STOP bits generated by the transmitter section : 0 : 1 bit STOP 1 : 2 bit STOP *The receiver always checks only for the first bit STOP.*
3	Active high. Enable parity generation in the transmitter section and parity checking in the receiver section. The parity bit is inserted between the last word bit and the first STOP bit.
4	Parity Control. Generates/checks an odd/even number of logic one bits in data word + parity bit. 1 : Even parity. 0 : Odd parity.
5	Break Control. Active high. The macro UART generates a break condition, which is SOUT at low level for at least one full word transmission. The SOUT output is at 1 by default.
6	DIV. Active high. Enable access to the divisor register.
7	Not used.

1.5.2 Divisor register

The baud rate generator is composed of a programmable clock divider. The clock divider is made up of a 16-bit counter, loaded by the value of the divisor register.
The result of the division is the system clock divided by the register divisor value.
For example if the system clock is 50MHz, this latter is divided by the register divisor value, for example 325\d, we get 50MHz /(325) = 153,846 KHz, this is the BAUDOUT signal. Then to get the baud rate, this value has to be divided by 16, so 153,846 KHz / 16 = 9615,38 bits/s (9600 bits/s).
The Baudout signal is a positive pulse of one system clock period. The baudout signal is used by the recipient in order to sample 16 times the received bits. The recipient uses the baudout clock to create a middle clock, which is placed in the middle time of the received bits.

1.5.3 Line Status Register

The Line Status Register enables the host processor to examine data transfers.

BIT	SIGNAL	DESCRIPTION
0	RDR	Receiver Data Ready. Active high. Indicates that an incoming word has been received and transferred to the receiver buffer register. In FIFO mode, the Receiver FIFO has reached its trigger level. Generates a receive data available interrupt. This bit is cleared once it has been read.
1	OE	Overrun error. Active high. Indicates that new data has been written over unread data in the receiver buffer register. In FIFO mode, when the FIFO is full, indicates a new data has been received in the receiver shift register. The character in the the receiver shift register is overwritten and not written in the receiver FIFO. Generates a line status interrupt. This bit is cleared once it has been read.
2	PE	Parity error. Active high. Indicates that newly received data has incorrect parity. In FIFO mode, this error is registered with each character received. This error is revealed with the character at the top of the Receiver FIFO. Generates a line status interrupt. In FIFO mode, one line status interrupt is generated for each received character containing a parity error. This bit is cleared once it has been read.
3	FE	Framing error. Active high. Indicates that newly received data had incorrect stop bit. In FIFO mode, this error is registered with each character received. This error is revealed with the character at the top of the Receiver FIFO. Generates a line status interrupt. In FIFO mode, one line status interrupt is generated for each received character containing a framing error. This bit is cleared once it has been read.
4	BI	Break interrupt. Active high. Indicates that a break condition was detected on the serial input. A break condition occurs when the serial data in is held at logic low for longer than full word transmission. In FIFO mode, this error is registered with only the first break character received. When break occcurs, only one zero character is loaded into the Receiver FIFO. The next character is written in the Receiver FIFO on the next valid start detected. Generates a line status interrupt. This bit is cleared once it has been read.
5	TBRE	Transmitter buffer register empty. Active high. Indicates that the UART macro is ready to accept a new data word from the microprocessor for transmission. In the FIFO mode this bit is set to one when the Transmitter FIFO has reached its trigger level. Generates Transmitter buffer register empty interrupt. This bit is cleared once it has been read or by reading the interrupt ID register or by writing to the Transmitter buffer register or by writing to Transmitter FIFO to drop below the trigger level.
6	TRE	Transmitter empty. Active high. Indicates that the Transmitter buffer register and the serial transmitter register are both empty. In the FIFO mode, indicates the Transmitter FIFO and the serial transmitter register are both empty. This bit is cleared once it has been read.
7	F_ERR	FIFO contains error. Active high. In the 16450 mode this bit is at 0. In the FIFO mode this bit is set to one when there is at least one parity error, framing error or break indication in the FIFO. This bit is cleared once it has been read.

1.5.4 FIFO Control Register

The FIFO Control Register sets the FIFO mode used by the UART macro.

BIT	DESCRIPTION
0	Sets the FIFO mode. At one the FIFO counter logic is reset. The following bits are taken into account if bit 0 is set to one.
1	Active high. Reset the Receiver FIFO counter logic. The Receiver shift register is not cleared. Once take into account this bit is automatically cleared.
2	Active high. Reset the Transmitter FIFO counter logic. The Transmitter shift register is not cleared. Once take into account this bit is automatically cleared.
3	Not used.
4..5	Sets the trigger level for the Transmitter FIFO: 00 : 1 byte | 01 : 4 bytes | 10 : 8 bytes | 11 : 12 bytes | When the trigger level has been reached, it remains 1, 4, 8 or 12 bytes to transmit in the Transmitter FIFO.
6..7	Sets the trigger level for the Receiver FIFO: 00 : 1 byte | 01 : 4 bytes | 10 : 8 bytes | 11 : 12 bytes | When the trigger level has been reached, there is 1, 4, 8 or 12 bytes in the Receiver FIFO.

1.5.5 Interrupt Identification Register

This register enables the microprocessor to identify the interrupt coming from the macro UART.

BIT	0	1	2	3
Interrupt Type	Receiver Status	Receiver buffer register full	Transmitter buffer register empty	MODEM Status
Interrupt Source	Overrun, Parity, Frame error, break interrupt.	Receiver data available Or Receiver FIFO has Reached its trigger level	Transmitter buffer register empty Or Transmitter FIFO has Reached its trigger level	CTS, DSR, RI or DCD change state.
Interrupt Reset	Read the Line status register.	Read the Receiver buffer register Or Read the Receiver FIFO to drop below the trigger level.	Read the interrupt ID register Or Write to Transmitter buffer register Or Write to Transmitter FIFO to drop below the trigger level.	Read the MODEM status register.

BIT	4	5	6	7
DESCRIPTION	Not used.	Not used.	At one when in FIFO mode. (FIFO Control Register Bit 0 at one)	At one when in FIFO mode. (FIFO Control Register Bit 0 at one)

1.5.6 Interrupt Enable Register

The interrupt enable register selectively enables or disable four different sources of interruption. When a bit is at 0, the interrupt is not enabled.

Bit	Signal	Description
0	RDA	Received data available. Enables interrupts when receive data is loaded in the receiver buffer register or when the Receiver FIFO has reached its trigger level.
1	THRE	Transmitter buffer register empty. Enables interrupts when the Transmitter buffer register is empty or when the Transmitter FIFO has reached its trigger level.
2	RLS	Receiver line status. Enables interrupts when the Receiver line status register changes state.
3	MS	Modem status. Enables interrupts when the Modem status register changes state.
7 :4	-	Not used.

1.5.7 MODEM Control Register

The MODEM Control Register controls the modem interface outputs.

BIT	SIGNAL	DESCRIPTION
0	DTR	Data Terminal Ready. The user can program the DTR bit to control the DTR output.
1	RTS	Request To Send. The user can program the RTS bit to control the RTS output.
2	OUT1	Output 1. The user can program the OUT1 bit to control the OUT1 output.
3	OUT2	Output 2. The user can program the OUT2 bit to control the OUT2 output.
4	LOOP	Enable loopback. Active high. Connection are as follows : - The SOUT output is set to high. - The SIN input is ignored. - The internal SOUT is connected to the internal SIN. - The MODEM control inputs are ignored. - The MODEM control outputs are used internally in place of the modem control inputs. The connections are as follows : DTR => DSR RTS => CTS OUT1 => RI OUT2 => DCD
2..7	Not used.	

1.5.8 MODEM status register

The MODEM status register enables the microprocessor to examine the condition of the modem interface inputs.

BIT	SIGNAL	DESCRIPTION
0	FCTS	Front clear to send. Active high. Indicates that the CTS input has changed since the processor read the modem status register. Generates a modem status interrupt. This bit is cleared once it has been read.
1	FDSR	Front data set ready. Active high. Indicates that the DSR input has changed since the processor read the modem status register. Generates a modem status interrupt. This bit is cleared once it has been read.
2	FRI	Front ring indicator. Active high. Indicates that the RI input has changed from 0 to 1 since the processor read the modem status register. Generates a modem status interrupt. This bit is cleared once it has been read.
3	FDCD	Front data carrier. Active high. Indicates that the DCD input has changed since the processor read the modem status register. Generates a modem status interrupt. This bit is cleared once it has been read.
4	CTS	Clear To Send. This bit is the state of the pin CTS.
5	DSR	Data Set Ready. This bit is the state of the pin DSR.
6	RI	Ring Indicator. This bit is the state of the pin RI.
7	DCD	Data Carrier Detect. This bit is the state of the pin DCD.

1.5.9 Receiver buffer register

The receiver buffer register is a read only register that contains the last complete data word sample received by the UART. The microprocessor is advised by an interrupt signal.

1.5.10 Transmitter buffer register

The transmitter buffer register is a write only register that loads the next data byte to be transmitted by the UART. The microprocessor is advised by an interrupt signal that this register is empty.

1.5.11 Transmitter FIFO

The transmitter FIFO is only active in FIFO mode. In FIFO mode, as soon as there is a data in the FIFO, this one is sent to the transmission logic. The FIFO is protected against overwritting from the user, it means when the FIFO is full, the next data coming from the user will not be written in the FIFO.
When the read pointer reaches his transmission trigger level the microprocessor is advised by an interrupt.

1.5.12 Receiver FIFO

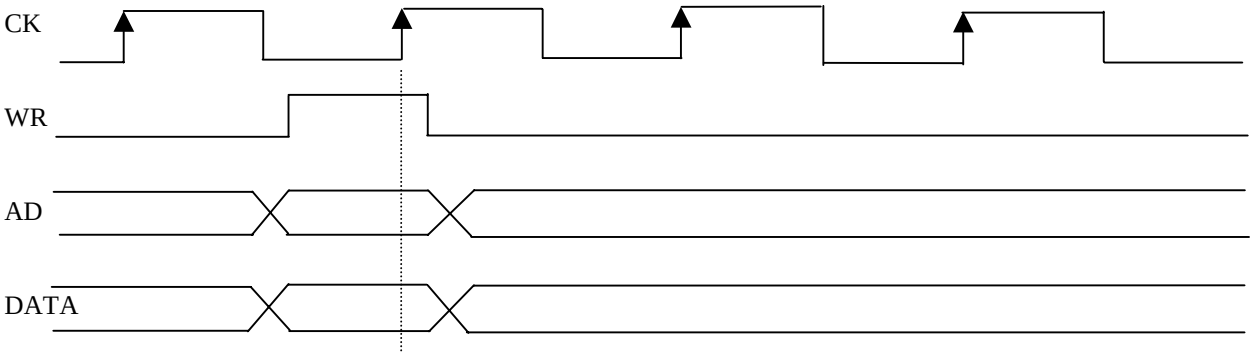
The receiver FIFO is only active in FIFO mode. In FIFO mode, as soon as the writting pointer reaches his reception trigger level the microprocessor is advised by an interrupt signal. The FIFO is protected against overwritting from the reception side, it means when the FIFO is full the next data received is not written in the FIFO.
The reception FIFO is also protected against overreading from the user side, it means if the FIFO is empty the read pointer is not incremented.

1.6 Write cycle

The write cycle is made up of a positive pulse of the WR signal sampling by the system clock.

The WR signal enables the decoding of the 3 address signals A(2 :0). The data should be present at the same time.

The following chronogram describes the write cycle :



The Setup and hold timings are implementation-dependent.

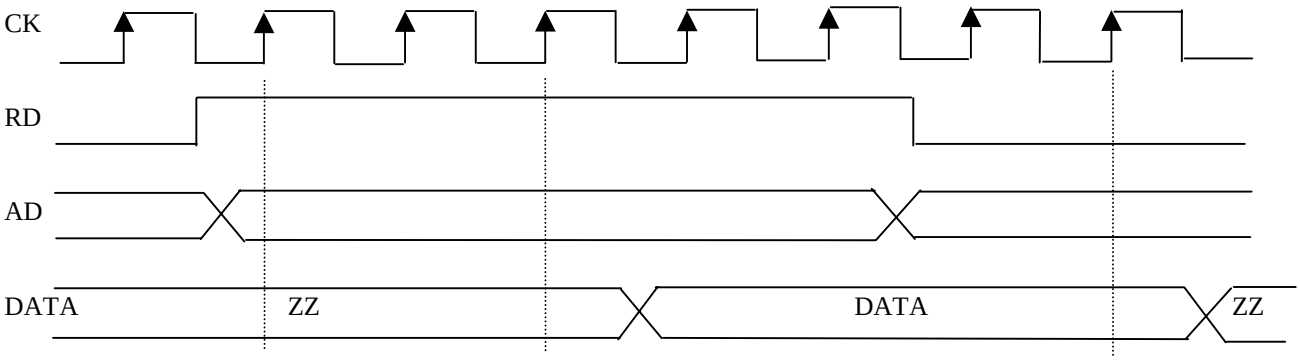
If the macro is used alone in the FPGA, the timing will be equal to that of the FPGA I/O. Please refer to the appropriate FPGA data sheet.

If the macro is used in a design, these timings will be controlled by the Place and Route software because of the synchronous conception.

1.7 Read cycle

The read cycle is initialized as soon as and while the RD signal is at level 1. This signal should be synchronous to the system clock.

The following chronogram describes the write cycle :



The Setup and hold timings are implementation-dependent.

If the macro is used alone in the FPGA, the timing will be equal to that of the FPGA I/O. Please refer to the appropriate FPGA data sheet.

If the macro is used in a design, because of the synchronous conception, these timings will be controlled by the Place and Route software.

2. Specificity and Recall

At the reception side, if the user configures less than 8 bits for the data, the user should mask the high bits in proportion when reading the Receiver Buffer Register. For instance, if the data is composed of 5 bits, the user should mask or not pay attention to the 3 high bits (7,6 and 5) when reading the Receiver Buffer Register.

The configuration of the UART is the same as for the transmitter and the receiver.
The 0000\h value should not be used for the divisor register.
There is no encoding priority on interruption.
The DIVisor bit is placed in bit 6 and not in 7.
There is no scratchpad register.
The following registers are not readable : transmitter buffer register, divisor register, interrupt enable register, line control register and modem control register.

3. Tool version used

The Macro has been done with a PC on Windows N.T. 4 and with the following tools :

- Synthesis tool : Leonardo Spectrum level 2 V1998.2e from Exemplar.
- Place and Route tool : Orca Foundry V9.35(Patch A) from Lucent technologies.
- VHDL Simulation tool : ModelSim EE V5.2e from ModelTech

Every tool has been used through its GUI.

4. Recommended Design Experience

Designers should be familiar with asynchronous communication controllers, VHDL, synthesis tools, ORCA Foundry data flow and VHDL simulation software. Experience with microprocessor is recommended. The macro can easily be integrated into hierarchical VHDL designs.

5. Available Support Products

Support products available from Logic Design Solutions.

6. Ordering Information

To purchase or make further inquiries about this, or any other Logic Design Solutions products and services, contact Logic Design Solutions in France.
Logic Design Solutions also offers macro integration and design services on FPGA technologies.
Logic Design Solutions macros are purchased under a License Agreement, copies of which are available on request.
Logic Design Solutions reserves the right to make changes to these specifications at any time, without notice.

7. Related Information

Lucent Programmable Logic

For information on Lucent programmable logic or development system software, please contact your local Lucent sales office.
WEB: http://www.lucent.com/orca

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