LINEAR INTEGRATED CIRCUITS

MC1458
MC1458C

7929225 S G S SEMICONDUCTOR CORP

PRELIMINARY DATA

DUAL OPERATIONAL AMPLIFIERS

- INTERNALLY COMPENSATED
- SHORT-CIRCUIT PROTECTED
- LOW POWER CONSUMPTION
- WIDE COMMON-MODE AND DIFFERENTIAL VOLTAGE RANGES
- NO LATCH-UP

The MC 1458 is a dual operational amplifier with frequency and phase compensation built into the chip, available in 8-lead minidip package and in 8-lead micropackage. It is intended for a wide range of applications where space and cost saving are the main goals. In spite of that, the MC 1458 offers good performance and absence of latch-up makes the device ideal for use as voltage follower, integrator, summing amplifier and general feedback applications.

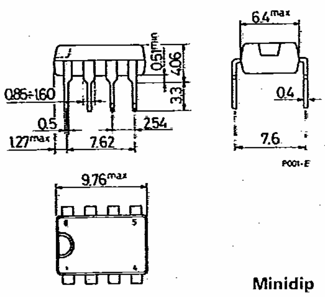
ABSOLUTE MAXIMUM RATINGS

V_s	Supply voltage		± 18	V
V_i	Input voltage (*)		± 15	V
V_i	Differential input voltage		± 30	V
P_{tot}	Power dissipation at T_{amb} = 70°C	Minidip	665	mW
		Micropackage	400	mW
T_{op}	Operating temperature		0 to 70	°C
T_{stg}	Storage temperature		-55 to 150	°C

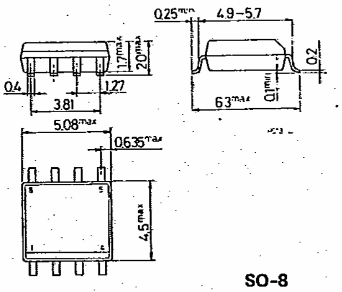
(*) For V_s lower than ± 15V, the absolute maximum input voltage is equal to the supply voltage.

MECHANICAL DATA

Dimensions in mm

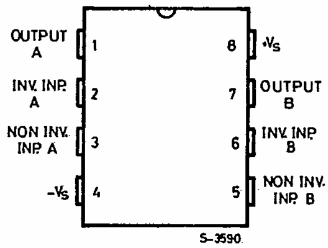


Minidip



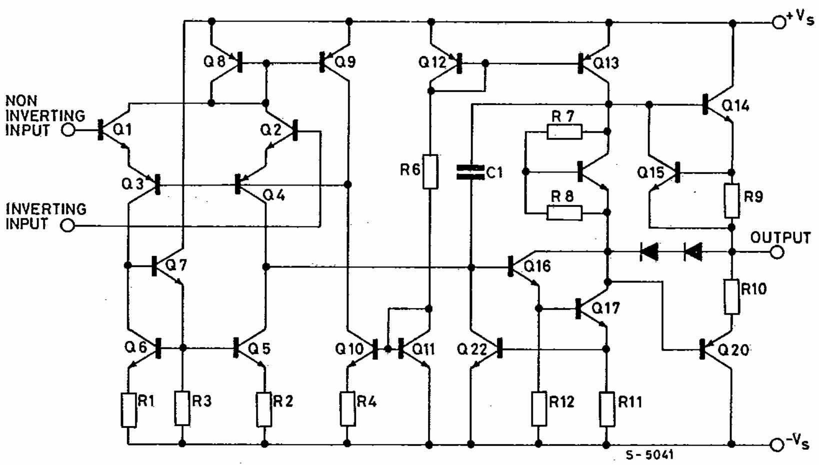
SO-8

CONNECTION DIAGRAM AND ORDERING NUMBERS
(top view)



Type	Minidip	SO-8
MC 1458	MC 1458 P1	MC 1458 M
MC 1458C	MC 1458 CP1	MC 1458 CM

SCHEMATIC DIAGRAM (one section)



THERMAL DATA

			Minidip	SO-8
$R_{th\ j\text{-}amb}$	Thermal resistance junction-ambient	max	120 °C/W	200* °C/W

* Measured with the device mounted on a ceramic substrate (25 x 16 x 0.6 mm.).

ELECTRICAL CHARACTERISTICS (V_s= ± 15V, T_{amb}= 25°C, unless otherwise specified)

Parameter		Test conditions		MC 1458			MC 1458C			Unit
				Min.	Typ.	Max.	Min.	Typ.	Max.	
I_s	Supply current (both amplifiers)					5.6			8	mA
I_b	Input bias current					0.5			0.7	μA
		$0°C < T_{op} < 70°C$				0.8			1	μA
V_{os}	Input offset voltage	$R_g \leq 10\ K\Omega$			2	6		2	10	mV
		$R_g \leq 10\ K\Omega$ $0°C < T_{op} < 70°C$				7.5			12	mV
$\frac{\Delta V_{os}}{\Delta T}$	Input offset voltage drift	$R_g = 10\ K\Omega$ $0°C < T_{op} < 70°C$			6			6		μV/°C
I_{os}	Input offset current				20	200		20	300	nA
		$0°C < T_{op} < 70°C$				300			400	nA
$\frac{\Delta I_{os}}{\Delta T}$	Input offset current drift	$0°C < T_{op} < 70°C$			0.5			0.5		nA/°C
I_{sc}	Output short circuit current				20			20		mA
G_v	Large signal open loop voltage gain	$R_L = 2K\Omega$	T_{amb}= 0 to 70°C	83						dB
		$R_L = 2K\Omega$		86	106					dB
		$R_L = 10K\Omega$	T_{amb}= 0 to 70°C				83			dB
		$R_L = 10K\Omega$					86	106		dB
B	Unity gain bandwidth				0.8			0.8		MHz
e_N	Input noise voltage	B= 10Hz to 10 KHz	R_g= 1 KΩ		3			3		μV
		B= 10Hz to 10 KHz	R_g= 500 KΩ		25			25		μV
V_o	Output voltage swing	R_L= 2 KΩ		± 10	± 13		± 9	± 13		V
		R_L= 10 KΩ		± 12	± 14		± 11	± 14		V
SR	Slew Rate			0.3			0.3			V/μs
CMR	Common mode rejection			70	90		60	90		dB
SVR	Supply voltage rejection			76	90			90		dB
	Common mode input voltage range			± 12	± 13		± 11	± 13		V