T-52-15

GigaBit Logic

10G014
ADVANCE

High Speed DRAM and SRAM Driver/Translator 100MHZ Clock - 5 ns Delay Time

10G PicoLogic™ Family

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FEATURES

- 90 mA output capability for driving large memory array terminated in 25Ω
- Built-in clocked addresses & controls provide pipelining with no external components
- Differential outputs minimize transient current
- 2:1 multiplexed Row & Column addresses
- Three devices address 16M word bank of memory with provision for additional expansion.
- Guaranteed 100 MHz clock rate
- VCC=+5V and VEE= -5.2 V power supplies
- Temperature and voltage compensated using VBB threshold reference input providing compatibility with 10K and 100K ECL families.
- Increases system memory speed or decreases RAM cost
- Available in 40 pin leaded or leadless chip carrier, 44-pin PLCC or die form

APPLICATIONS

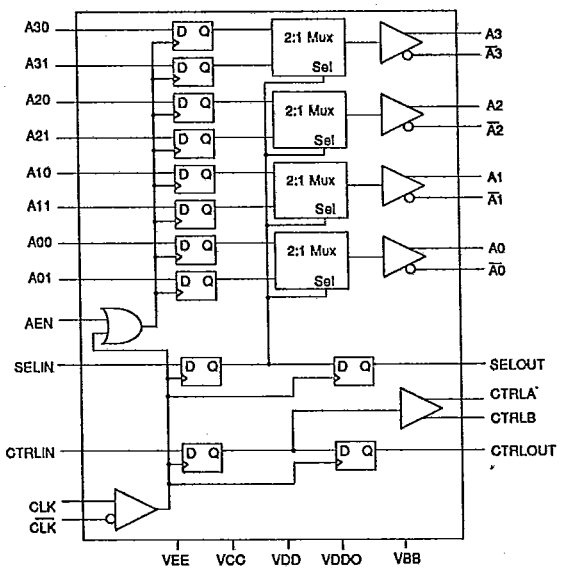
- DRAM address and control driver
- Dual source SRAM address driver
- High speed quad registered ECL to TTL multiplexer
- ECL to TTL level translator

FUNCTIONAL DESCRIPTION

The 10G014 is a high speed interface IC designed specifically to drive the large distributed capacitive loads of large memory arrays. Eight ECL address inputs are latched by a rising edge clock. Row addresses (An,.) or Column addresses (A.,m) are selelected under control of a registered Select input signal (SELIN). The four differential address outputs of the 10G014 are TTL compatible, open drain and designed to be terminated in resistors as low as 25Ω to a positive supply. Complementary outputs minimize transient currents while doubling fanout. CTRLIN and SELIN inputs (ECL levels) are register delayed by two clock cycles and appear as SELOUT and CTRLOUT ECL outputs. SELOUT and CTRLOUT are used as inputs to other 10G014's for supporting additional memory banks pipeline delayed by two clock cycles. This operation permits up to 7.5ns of external delay between 10G014's in different banks when clocking at 100 MHz.

During a read or write cycle, AEN (Address Enable) is at an ECL logic low state to capture the input addresses. SELIN should be low to select the Row addresses (An,.) and should be brought high to direct the Column addresses (A.,m) to the outputs.

BLOCK DIAGRAM



10G014 ORDERING INFORMATION

PACKAGE TYPE	Clock Frequency 100MHz
40-pin C-Leaded CC	10G014-2C
40-pin Leadless CC	10G014-2L
44-pin PLCC	10G014-2P2
Die	10G014-2X

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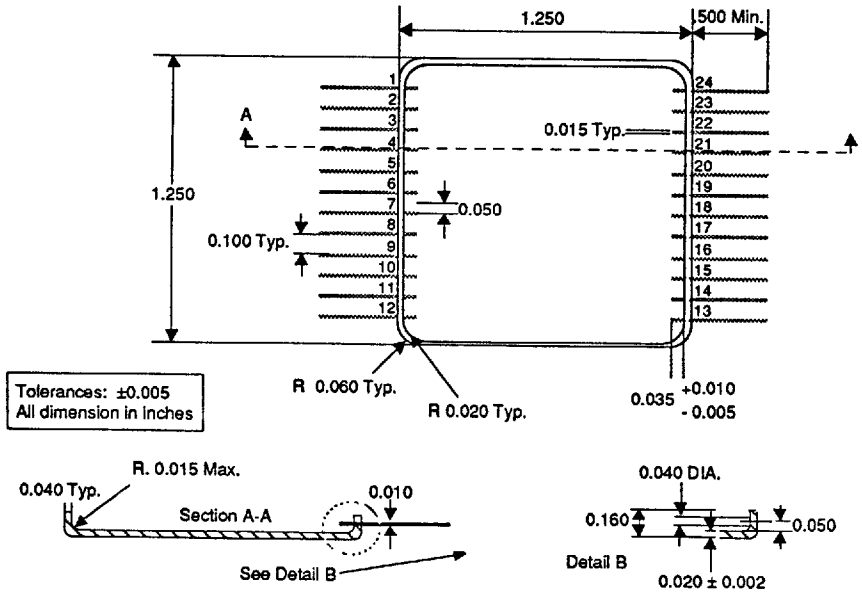
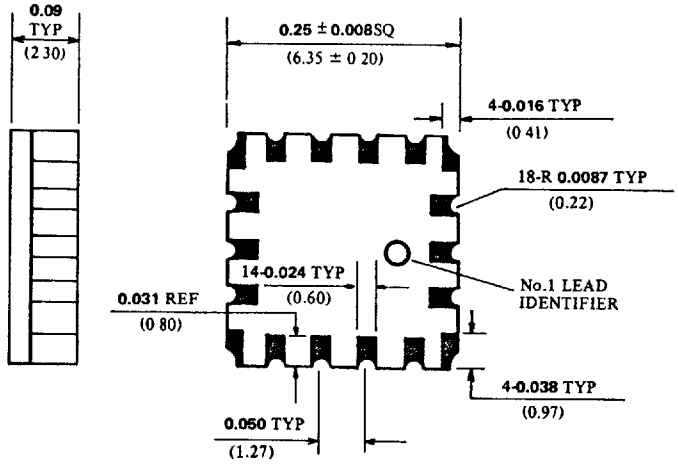
24 PIN METAL FLATPACK
18 PIN PACKAGE

24 PIN METAL FLATPACK
Type H



18 PIN LEADLESS CHIP CARRIER
TYPE L1



All dimensions shown in inches and (millimeters)

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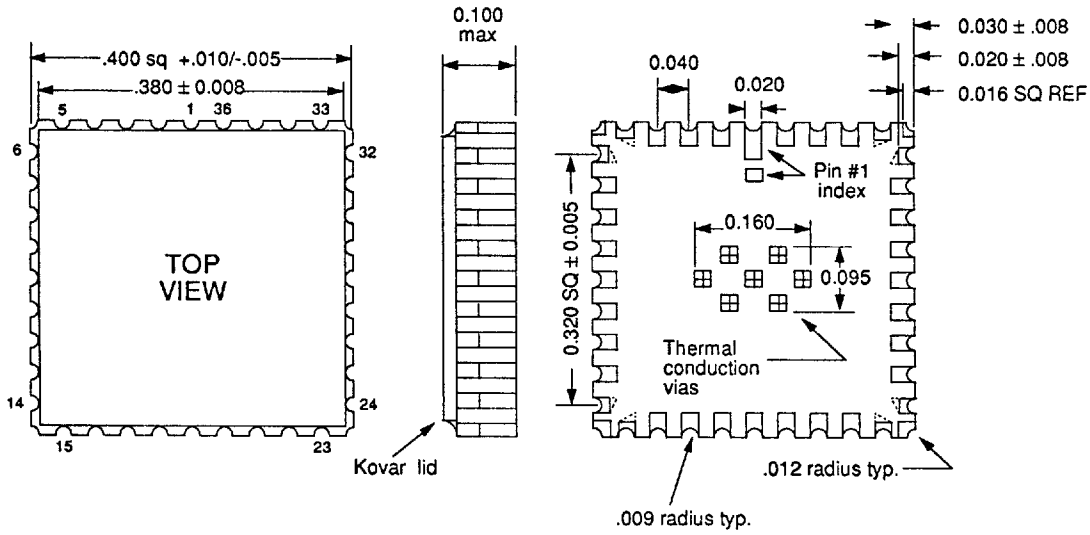
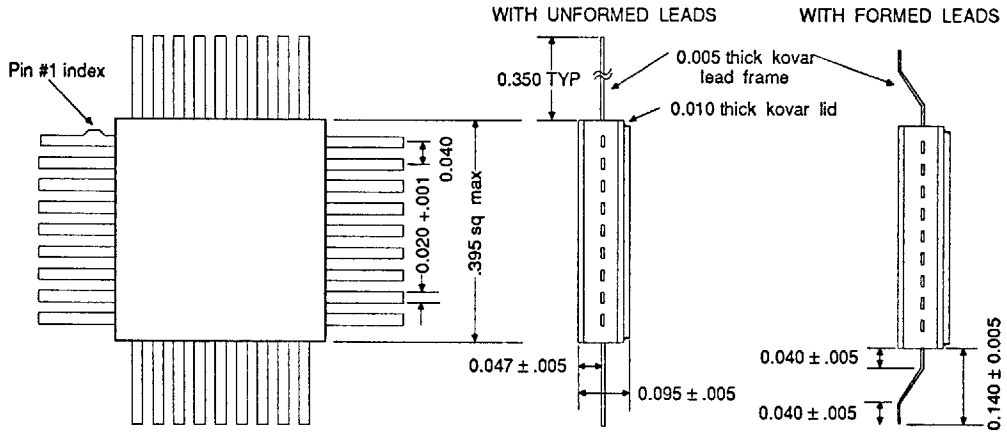
36 PIN PACKAGES

36 PIN LEADLESS CHIP CARRIER
TYPE L36



NOTES:
1) The package bottom thermal vias, top lid surface and 4 metallized corner castellations (when present) are all at Vss potential.
2) All dimensions in inches.
3) Plin #1 identifier may be an elongated pad or small, square gray marker.

36 I/O LEAD FLATPACK
TYPE F



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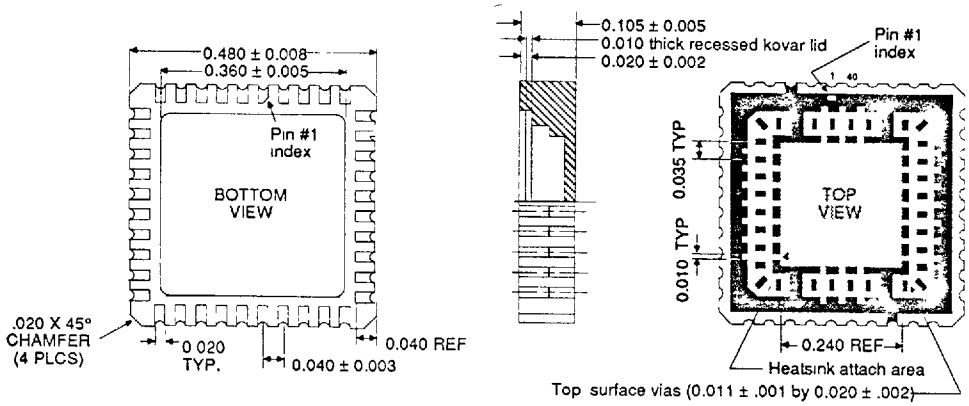
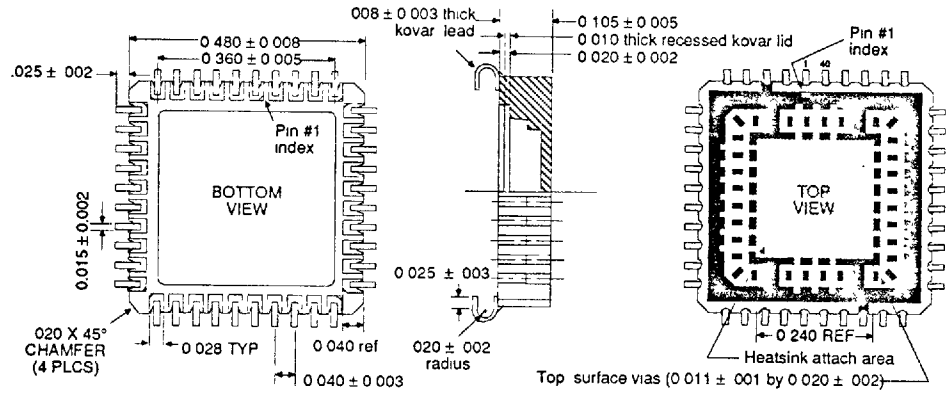
40 PIN PACKAGES

40 PIN LEADLESS CHIP CARRIER
TYPE L

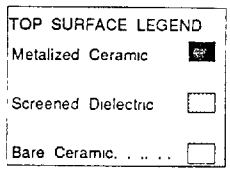


40 PIN LEADED CHIP CARRIER
TYPE C

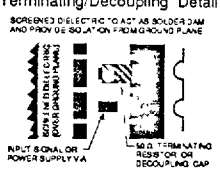


NOTES

(1) Footprint is JEDEC standard outline
(2) Top surface v as (for terminating resistors and decoupling capacitors) are not available on pins 3 4 17 18 23 24 37 and 38
(3) Top surface metal (not including vias) and p ns 3 and 23 are fixed at VTT potential
(4) Recommended top surface chip res stors are 0 040 long by 0 020 w de by 0 010 thick typ 100 mw min nominal power rating (M ni-Systems MSR 21 or equivalent)
(5) Recommended top surface ch p capac tors are 0 040 ong by 0 030 wide by 0 020 thick typ 25V VDCW 1000 pf min (Johanson R09 case or equivalent)
(6) Recommended heatsinks a e GBL P/Ns 90GHS 40 A and 90GHS 40 B
(7) Thermally conductive, e ectrically non-conductive epoxy is recommended for heatsink attachment (Ablestick 789 4 or 561K, or Thermalloy Thermalbond™ or equivalent.)
(8) L40 and C40 packages are dimensionally identical except for contact finger width



Top Surface Terminating/Decoupling Detail



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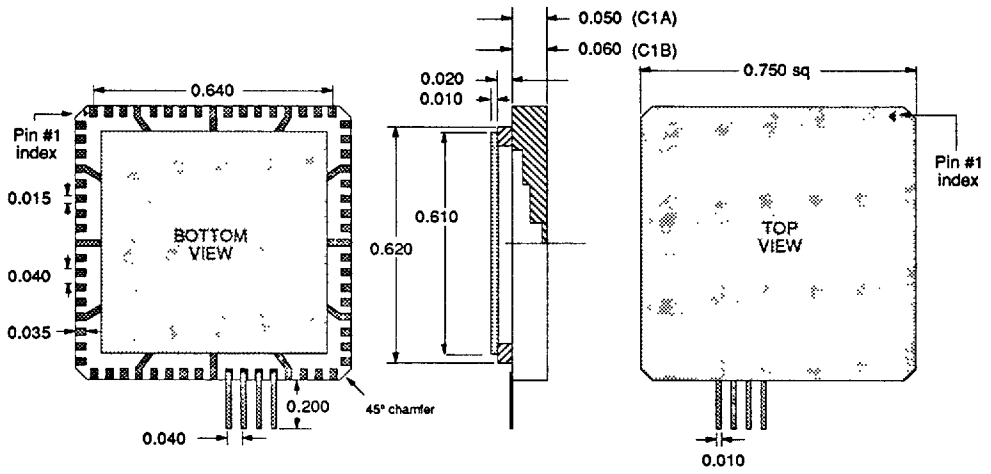
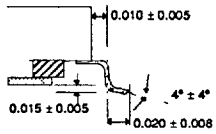
68 & 132 PIN PACKAGES

68 PIN LEADED CHIP CARRIER
TYPE C1



1. All dimensions in inches.
2. C1A PACKAGE: Package lid, top, and pins 4, 9, 14, 21, 26, 31, 38, 43, 48, 55, 60, 65 are at common potential (system ground).
3. C1B PACKAGE: Package lid and pins 4, 9, 14, 21, 26, 31, 38, 43, 48, 55, 60, 65 are at common potential (system ground).
4. Tolerance on all dimensions is ± 1 % but not larger than ± 0.005. Tolerance on 0.640 end pad to end pad dimension is ± 0.003.

GULLWING LEADS



132 PIN LEADED CHIP CARRIER
TYPE C3