MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

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# Military 8S512

*Advance Information*

# 512K x 8 CMOS SRAM Multichip Module

The Motorola 8S512 is a CMOS SRAM housed in a hermetically sealed ceramic 32 pin package. Featuring JEDEC standard pinouts, the device provides 512K bytes of read/write low power memory. The device is well suited for battery backed operations and will retain data at voltages as low as 2.0 volts.

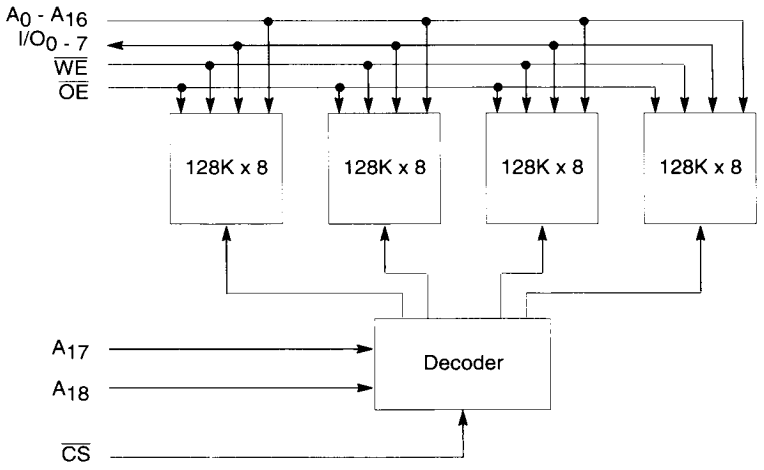
Designed for use in demanding applications, the memory packaging and construction is well suited for military and severe industrial applications. The rugged ceramic package features a welded metal cover and co-fired construction to assure maximum integrity and hermetic seal. The module also features internal power supply bypass capacitors to enhance performance.

Inputs and outputs are TTL compatible. The logic levels and drive capabilities permit the memory to interface with most digital logic systems. Since the device is all CMOS, low power operations for standby applications such as battery backed systems is straightforward.

**FEATURES:**

- Access Times 25 to 120 ns
- JEDEC Standard 32 pin DIP, Hermetic Ceramic Package
- Military Temperature Range (- 55°C to + 125°C)
- MIL-STD-883 Compliant Devices (Planned)
- DESC Standard Military Drawing (Planned)
- Military Screening and Burn-In Available
- Commercial Plus Processing Available
- All CMOS Fully Static Design, No Clock
- 5 Volt Operation
- TTL Compatible Inputs and Outputs
- Battery Back-Up Operation

**BLOCK DIAGRAM**

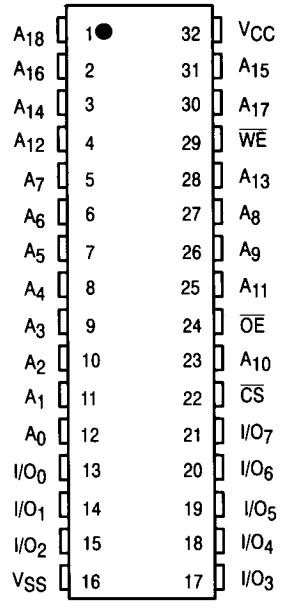



**SRAM MULTICHIP MODULE**

**AVAILABLE AS**
**1) JAN: N/A**
**2) SMD: Planned**
**3) 883: 8S512-XX/BXCJC**
**4) CMP: 8S512-XX/ ***
*** See Commercial Plus and Avionics Options: (BR914/D)**
**PACKAGE: DIL: X**

**XX = Speed in ns (25 to 120)**

**PIN ASSIGNMENT**




**PIN NAMES**

| | |
|---|---|
| $A_0$ - $A_{18}$ | Address Inputs |
| $I/O_0$ - $I/O_7$ | Data Input/Output |
| $\overline{CS}$ | Chip Select |
| $\overline{OE}$ | Output Enable |
| $\overline{WE}$ | Write Enable |
| $V_{CC}$ | + 5.0 Power |
| $V_{SS}$ | Ground |

This document contains information on a new product. Specifications and information herein are subject to change without notice.

MOTOROLA

| ABSOLUTE MAXIMUM RATINGS | | | |
|---|---|---|---|
| **Parameter** | **Symbol** | **Value** | **Unit** |
| Operating Temperature | $T_A$ | - 55 to + 125 | °C |
| Storage Temperature Range | $T_{STG}$ | - 65 to + 150 | °C |
| Supply Voltage | $V_{CC}$ | - 0.5 to + 7.0 | V |
| Supply Voltage (Any Pin) | $V_G$ | - 0.5 to + 7.0 | V |

| TRUTH TABLE | | | | | | |
|---|---|---|---|---|---|---|
| $\overline{CS}$ | $\overline{OE}$ | $\overline{WE}$ | $A_0$-$A_{18}$ | **Mode** | **Data I/O** | **Device Current** |
| H | X | X | X | Standby | High-Z | Standby |
| L | L | H | Stable | Read | Data Out | Active |
| L | X | L | Stable | Write | Data In | Active |
| L | H | H | Stable | Out Disable | High-Z | Active |

| RECOMMENDED OPERATING CONDITIONS | | | | |
|---|---|---|---|---|
| **Parameter** | **Symbol** | **Min** | **Max** | **Unit** |
| Supply Voltage | $V_{CC}$ | 4.5 | 5.5 | V |
| Input High Voltage | $V_{IH}$ | 2.2 | $V_{CC}$ + 0.3 | V |
| Input Low Voltage | * $V_{IL}$ | - 0.5 | + 0.8 | V |
| Operating Temp. (Mil.) | $T_A$ | - 55 | + 125 | °C |

* $V_{IL}$(min) = 3.0 V for pulse width less than 20 ns.

| CAPACITANCE (@ $T_A$ = 25°C) | | | | |
|---|---|---|---|---|
| **Parameter** | **Symbol** | **Condition** | **Max** | **Unit** |
| * Input Capacitance | $C_{IN}$ | $V_{IN}$ = 0 V, f = 1.0 MHz | 40 | pF |
| * Output Capacitance | $C_{OUT}$ | $V_{OUT}$ = 0 V, f = 1.0 MHz | 40 | pF |

* Periodically sampled rather than 100% tested.

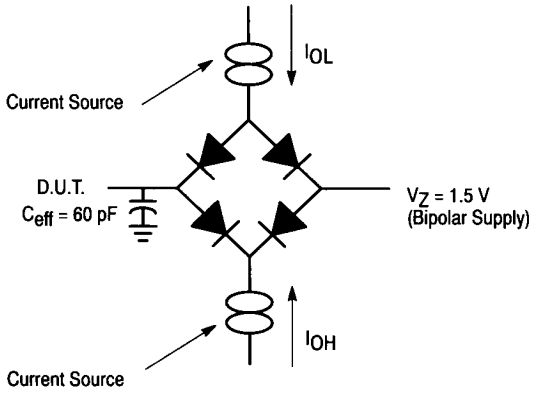
## DC CHARACTERISTICS

($V_{CC}$ = 5 V ± 10%, $V_{SS}$ = 0 V, $T_A$ = - 55°C to + 125°C)

| **Parameter** | **Symbol** | **Limits** | | | | | | | | **Unit** | **Test Condition (Unless Otherwise Specified)** |
|---|---|---|---|---|---|---|---|---|---|---|---|
| **Functional Parameters:** | | **- 25** | | **- 35** | | **- 45** | | **- 55** | | | |
| | | **Min** | **Max** | **Min** | **Max** | **Min** | **Max** | **Min** | **Max** | | |
| Input Leakage Current | $I_{LI}$ | | 15 | | 15 | | 15 | | 15 | µA | $V_{CC}$ = Max, $V_{IN}$ = Gnd or $V_{CC}$ |
| Output Leakage Current | $I_{LO}$ | | 15 | | 15 | | 15 | | 15 | µA | $\overline{CS}$ = $V_{IH}$, $\overline{OE}$ = $V_{IH}$, $V_{OUT}$ = Gnd or $V_{CC}$ |
| Dynamic Supply Current | $I_{CC}$ | | 150 | | 150 | | 150 | | 130 | mA | $\overline{CS}$ = $V_{IL}$, $\overline{OE}$ = $V_{IH}$, Duty Cycle = Max |
| Standby Current | $I_{SB}$ | | 60 | | 60 | | 55 | | 50 | mA | $\overline{CS}$ = $V_{CC}$, $\overline{OE}$ = $V_{IH}$, Duty Cycle = Max |
| Output Low Voltage | $V_{OL}$ | | 0.4 | | 0.4 | | | | | V | $I_{OL}$ = 8 mA, $V_{CC}$ = Min |
| | | | | | | | 0.4 | | 0.4 | V | $I_{OL}$ = 2.1 mA, $V_{CC}$ = Min |
| Output High Voltage | $V_{OH}$ | 2.4 | | 2.4 | | | | | | V | $I_{OH}$ = - 4.0 mA, $V_{CC}$ = Min |
| | | | | | | 2.4 | | 2.4 | | V | $I_{OH}$ = - 1.0 mA, $V_{CC}$ = Min |

| **Parameter** | **Symbol** | **Limits** | | | | | | | | **Unit** | **Test Condition (Unless Otherwise Specified)** |
|---|---|---|---|---|---|---|---|---|---|---|---|
| **Functional Parameters:** | | **- 70** | | **- 85** | | **- 100** | | **- 120** | | | |
| | | **Min** | **Max** | **Min** | **Max** | **Min** | **Max** | **Min** | **Max** | | |
| Input Leakage Current | $I_{LI}$ | | 15 | | 15 | | 15 | | 15 | µA | $V_{CC}$ = Max, $V_{IN}$ = Gnd or $V_{CC}$ |
| Output Leakage Current | $I_{LO}$ | | 15 | | 15 | | 15 | | 15 | µA | $\overline{CS}$ = $V_{IH}$, $\overline{OE}$ = $V_{IH}$, $V_{OUT}$ = Gnd or $V_{CC}$ |
| Dynamic Supply Current | $I_{CC}$ | | 120 | | 80 | | 70 | | 70 | mA | $\overline{CS}$ = $V_{IL}$, $\overline{OE}$ = $V_{IH}$, Duty Cycle = Max |
| Standby Current | $I_{SB}$ | | 45 | | 4 | | 2.5 | | 2.5 | mA | $\overline{CS}$ = $V_{CC}$, $\overline{OE}$ = $V_{IH}$, Duty Cycle = Max |
| Output Low Voltage | $V_{OL}$ | | 0.4 | | 0.4 | | 0.4 | | 0.4 | V | $I_{OL}$ = 2.1 mA |
| Output High Voltage | $V_{OH}$ | 2.4 | | 2.4 | | 2.4 | | 2.4 | | V | $I_{OH}$ = - 1.0 mA |

## AC TEST CIRCUIT




## AC TEST CONDITIONS

| Parameters | Typical | Unit |
|---|---|---|
| Input Pulse Levels | $V_{IL}$ = 0, $V_{IH}$ = 3.0 | V |
| Input Rise and Fall | 5 | ns |
| Input/Output Reference Level | 1.5 | V |
| Output Timing Reference Level | 1.5 | V |

Notes:
$V_Z$ is programmable from - 2 V to + 7 V
$I_{OL}$ & $I_{OH}$ programmable from 0 to 16 mA
Tester Impedance Z0 = 75Ω
$V_Z$ is typically the midpoint of $V_{OH}$ and $V_{OL}$
(i.e. (2.4 + 0.4)/2 = 1.4 V)
$I_{OL}$ & $I_{OH}$ are adjusted to simulate a typical resistive load circuit
ATE Tester Includes Jig Capacitance

## AC CHARACTERISTICS

($V_{CC}$ = 5 V ± 10%, $V_{SS}$ = 0 V, $T_A$ = - 55°C to + 125°C)

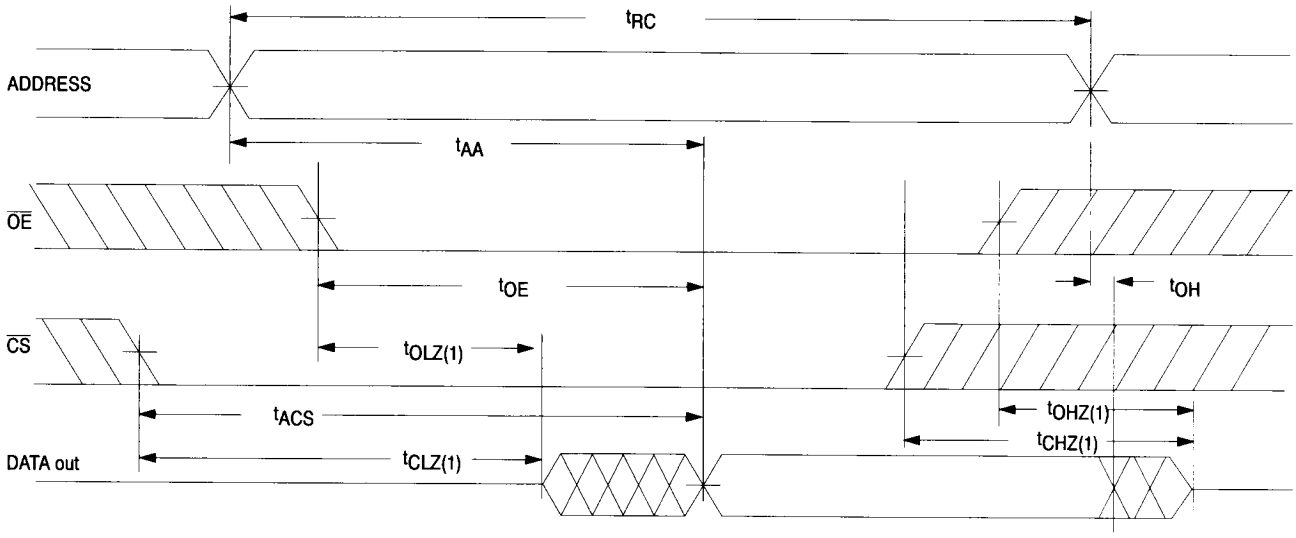
| Parameter | Symbol | Limits | | | | | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| **Read Cycle:** | | - 25 | | - 35 | | - 45 | | - 55 | | |
| | | Min | Max | Min | Max | Min | Max | Min | Max | |
| Read Cycle Time | $t_{RC}$ | 25 | | 35 | | 45 | | 55 | | ns |
| Address Access Time | $t_{AA}$ | | 25 | | 35 | | 45 | | 55 | ns |
| Output Hold from Address Change | $t_{OH}$ | 5 | | 5 | | 5 | | 5 | | ns |
| $\overline{CS}$ Access Time | $t_{ACS}$ | | 25 | | 35 | | 45 | | 55 | ns |
| Output Enable to Output Valid | $t_{OE}$ | | 20 | | 25 | | 35 | | 40 | ns |
| Chip Select to Output in Low Z | $t_{CLZ}$[1] | 5 | | 5 | | 5 | | 5 | | ns |
| Output Enable to Output in Low Z | $t_{OLZ}$[1] | 5 | | 5 | | 5 | | 5 | | ns |
| Chip Select to Output in High Z | $t_{CHZ}$[1] | | 15 | | 20 | | 30 | | 35 | ns |
| Output Enable to Output in High Z | $t_{OHZ}$[1] | | 15 | | 20 | | 25 | | 30 | ns |

1. This parameter is guaranteed by design but not tested.

| Parameter | Symbol | Limits | | | | | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| **Read Cycle:** | | - 70 | | - 85 | | - 100 | | - 120 | | |
| | | Min | Max | Min | Max | Min | Max | Min | Max | |
| Read Cycle Time | $t_{RC}$ | 70 | | 85 | | 100 | | 120 | | ns |
| Address Access Time | $t_{AA}$ | | 70 | | 85 | | 100 | | 120 | ns |
| Output Hold from Address Change | $t_{OH}$ | 5 | | 15 | | 15 | | 15 | | ns |
| $\overline{CS}$ Access Time | $t_{ACS}$ | | 70 | | 85 | | 100 | | 120 | ns |
| Output Enable to Output Valid | $t_{OE}$ | | 50 | | 55 | | 60 | | 60 | ns |
| Chip Select to Output in Low Z | $t_{CLZ}$[1] | 5 | | 10 | | 10 | | 10 | | ns |
| Output Enable to Output in Low Z | $t_{OLZ}$[1] | 5 | | 5 | | 5 | | 5 | | ns |
| Chip Select to Output in High Z | $t_{CHZ}$[1] | | 40 | | 45 | | 50 | | 50 | ns |
| Output Enable to Output in High Z | $t_{OHZ}$[1] | | 40 | | 45 | | 50 | | 50 | ns |

1. This parameter is guaranteed by design but not tested.

## READ CYCLE TIMING DIAGRAM




1. Measured 200 mV steady State; guaranteed but not tested.

## AC CHARACTERISTICS

($V_{CC}$ = 5 V ± 10%, $V_{SS}$ = 0 V, $T_A$ = - 55°C to + 125°C)

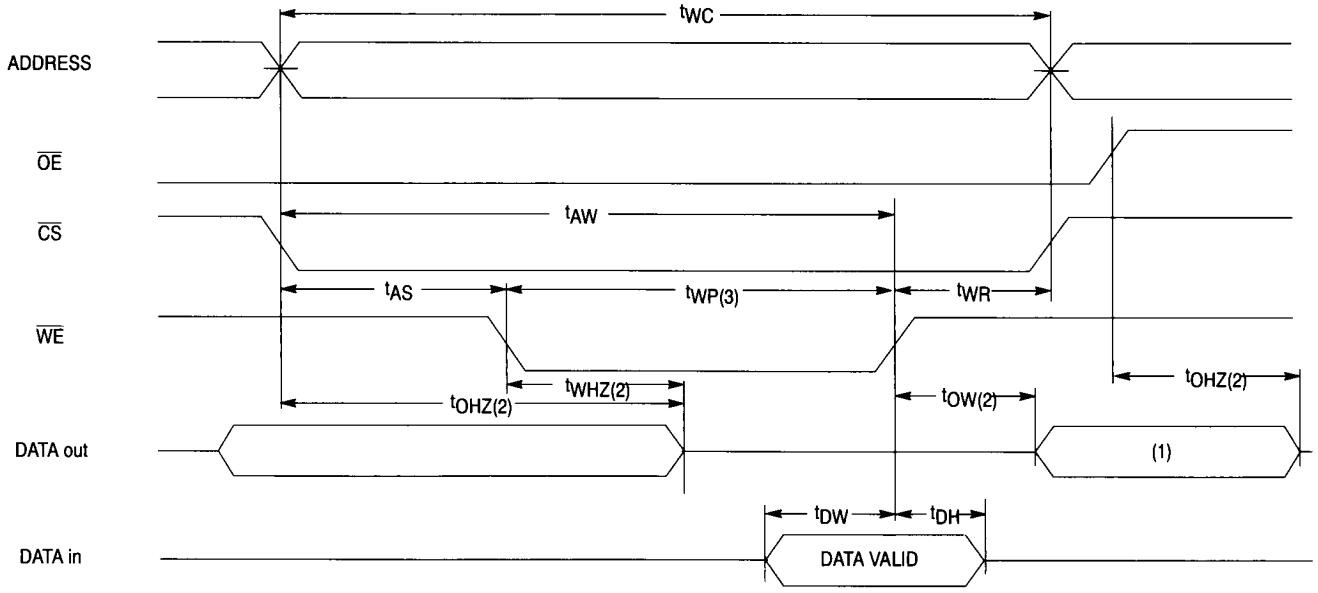
| Parameter | Symbol | Limits | | | | | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| **Write Cycle:** | | - 25 | | - 35 | | - 45 | | - 55 | | |
| | | Min | Max | Min | Max | Min | Max | Min | Max | |
| Write Cycle Time | $t_{WC}$ | 25 | | 35 | | 45 | | 55 | | ns |
| Address Valid to End of Write | $t_{AW}$ | 20 | | 25 | | 30 | | 50 | | ns |
| Data Valid to End of Write | $t_{DW}$ | 15 | | 20 | | 25 | | 30 | | ns |
| Write Pulse Width | $t_{WP}$ | 20 | | 25 | | 30 | | 40 | | ns |
| Address Setup Time | $t_{AS}$ | 0 | | 0 | | 0 | | 0 | | ns |
| Write Recovery Time | $t_{WR}$ | 0 | | 0 | | 0 | | 0 | | ns |
| Output Active from End of $\overline{WE}$ | $t_{OW}$[1] | 5 | | 5 | | 5 | | 5 | | ns |
| Write Enable to Output in High Z | $t_{WHZ}$[1] | 0 | 15 | 0 | 20 | 0 | 25 | 0 | 30 | ns |
| Data Hold Time | $t_{DH}$ | 0 | | 0 | | 0 | | 0 | | ns |

1. This parameter is guaranteed by design but not tested.

| Parameter | Symbol | Limits | | | | | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| **Write Cycle:** | | - 70 | | - 85 | | - 100 | | - 120 | | |
| | | Min | Max | Min | Max | Min | Max | Min | Max | |
| Write Cycle Time | $t_{WC}$ | 70 | | 85 | | 100 | | 120 | | ns |
| Address Valid to End of Write | $t_{AW}$ | 50 | | 75 | | 75 | | 85 | | ns |
| Data Valid to End of Write | $t_{DW}$ | 40 | | 45 | | 50 | | 50 | | ns |
| Write Pulse Width | $t_{WP}$ | 40 | | 65 | | 70 | | 80 | | ns |
| Address Setup Time | $t_{AS}$ | 0 | | 0 | | 0 | | 0 | | ns |
| Write Recovery Time | $t_{WR}$ | 0 | | 0 | | 0 | | 0 | | ns |
| Output Active from End of $\overline{WE}$ | $t_{OW}$[1] | 10 | | 10 | | 10 | | 10 | | ns |
| Write Enable to Output in High Z | $t_{WHZ}$[1] | 0 | 40 | 0 | 45 | 0 | 50 | 0 | 50 | ns |
| Data Hold Time | $t_{DH}$ | 0 | | 0 | | 0 | | 0 | | ns |

1. This parameter is guaranteed by design but not tested.

## WRITE CYCLE TIMING DIAGRAM



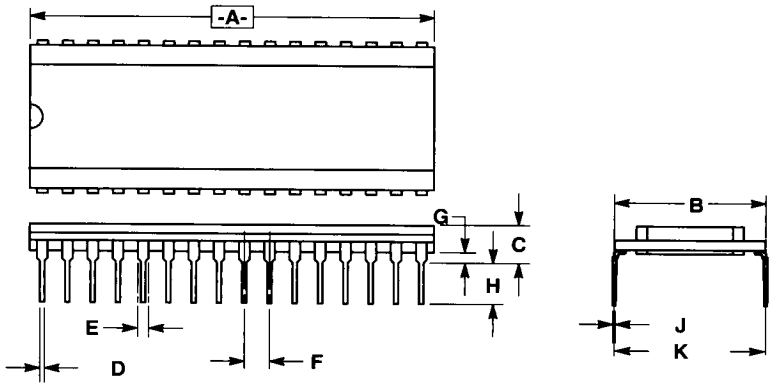

1. I/O pins are in their output state, input signals must not be applied.
2. This parameter is guaranteed by design but not tested.
3. A write occurs during the overlap ($t_{WP}$) of a low $\overline{CS}$ and a low $\overline{WE}$.

| Parameter | Symbol | Condition | Limits | | | | | | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | - 25 | | | - 35 | | | - 45 | | | |
| | | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| Data Retention Supply Voltage | $V_{DR}$ | $\overline{CS} \geq V_{CC}$ - 0.2 V | 2.0 | | 5.5 | 2.0 | | 5.5 | 2.0 | | 5.5 | V |
| Data Retention Current | $I_{CCDR1}$ | $V_{CC}$ = 3 V | | .5 | 8.0 | | .5 | 8.0 | | .5 | 8.0 | mA |
| | $I_{CCDR2}$ | $V_{CC}$ = 2 V | | .25 | 4.0 | | .25 | 4.0 | | .25 | 4.0 | mA |

| Parameter | Symbol | Condition | Limits | | | | | | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | - 55 | | | - 70 | | | - 85 | | | |
| | | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| Data Retention Supply Voltage | $V_{DR}$ | $\overline{CS} \geq V_{CC}$ - 0.2 V | 2.0 | | 5.5 | 2.0 | | 5.5 | 2.0 | | 5.5 | V |
| Data Retention Current | $I_{CCDR1}$ | $V_{CC}$ = 3 V | | .03 | 3.2 | | .03 | 3.0 | | .01 | 1.6 | mA |
| | $I_{CCDR2}$ | $V_{CC}$ = 2 V | | .02 | 2.1 | | .02 | 2.0 | | .007 | 1.2 | mA |

| Parameter | Symbol | Condition | Limits | | | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|
| | | | - 100 | | | - 120 | | | |
| | | | Min | Typ | Max | Min | Typ | Max | |
| Data Retention Supply Voltage | $V_{DR}$ | $\overline{CS} \geq V_{CC}$ - 0.2 V | 2.0 | | 5.5 | 2.0 | | 5.5 | V |
| Data Retention Current | $I_{CCDR1}$ | $V_{CC}$ = 3 V | | 10 | 1100 | | 10 | 1100 | µA |
| | $I_{CCDR2}$ | $V_{CC}$ = 2 V | | 7 | 850 | | 7 | 850 | µA |

## Package Outline




| DIM | MILLIMETERS | | INCHES | |
|---|---|---|---|---|
| | MIN | MAX | MIN | MAX |
| A | 40.23 | 41.05 | 1.584 | 1.616 |
| B | 13.8 | 14.1 | 0.544 | 0.556 |
| C | 3.68 | 5.08 | 0.145 | 0.200 |
| D | 0.4 | 0.5 | 0.016 | 0.020 |
| E | 1.1 | 1.4 | 0.045 | 0.055 |
| F | 2.5 TYP. | | 0.100 TYP. | |
| G | 0.635 | 1.524 | 0.025 | 0.060 |
| H | 3.2 MIN. | | 0.125 MIN. | |
| J | 0.23 | 0.30 | 0.009 | 0.012 |
| K | 15.0 | 15.5 | 0.590 | 0.610 |



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1PHX33389-0 PRINTED IN USA 3/93 IMPERIAL LITHO 90879 15,000 BIP MIL YDACAA

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