FUJITSU SEMICONDUCTOR
DATA SHEET

DS05–13110–3E

*Memory FRAM*

# 128 K (16 K × 8) Bit I²C

# MB85RC128

## ■ DESCRIPTION

The MB85RC128 is a FRAM (Ferroelectric Random Access Memory) Stand-Alone chip in a configuration of 16,384 words × 8 bits, using the ferroelectric process and silicon gate CMOS process technologies for forming the nonvolatile memory cells.

The MB85RC128 adopts the two-wire serial interface.

Unlike SRAM, the MB85RC128 is able to retain data without using a data backup battery.

The read/write endurance of the nonvolatile memory cells used for the MB85RC128 has improved to be at least $10^{10}$ cycles, significantly out performing Flash memory and E²PROM in the number.

The MB85RC128 does not need a polling sequence after writing to the memory such as the case of Flash memory nor E²PROM.

## ■ FEATURES

- Bit configuration : 16,384 words × 8 bits
- Operating power supply voltage : 2.7 V to 3.6 V
- Operating frequency : 400 kHz (Max)
- Two-wire serial interface : I²C-bus specification ver. 2.1 compliant, supports Standard-mode/ Fast-mode.
  Fully controllable by two ports: serial clock (SCL) and serial data (SDA).
- Operating temperature range : − 40 °C to +85 °C
- Data retention : 10 years ( + 75 °C)
- Read/write endurance : $10^{10}$ times
- Package : Plastic / SOP, 8-pin (FPT-8P-M02)
- Low power consumption : Operating current 0.15 mA (Max: @400 kHz), Standby current 5 μA (Typ)

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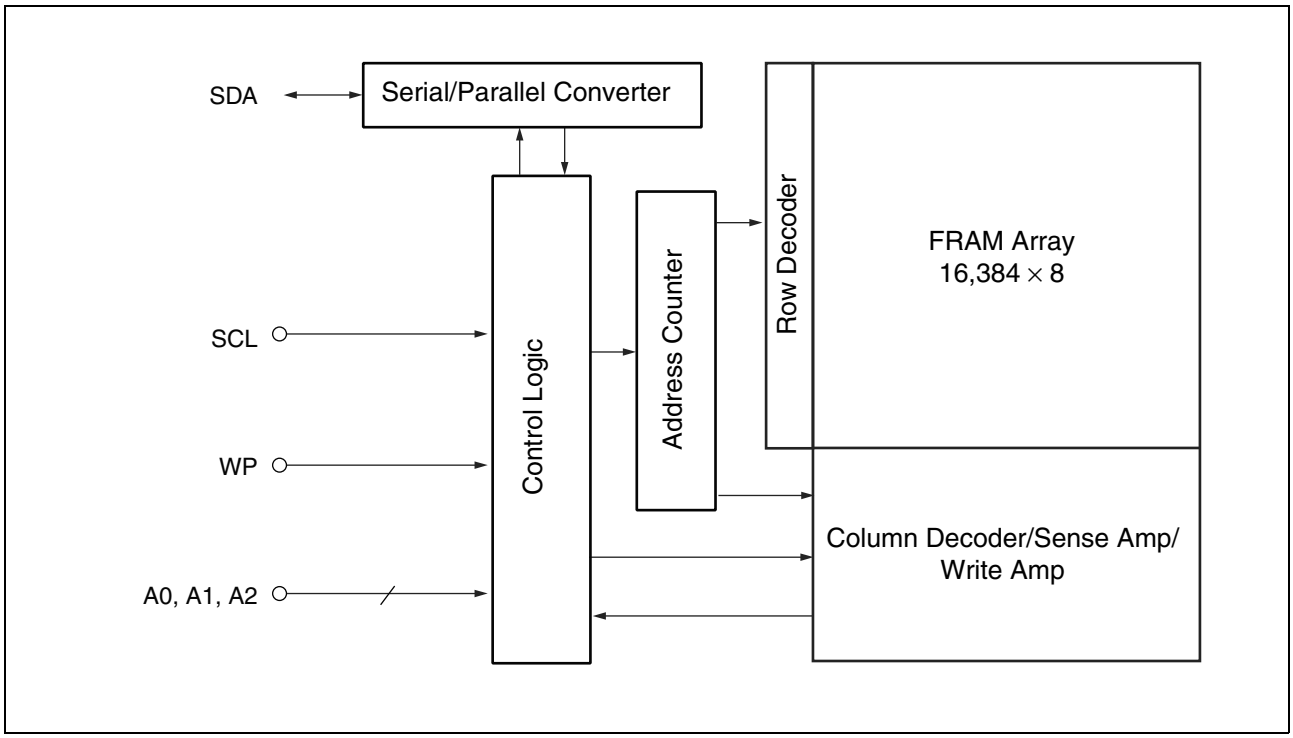
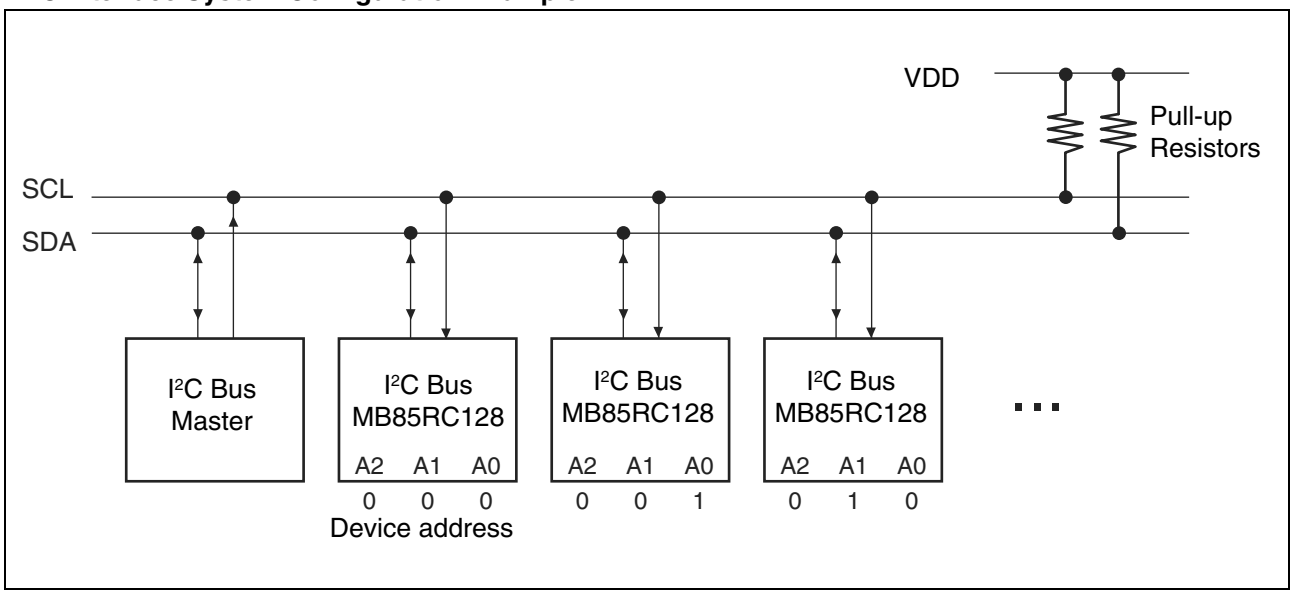
## ■ BLOCK DIAGRAM




## ■ I²C (Inter-Integrated Circuit)

The MB85RC128 has a two-wire serial interface, supports the I²C bus, and operates as a slave device. The I²C bus defines communication roles of “master” and “slave” devices, with the master side holding the authority to initiate control. Furthermore, a I²C bus connection is possible where a single master device is connected to multiple slave devices. In this case, it is necessary to assign a unique device address to the slave device, the master side starts communication after specifying the slave to communicate by addresses.

**• I²C Interface System Configuration Example**



## ■ I²C COMMUNICATION PROTOCOL

The I²C bus is a two wire serial interface that uses a bidirectional data bus (SDA) and serial clock (SCL). A data transfer can only be initiated by the bus master, which will also provide the serial clock for synchronization. The SDA signal should change while SCL is Low. However, as an exception, when starting and stopping communication sequence, SDA is allowed to change while SCL is High.

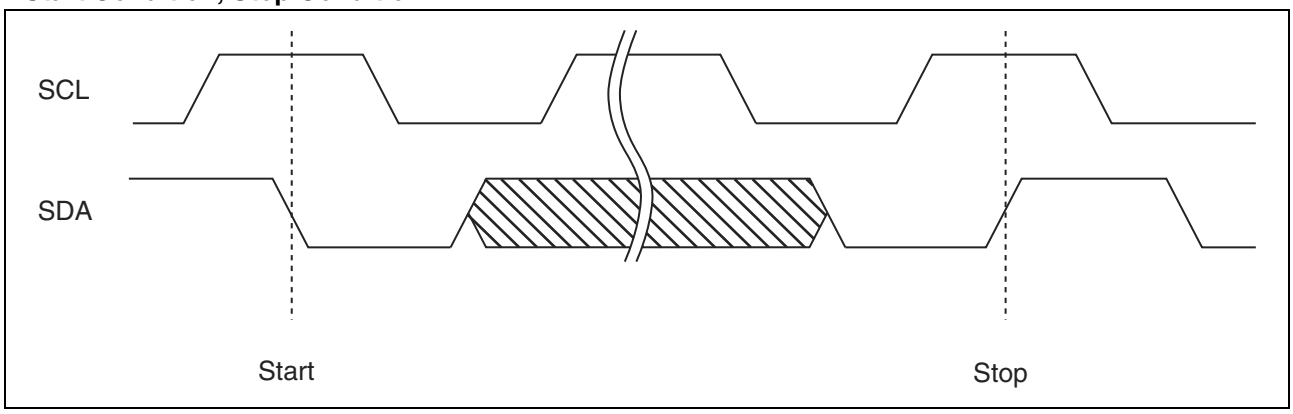
- Start Condition

To start read or write operations by the I²C bus, change the SDA input from High to Low while the SCL input is in the high state.

- Stop Condition

To stop the I²C bus communication, change the SDA input from Low to High while the SCL input is in the high state. In the reading operation, inputting the stop condition finishes reading and enters the standby state. In the writing operation, inputting the stop condition finishes inputting the rewrite data.

**• Start Condition, Stop Condition**



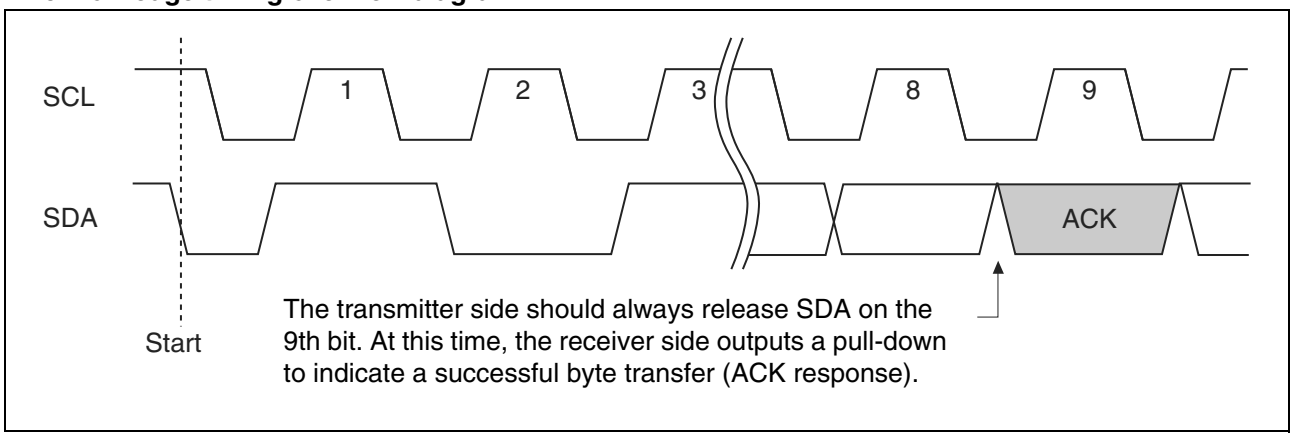

Note : The FRAM device does not need the programming wait time ($t_{WC}$) after issuing the Stop Condition during the write operation.

## ■ ACKNOWLEDGE (ACK)

In the I²C bus, serial data including address or memory information is sent in units of 8 bits. The acknowledge signal indicates that every each 8 bits of the data is successfully sent and received. The information receiver side usually outputs “L” every time on the 9th SCL clock after each 8 bits are successfully transmitted. On the transmitter side, the bus is temporarily released to Hi-Z every time on this 9th clock to allow the acknowledge signal to be received and checked. During this Hi-Z-released period, the receiver side pulls the SDA line down to indicate “L” that the previous 8bits communication is successfully received.

If the information receiver side detects Stop condition before driving the acknowledge “L”, the read operation ends and the I²C bus enters the standby state. If Stop condition is not sent, nor does the transmitter detect the acknowledge “L”, the bus remains in the released state “H” without doing anything.

**• Acknowledge timing overview diagram**



## ■ DEVICE ADDRESS WORD (Slave address)

Following the start condition, the bus master sends the 8bits device address word (Slave address) to start $I^2C$ communication. The device address word (8bits) consists of a device Type code (4bits), device address code (3bits), and a read/write code (1bit).

- Device Type Code (4bits)

The upper 4 bits of the device address word are a device type code that identifies the device type, and are fixed at “1010” for the MB85RC128.

- Device Address Code (3bits)

Following the device type code, the 3 bits of the device address code are input in order of A2, A1, and A0 pins. Each MB85RC128 is given a unique 3bits code on the device address pin (external hardware pin A2, A1, and A0). When the device address code is received by the slave device, the slave only responds if the hardware device address of which is equal to its unique 3bits code.

- Read/Write Code (1bit)

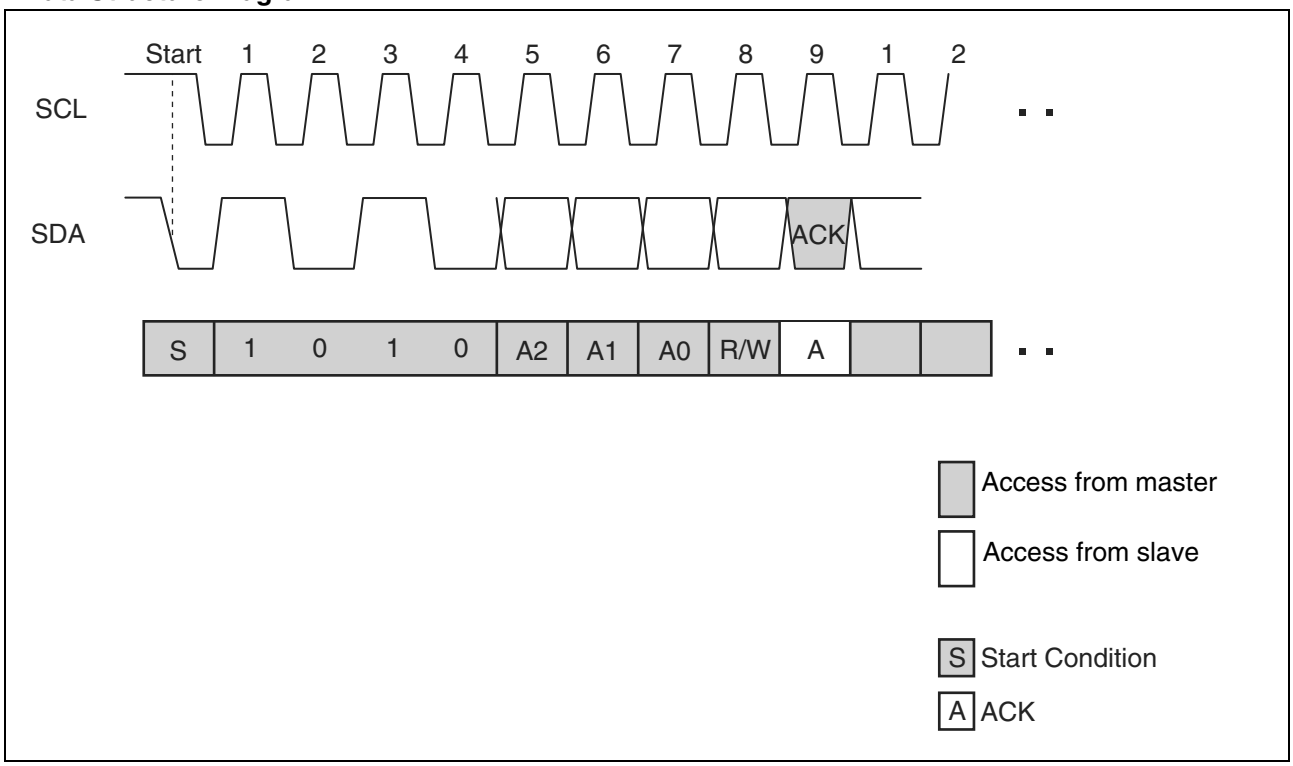
The 8th bit of the device address word is the R/W (read/write) code. When the R/W code is “L”, a write operation is enabled, and the R/W code is “H”, a read operation is enabled for the MB85RC128.

## ■ DATA STRUCTURE

In the I²C bus, the acknowledge “L” is output on the 9th bit after the 8 bits of the device and address word following the start condition. After confirming the acknowledge response at the slave, the I²C master outputs 8bits × 2 memory address to the I²C slave. When the memory address input ends, the slave again outputs the acknowledge “L”. After this operation, the I/O data follows in units of 8 bits, with the acknowledge “L” output after every 8bits.

It is determined by the R/W code whether the data line is driven by the master or the slave. For a write operation the slave will accept 8bits from the master then send an acknowledge. If the master detects the acknowledge, the master will transfer the next 8bits. For a read operation the slave will place 8bits on the I²C bus, then wait for an acknowledge from the master.

• **Data Structure Diagram**




## ■ FRAM ACKNOWLEDGE -- POLLING NOT REQUIRED

The MB85RC128 performs write operations at the same speed as read operations, so any waiting time for an ACK polling* does not occur. The write cycle takes no additional time.

*: As to E²PROM, the Acknowledge Polling is performed as a progress check in the write programming step. It places NAK condition on the bus as of “not acknowledged” during the writing programming period. The busy status for the write programming is given from 9th ACK bit. That “done” condition is placed onto I²C bus by E²PROM I²C device and your program had to poll the bus in order to sense that condition.

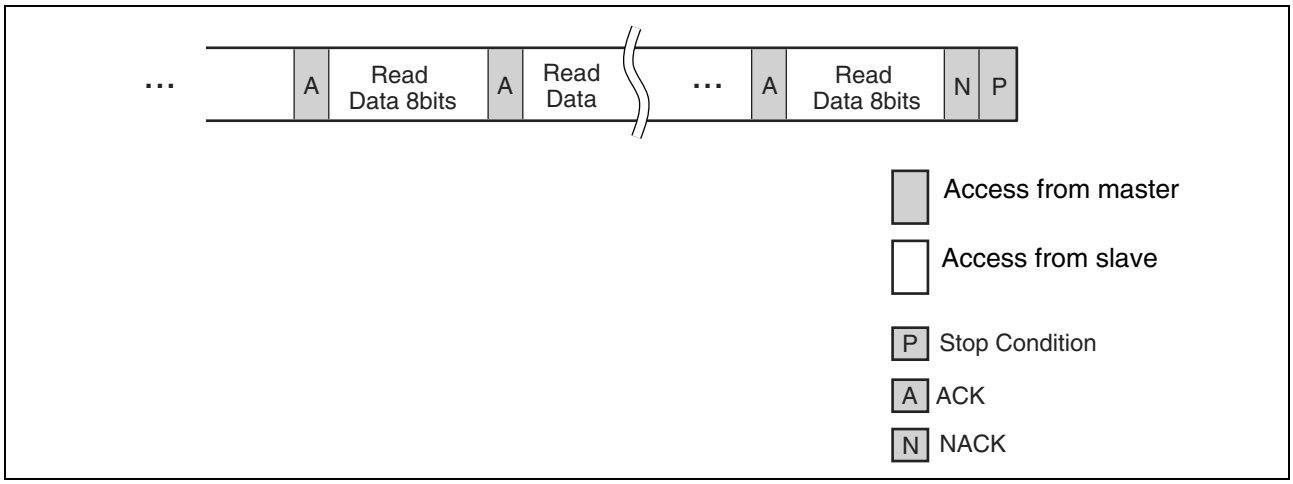
## ■ WRITE PROTECT (WP)

The entire memory array can be write protected using the Write Protect pin. When the Write Protect is set to “H”, the entire memory map will be write protected. When the write protect pin is “L”, all addresses may be overwritten.

Note : The Write Protect pin is pulled down internally to VSS pin, therefore if the Write Protect pin is open, the pin status is detected as Low (write enabled).

• Sequential Read

Data can be received continuously following the control byte after specifying the address the same as for Random Read. If the read exceeds the end of address for the MB85RC128, the internal read address automatically rolls over to $0000_H$.



## ■ ABSOLUTE MAXIMUM RATINGS

| Parameter | Symbol | Rating | | Unit |
|---|---|---|---|---|
| | | Min | Max | |
| Power supply voltage* | $V_{CC}$ | − 0.5 | +4.0 | V |
| Input pin voltage* | $V_{IN}$ | − 0.5 | $V_{CC}$ + 0.5 ( ≤ 4.0) | V |
| Output pin voltage* | $V_{OUT}$ | − 0.5 | $V_{CC}$ + 0.5 ( ≤ 4.0) | V |
| Ambient temperature | $T_A$ | − 40 | + 85 | °C |
| Storage temperature | Tstg | − 40 | + 125 | °C |

* : These parameters are based on the condition that VSS is 0 V.

WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

## ■ RECOMMENDED OPERATING CONDITIONS

| Parameter | Symbol | Value | | | Unit |
|---|---|---|---|---|---|
| | | Min | Typ | Max | |
| Power supply voltage* | $V_{CC}$ | 2.7 | 3.3 | 3.6 | V |
| “H” level input voltage* | $V_{IH}$ | $V_{CC} \times 0.8$ | — | $V_{CC}$ + 0.5 ( ≤ 4.0) | V |
| “L” level input voltage* | $V_{IL}$ | − 0.5 | — | + 0.6 | V |
| Ambient temperature | $T_A$ | − 40 | — | + 85 | °C |

* : These parameters are based on the condition that VSS is 0 V.

WARNING: The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.

Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their representatives beforehand.

## ■ ELECTRICAL CHARACTERISTICS

### 1. DC Characteristics

(within recommended operating conditions)

| Parameter | Symbol | Condition | Value | | | Unit |
|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | |
| Input leakage current | $\|I_{LI}\|$ | SCL, SDA = 0 V to $V_{CC}$<br>A0, A1, A2, WP = 0 V or $V_{CC}$ | — | — | 1 | µA |
| Output leakage current | $\|I_{LO}\|$ | $V_{OUT}$ = 0 V to $V_{DD}$ | — | — | 1 | µA |
| Operating power supply current | $I_{CC}$ | SCL = 400 kHz | — | 100 | 150 | µA |
| Standby current | $I_{SB}$ | SCL, SDA = $V_{CC}$<br>A0, A1, A2, WP = 0 V or $V_{CC}$ | — | 5 | 20 | µA |
| “L” level output voltage | $V_{OL}$ | $I_{OL}$ = 2 mA | — | — | 0.4 | V |

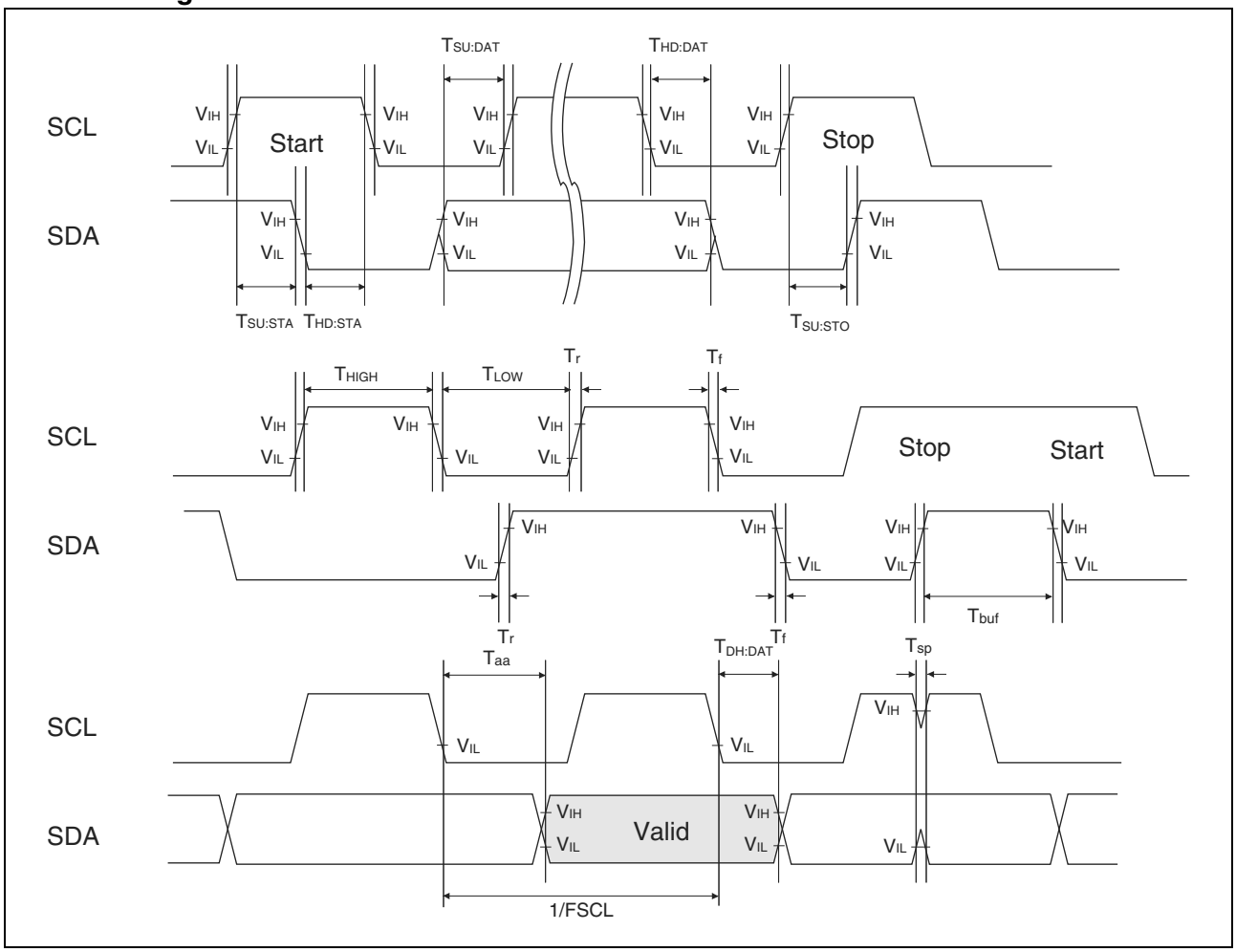
### 2. AC Characteristics

| Parameter | Symbol | Value | | Unit |
|---|---|---|---|---|
| | | Min | Max | |
| SCL clock frequency | FSCL | 0 | 400 | kHz |
| Clock high time | $T_{HIGH}$ | 600 | — | ns |
| Clock low time | $T_{LOW}$ | 1300 | — | ns |
| SCL/SDA rise time | $T_r$ | — | 300 | ns |
| SCL/SDA fall time | $T_f$ | — | 300 | ns |
| Start condition hold | $T_{HD:STA}$ | 600 | — | ns |
| Start condition setup | $T_{SU:STA}$ | 600 | — | ns |
| SDA input hold | $T_{HD:DAT}$ | 0 | — | ns |
| SDA input setup | $T_{SU:DAT}$ | 100 | — | ns |
| SDA output hold | $T_{DH:DAT}$ | 0 | — | ns |
| Stop condition setup | $T_{SU:STO}$ | 600 | — | ns |
| SDA output access after SCL fall | $T_{AA}$ | — | 900 | ns |
| Pre-charge time | $T_{BUF}$ | 1300 | — | ns |
| Pulse width ignored<br>(Input Filter on SCL and SDA) | $T_{SP}$ | — | 50 | ns |

AC characteristics were measured under the following measurement conditions.

| | |
|---|---|
| Power supply voltage | : 2.7 V to 3.6 V |
| Operating temperature | : – 40 °C to + 85 °C |
| Input voltage magnitude | : 0.3 V to 2.7 V |
| Input rise time | : 5 ns |
| Input fall time | : 5 ns |
| Input judge level | : $V_{CC}$/2 |
| Output judge level | : $V_{CC}$/2 |

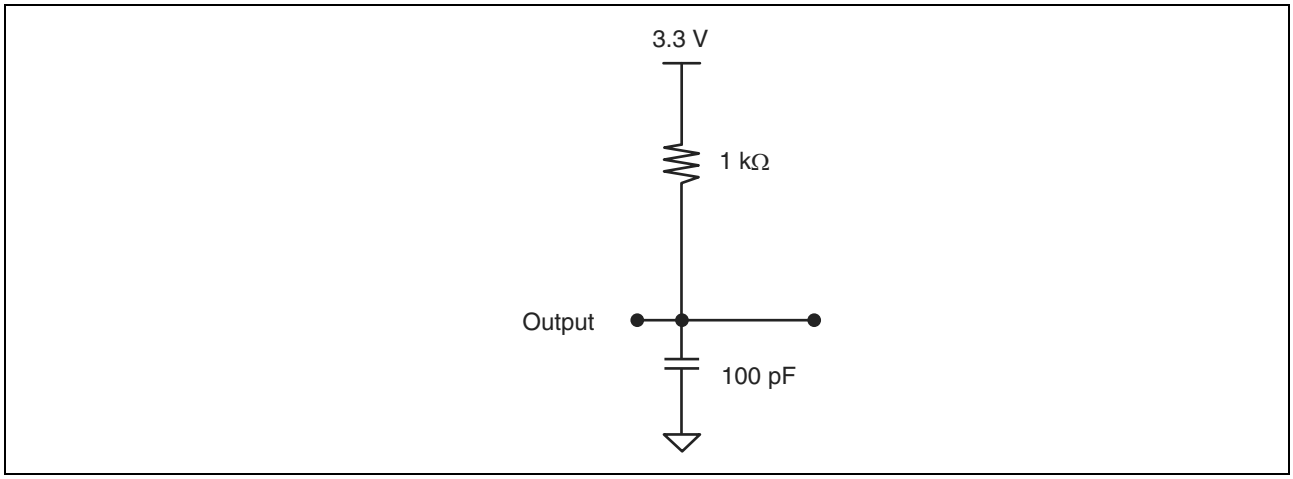
## 3. AC Timing Definitions




## 4. Pin capacitance

| Parameter | Symbol | Conditions | Value | | | Unit |
|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | |
| I/O capacitance | $C_{I/O}$ | $V_{IN} = V_{OUT} = 0$ V, f = 1 MHz, $T_A$ = + 25 °C | — | — | 15 | pF |
| Input capacitance | $C_{IN}$ | | — | — | 15 | pF |

### 5. AC Test Load Circuit



## ■ ORDERING INFORMATION

| Part number | Package | Remarks |
|---|---|---|
| MB85RC128PNF-G-JNE1 | 8-pin, plastic SOP (FPT-8P-M02) | |
| MB85RC128PNF-G-JNERE1 | 8-pin, plastic SOP (FPT-8P-M02) | Embossed Carrier tape |

# MEMO

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