Power MOSFET 14 Amps, 25 Volts

N-Channel DPAK

Features

- Planar HD3e Process for Fast Switching Performance
- Low R_{DS(on)} to Minimize Conduction Loss
- Low C_{iss} to Minimize Driver Loss
- Low Gate Charge
- Optimized for High Side Switching Requirements in High–Efficiency DC–DC Converters

MAXIMUM RATINGS (T_J = 25°C unless otherwise specified)

Parameter	Symbol	Value	Unit
Drain-to-Source Voltage	V_{DSS}	25	vdc
Gate-to-Source Voltage - Continuous	V_{GS}	±20	vdc
Thermal Resistance – Junction–to–Case Total Power Dissipation @ $T_A = 25^{\circ}C$ Drain Current – Continuous @ $T_A = 25^{\circ}C$, Chip – Continuous @ $T_A = 25^{\circ}C$, Limited by Package – Single Pulse (tp \leq 10 μ s)	$\begin{array}{c} R_{\thetaJC} \\ P_{D} \\ I_{D} \\ I_{D} \\ I_{D} \end{array}$	6.0 20.8 14 11.4 28	°C/W A A A
Thermal Resistance – Junction–to–Ambient (Note 1) Total Power Dissipation @ T _A = 25°C Drain Current – Continuous @ T _A = 25°C	R _{θJA} P _D I _D	80 1.56 3.1	°C/W W A
Thermal Resistance – Junction–to–Ambient (Note 2) Total Power Dissipation @ T _A = 25°C Drain Current – Continuous @ T _A = 25°C	R _{θJA} P _D I _D	120 1.04 2.5	°C/W W A
Operating and Storage Temperature Range	T _J , T _{stg}	-55 to 150	°C
Maximum Lead Temperature for Soldering Purposes, 1/8" from case for 10 seconds	TL	260	°C

- 1. When surface mounted to an FR4 board using 0.5 sq. in pad size.
- When surface mounted to an FR4 board using minimum recommended pad size.

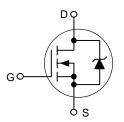


ON Semiconductor®

http://onsemi.com

14 AMPERES, 25 VOLTS $R_{DS(on)} = 70.4 \text{ m}\Omega \text{ (Typ)}$

N-CHANNEL



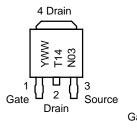


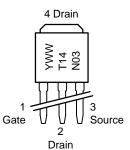
CASE 369C DPAK (Surface Mount) STYLE 2



CASE 369D DPAK (Straight Lead) STYLE 2

MARKING DIAGRAM & PIN ASSIGNMENTS





14N03 = Device Code Y = Year WW = Work Week

ORDERING INFORMATION

Device	Package	Shipping
NTD14N03R	DPAK	75 Units/Rail
NTD14N03R-1	DPAK Straight Lead	75 Units/Rail
NTD14N03RT4	DPAK	2500 Tape & Reel

ELECTRICAL CHARACTERISTICS ($T_J = 25$ °C unless otherwise specified)

Characteristics			Min	Тур	Max	Unit
OFF CHARACTERISTICS						
Drain-to-Source Breakdown Voltage (Note 3) (V _{GS} = 0 Vdc, I _D = 250 μAdc) Temperature Coefficient (Positive)			25 -	28 -	_ _	Vdc mV/°C
Zero Gate Voltage Drain Current (V _{DS} = 20 Vdc, V _{GS} = 0 Vdc) (V _{DS} = 20 Vdc, V _{GS} = 0 Vdc, T _J = 150°C)			_ _	- -	1.0 10	μAdc
Gate–Body Leakage Current (V _{GS} = ±20 Vdc, V _{DS} = 0 Vdc)			-	-	±100	nAdc
ON CHARACTERISTICS (Note 3)						
Gate Threshold Voltage (Note 3) $(V_{DS} = V_{GS}, \ I_D = 250 \ \mu Adc)$ Threshold Temperature Coefficient (Negative)			1.0	1.5 -	2.0	Vdc mV/°C
Static Drain-to-Source On-Resistance (Note 3) $ (V_{GS} = 4.5 \text{ Vdc}, I_D = 5 \text{ Adc}) $ $ (V_{GS} = 10 \text{ Vdc}, I_D = 5 \text{ Adc}) $			- -	117 70.4	130 95	mΩ
Forward Transconductance (Note 3) (V _{DS} = 10 Vdc, I _D = 5 Adc)			_	7.0	_	Mhos
DYNAMIC CHARACTERISTICS						
Input Capacitance		C _{iss}	_	115	_	pF
Output Capacitance	$(V_{DS} = 20 \text{ Vdc}, V_{GS} = 0 \text{ V}, f = 1 \text{ MHz})$	C _{oss}	_	62	-	1
Transfer Capacitance		C _{rss}	_	33	_	
SWITCHING CHARACTERISTICS	(Note 4)					
Turn-On Delay Time		t _{d(on)}	_	3.8	-	ns
Rise Time	(V _{GS} = 10 Vdc, V _{DD} = 10 Vdc,	t _r	_	27	-	1
Turn-Off Delay Time	$I_D = 5 \text{ Adc}, R_G = 3 \Omega)$	t _{d(off)}	_	9.6	_	
Fall Time		t _f	_	2.0	_	
Gate Charge		Q_{T}	_	1.8	_	nC
	$(V_{GS} = 5 \text{ Vdc}, I_D = 5 \text{ Adc}, V_{DS} = 10 \text{ Vdc}) \text{ (Note 3)}$	Q ₁	_	0.8	_	
	, , ,	Q ₂	_	0.7	_	
SOURCE-DRAIN DIODE CHARAC	TERISTICS					
Forward On-Voltage	$(I_S = 5 \text{ Adc}, V_{GS} = 0 \text{ Vdc}) \text{ (Note 3)}$ $(I_S = 5 \text{ Adc}, V_{GS} = 0 \text{ Vdc}, T_J = 125^{\circ}\text{C})$	V _{SD}	- -	0.93 0.82	1.2 -	V _{dc}
Reverse Recovery Time		t _{rr}	-	6.6	_	ns
	(I _S = 5 Adc, V _{GS} = 0 Vdc,	ta	-	4.75	_	1
	$dI_{S}/dt = 100 \text{ A/}\mu\text{s}) \text{ (Note 3)}$	t _b	-	1.88	_	1
Reverse Recovery Stored Charge			_	0.002	_	μС

Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.
 Switching characteristics are independent of operating junction temperatures.

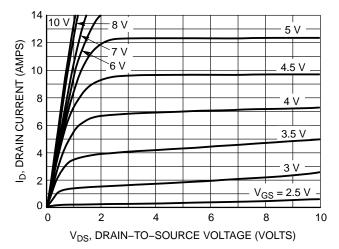


Figure 1. On-Region Characteristics

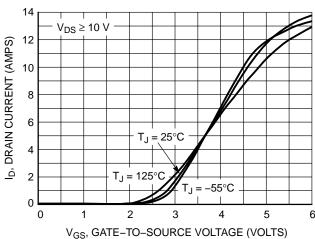


Figure 2. Transfer Characteristics

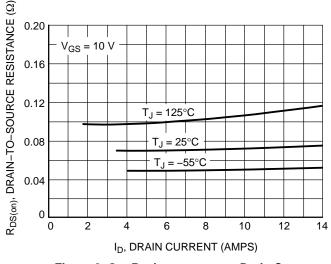


Figure 3. On–Resistance versus Drain Current and Temperature

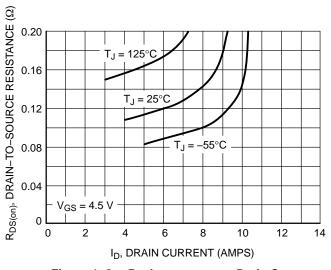


Figure 4. On-Resistance versus Drain Current and Temperature

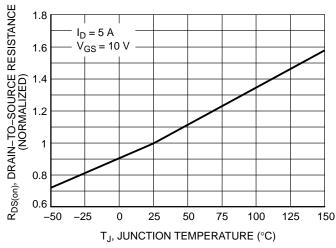


Figure 5. On–Resistance Variation with Temperature

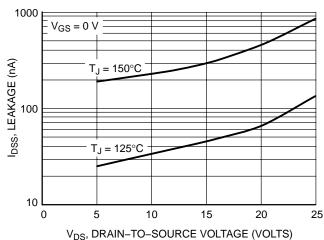


Figure 6. Drain-to-Source Leakage Current versus Voltage

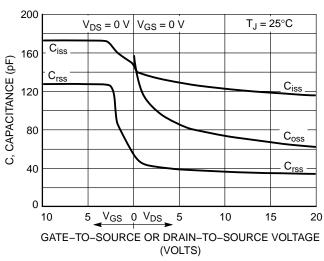


Figure 7. Capacitance Variation

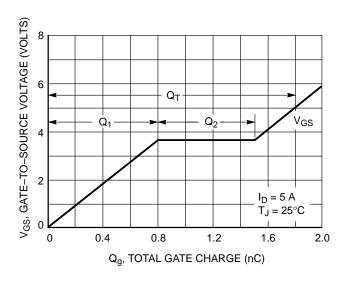


Figure 8. Gate-to-Source and Drain-to-Source Voltage versus Total Charge

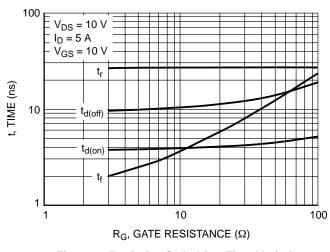


Figure 9. Resistive Switching Time Variation versus Gate Resistance

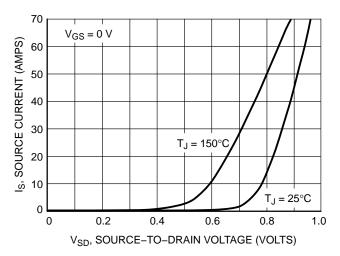
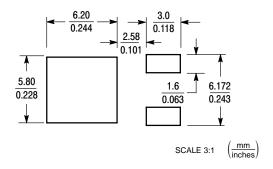


Figure 10. Diode Forward Voltage versus Current

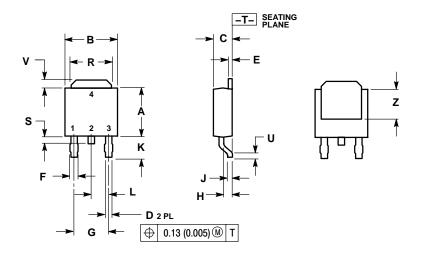
RECOMMENDED FOOTPRINTS FOR SURFACE MOUNTED APPLICATIONS

Surface mount board layout is a critical portion of the total design. The footprint for the semiconductor packages must be the correct size to ensure proper solder connection interface between the board and the package. With the correct pad geometry, the packages will self align when subjected to a solder reflow process.



PACKAGE DIMENSIONS

DPAK (SINGLE GAUGE) CASE 369C **ISSUE 0**



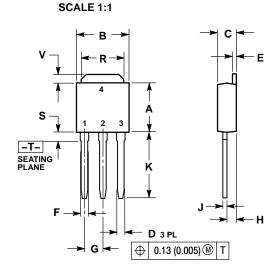
NOTES:

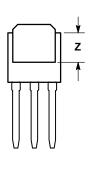
- 1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982. 2. CONTROLLING DIMENSION: INCH.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
Α	0.235	0.245	5.97	6.22
В	0.250	0.265	6.35	6.73
С	0.086	0.094	2.19	2.38
D	0.027	0.035	0.69	0.88
Е	0.018	0.023	0.46	0.58
F	0.037	0.045	0.94	1.14
G	0.180 BSC		4.58 BSC	
Н	0.034	0.040	0.87	1.01
J	0.018	0.023	0.46	0.58
K	0.102	0.114	2.60	2.89
L	0.090 BSC		2.29 BSC	
R	0.180	0.215	4.57	5.45
S	0.025	0.040	0.63	1.01
U	0.020		0.51	
٧	0.035	0.050	0.89	1.27
Z	0.155		3.93	

STYLE 2: PIN 1. GATE 2. DRAIN 3. SOURCE 4. DRAIN

DPAK (SINGLE GAUGE) CASE 369D **ISSUE 0**





NOTES:

- DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
 CONTROLLING DIMENSION: INCH.

	INCHES		MILLIN	IETERS
DIM	MIN	MAX	MIN	MAX
Α	0.235	0.245	5.97	6.35
В	0.250	0.265	6.35	6.73
С	0.086	0.094	2.19	2.38
D	0.027	0.035	0.69	0.88
Е	0.018	0.023	0.46	0.58
F	0.037	0.045	0.94	1.14
G	0.090 BSC		2.29 BSC	
Н	0.034	0.040	0.87	1.01
J	0.018	0.023	0.46	0.58
K	0.350	0.380	8.89	9.65
R	0.180	0.215	4.45	5.45
S	0.025	0.040	0.63	1.01
٧	0.035	0.050	0.89	1.27
Z	0.155		3.93	

STYLE 2: PIN 1. GATE

- 2. DRAIN 3. SOURCE 4. DRAIN

ON Semiconductor and are registered trademarks of Semiconductor Components Industries, LLC (SCILLC). SCILLC reserves the right to make changes without further notice to any products herein. SCILLC makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does SCILLC assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. "Typical" parameters which may be provided in SCILLC data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. SCILLC does not convey any license under its patent rights nor the rights of others. SCILLC products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the SCILLC product could create a situation where personal injury or death may occur. Should Buyer purchase or use SCILLC products for any such unintended or unauthorized application, Buyer shall indemnify and hold SCILLC and its officers, employees, subsidiaries, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that SCILLC was negligent regarding the design or manufacture of the part. SCILLC is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:

Literature Distribution Center for ON Semiconductor P.O. Box 5163, Denver, Colorado 80217 USA Phone: 303–675–2175 or 800–344–3860 Toll Free USA/Canada Fax: 303–675–2176 or 800–344–3867 Toll Free USA/Canada Email: orderlit@onsemi.com

N. American Technical Support: 800–282–9855 Toll Free LISA/Canada

Japan: ON Semiconductor, Japan Customer Focus Center 2–9–1 Kamimeguro, Meguro–ku, Tokyo, Japan 153–0051 Phone: 81–3–5773–3850

ON Semiconductor Website: http://onsemi.com

Order Literature: http://www.onsemi.com/litorder

For additional information, please contact your local Sales Representative.