AMD-K6®
Processor
I/O Model

Application Note

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Introduction

Advances in semiconductor process technology have allowed the performance of integrated circuits to increase dramatically. The operating frequency of output signals driven from these circuits continues to increase, while the switching transitions of these signals has decreased. These particular characteristics of high-speed signals pose challenges to a system designer responsible for the placement and routing of components on printed circuit boards (PCBs). In particular, the propagation delay of a signal must be considered to ensure that sufficient setup and hold time, with adequate margin, exist at a signal's destination. In addition, as the rise and fall times of signals decrease, the system designer must ensure the signal quality meets the system requirements.

Ensuring that system timing and signal quality objectives are met prior to PCB manufacturing reduces the development expense and expedites the time-to-market of a product. This application note describes the format and usage of the AMD-K6® processor I/O buffer behavioral model, which allows a system designer to perform analog simulations of processor signals that interface with the system logic. This model adheres to the *I/O Buffer Information Specification (IBIS), Version 3.2*.

IBIS Modeling

Overview

IBIS is a specification developed to provide an industry-standard method for semiconductor manufacturers to model the analog behavior of I/O buffers without disclosing proprietary process data. As the availability of IBIS models has grown, so too have the number of analog simulators that accept IBIS models.

IBIS Usage

Modeling a PCB Net

To simulate the analog behavior of a signal on a PCB net, all elements of the net must be modeled to ensure the simulator generates accurate results. A net that is driven by a signal that has a short switching transition relative to its propagation delay is best modeled as a transmission line. The general criterion used for deciding on a transmission line as an appropriate model is as follows:

$$T_{switch} < 2(T_{prop})$$

Where:

- T_{switch} is the time required for a signal to switch states
- T_{prop} is the time required for a signal to propagate from its source to its destination

The typical elements of a net sourced by the processor include the processor's I/O buffer (modeled using IBIS), the transmission line that models the PCB trace, the destination receiver(s), and any components used for termination (See Figure 1). This net topology is then defined in the format understood by the target simulator.

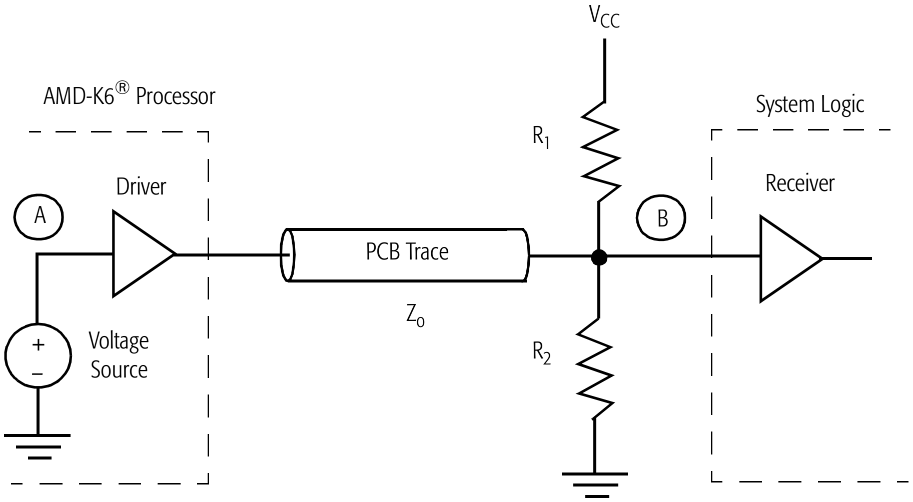

Figure 1. Modeling Example of Typical PCB Net

After the simulator has loaded the net input file, the simulator can be instructed to generate a rising or falling transition at the driver input to the processor driver (point 'A' in Figure 1). This signal generator is represented in Figure 1 by the voltage source input to the processor driver.

Setup and Hold Times

For each signal transition, the simulator can determine the signal propagation delay from point 'A' to point 'B' under worst-case, typical, and best-case conditions. The propagation delay under worst-case conditions is used to determine if the setup time at the destination receiver is met. Likewise, the progagation delay under best-case conditions is used to determine if the hold time at the destination receiver is met.

Figure 2 illustrates the timings that must be considered when determining whether the setup time of a signal is met. The timings are defined as follows:

- T_{period} is the period of the system clock
- T_{skew} is the maximum clock skew between the clock that launches a signal (solid-line clock) and the clock that captures a signal (dashed-line clock)
- T_{jitter} (not shown in Figure 2) is the maximum variance allowance between successive periods of the system clock
- $T_{validmax}$ is the maximum valid delay of a signal from its source

- $T_{propmax}$ is the maximum propagation delay of the signal along the PCB trace from its source to its destination. This delay is obtained by simulating with the worst-case conditions.
- $T_{setupmin}$ is the minimum required setup time of a signal at its destination

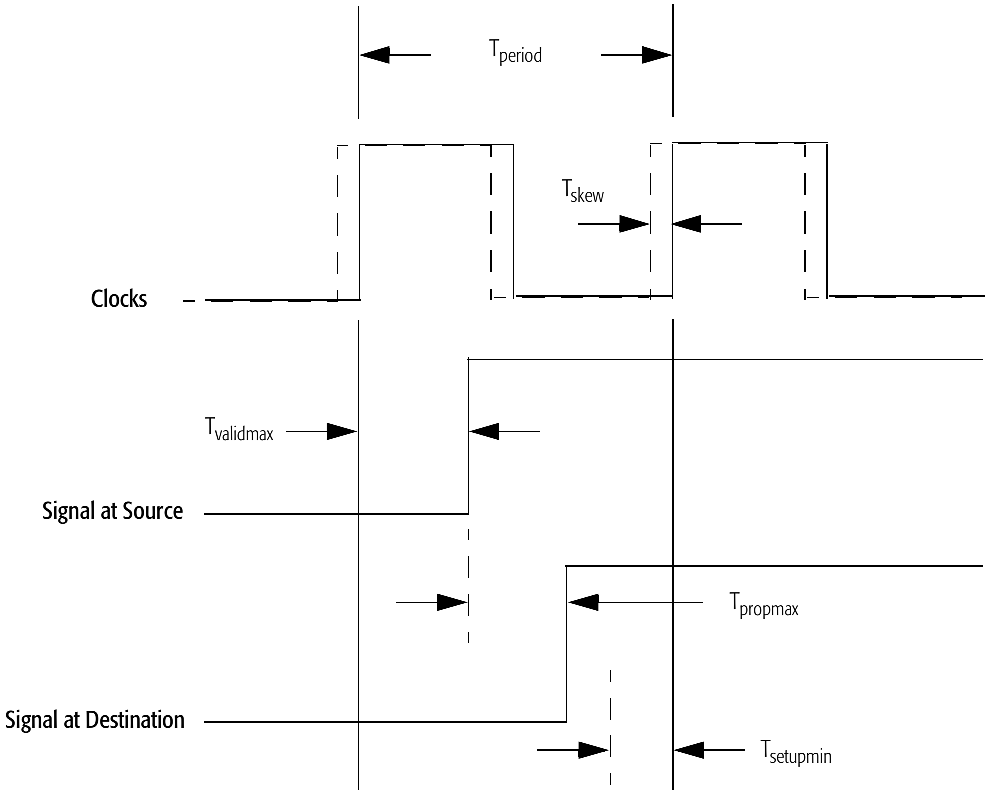

Figure 2. Timing Considerations for Meeting Setup Time

To ensure the setup time of a signal is met, the following relationship must be met:

$$T_{validmax} + T_{propmax} + T_{setupmin} < T_{period} - T_{skew} - T_{jitter}$$

Figure 3 illustrates the timings that must be considered when determining whether the hold time of a signal is met. The timings are defined as follows:

- T_{period} is the period of the system clock
- T_{skew} is the maximum clock skew between the clock that launches a signal (solid-line clock) and the clock that captures a signal (dashed-line clock)
- T_{jitter} (not shown in Figure 3) is the maximum variance allowance between successive periods of the system clock
- $T_{validmin}$ is the minimum valid delay of a signal from its source
- $T_{propmin}$ is the minimum propagation delay of the signal along the PCB trace from its source to its destination. This delay is obtained by simulating with the best-case conditions.
- $T_{holdmin}$ is the minimum required hold time of a signal at its destination

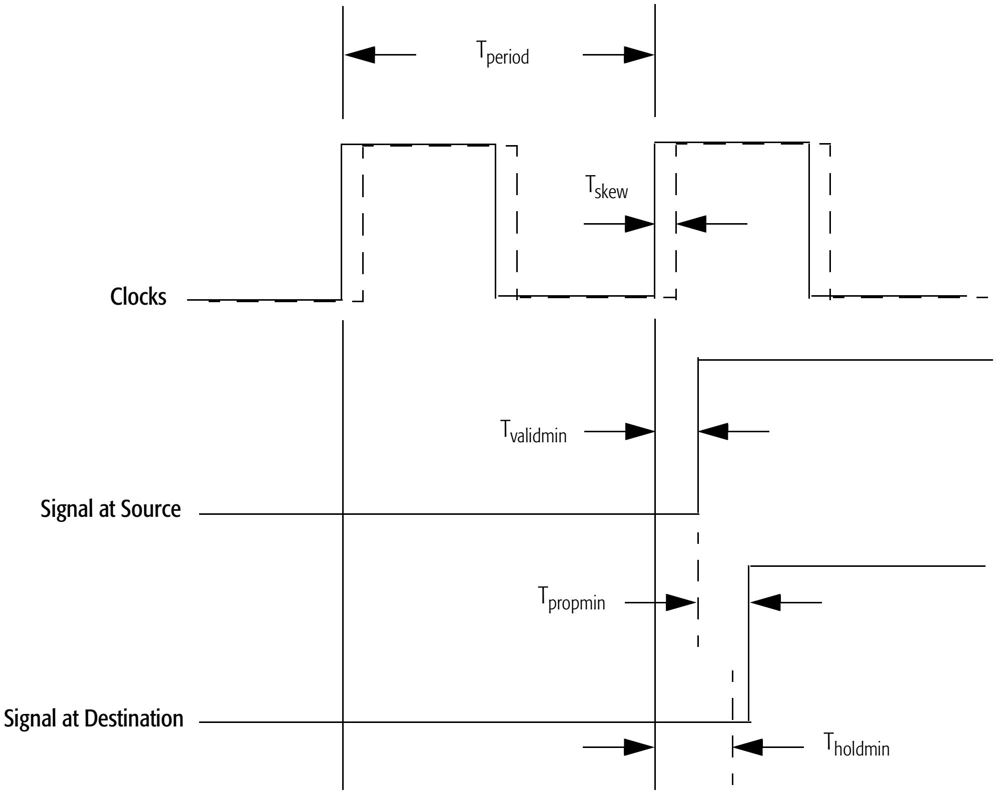

Figure 3. Timing Considerations to Meet Hold Time

To ensure the hold time of a signal is met, the following relationship must be met:

$$T_{validmin} + T_{propmin} - T_{skew} - T_{jitter} > T_{holdmin}$$

Signal Quality

In addition to providing propagation delays, the simulator can graphically display the output waveform presented at the output of the driver and the corresponding waveform produced at point ‘B’ in Figure 1. This display allows a designer to determine if the signal quality at the destination is acceptable. In addition to providing graphical data, most simulators generate numerical data that quantifies various signal quality characteristics.

The following list shows the signal quality characteristics that typically concern designers (all measurements are taken at the destination receiver):

- *Overshoot*—The difference between the maximum value of the voltage of a rising signal and the nominal I/O V_{CC} voltage (See Figure 4). Overshoot can adversely affect the reliability of the destination receiver. The time during which a signal remains above the nominal I/O V_{CC} voltage is also a reliability factor.
- *Undershoot*—The difference between the minimum value of the voltage of a falling signal and ground (See Figure 5). As with overshoot, undershoot can adversely affect the reliability of the destination receiver.
- *Ringback*—In the case of a rising waveform, the difference between the nominal I/O V_{CC} voltage and the minimum voltage of a signal after that signal has reached its maximum value. In the case of a falling waveform, ringback is the difference between the maximum voltage of a signal after that signal has reached its minimum value and ground (See Figures 4 and 5). Excessive ringing can cause the destination receiver to falsely switch if the signal traverses the switching threshold of the receiver.
- *Ring Settling Time*—In the case of a rising waveform, the time between when a signal crosses one-half of the nominal V_{CC} I/O voltage and when the signal settles within the specified tolerance of the I/O V_{CC} voltage. In the case of a falling waveform, ring settling time is the time between when a signal crosses one-half of the nominal I/O V_{CC} voltage and when the signal settles within a specific

percentage above and below ground (the percentage is dependent upon the electrical characteristics of the destination receiver). See Figure 6 for an example of ring settling time for a rising waveform. Settling time that approaches the period of the clock that launches a signal can potentially increase the switching time of that signal. This increase occurs if the signal is advancing in the opposite direction of the signal transition that occurs on the next clock edge.

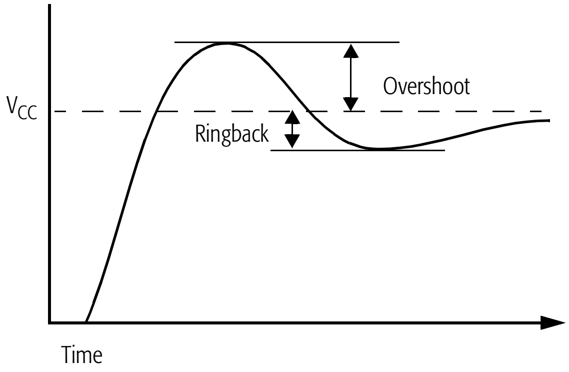

Figure 4. Example of Overshoot

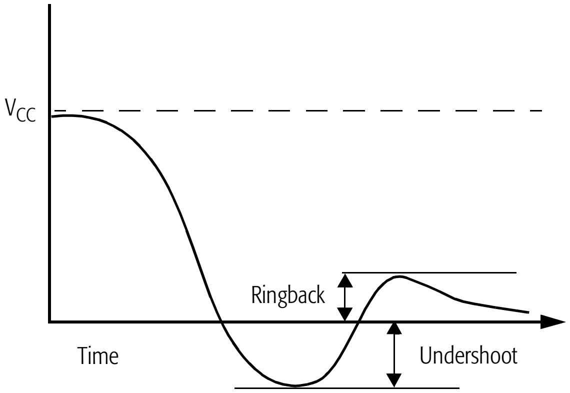

Figure 5. Example of Undershoot

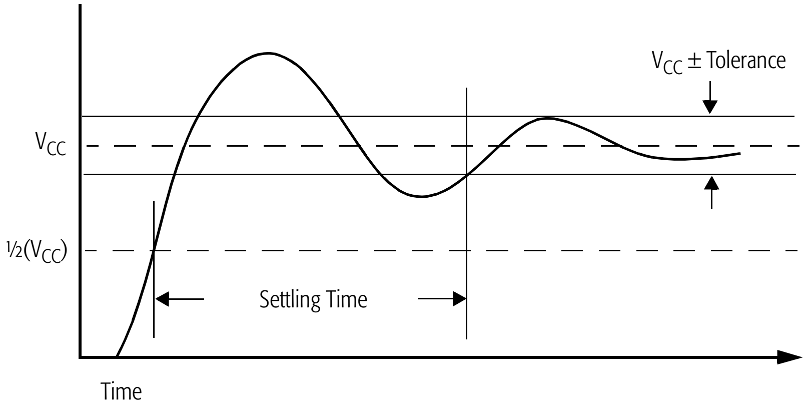

Figure 6. Example of Ring Settling Time for Rising Waveform

IBIS Structure

The IBIS specification defines a template that describes the properties of most elements of an I/O buffer design. The template uses required keywords and sub-parameters as well as optional keywords. The keywords and sub-parameters used by the AMD-K6 processor IBIS model, along with their definitions, are as follows:

- *IBIS Ver*—Specifies the version of the IBIS model.
- *File name*—Specifies the name of the file that contains the model.
- *File Rev*—Specifies the revision of the IBIS model.
- *Date*—Specifies the date the IBIS model was last modified.
- *Copyright*—The copyright claim.
- *Component*—Specifies the name of the component the model represents.
- *Manufacturer*—Specifies the manufacturer of the component.
- *Package* (R_pkg, L_pkg, C_pkg)—Specifies the R/L/C values of the package. These values are specified as 0 because the package R/L/C values are accounted for in the R_pin, L_pin, and C_pin sub-parameters of the *Pin* keyword.
- *Pin* (signal_name, model_name, R_pin, L_pin, C_pin, C_comp)—Itemizes each physical pin number along with its signal name, its I/O buffer name (K6STD or K6STG), and its R/L/C values. Power, ground, and no-connect pins do not

have R/L/C values specified. C_comp specifies the capacitance of the silicon die.

- *Model* (model_type, Vinl, Vinh, Vmeas, Cref, Rref, Vref)—Specifies the type of I/O buffer. K6STD and K6STG are the two buffers defined for the AMD-K6 processor. K6STD represents the standard strength driver and K6STG represents the strong strength driver.

  The model_type of both K6STD and K6STG is I/O, Vinl equals 0.8V, Vinh equals 2.0V, and Vmeas = 1.5V. Cref, Rref, and Vref, which represent the test load under which the specified propagation delays and switching times are defined. Rref = ∞; Cref and Vref = 0.
- *Temperature Range*—Specifies the temperature range within which the operation of the component is guaranteed.
- *Voltage Range*—Specifies the I/O voltage range.
- *Pulldown*—Specifies the voltage versus current (V/I) curves of the pulldown device within the I/O buffer.
- *Pullup*—Specifies the V/I curves of the pullup device within the I/O buffer.
- *GND Clamp*—Specifies the V/I curves of the ground clamp device within the I/O buffer.
- *POWER Clamp*—Specifies the V/I curves of the power clamp device within the I/O buffer.
- *Ramp* (dV/dt_r, dV/dt_f, R_load)—Specifies the rise and fall times of a signal at a load defined by R_load. R_load is equal to 50 ohms.
- *Rising Waveform*—Specifies the voltage versus time (V/T) curves of the rising edge of the waveform.
- *Falling Waveform*—Specifies the V/T curves of the falling edge of the waveform.

In addition to the keywords above, IBIS 3.x allows modeling drivers with multi-V/I characteristics and more detailed package modeling. Because the AMD-K6 processor family has multi-V/I drivers, it is recommended to use simulators that support the IBIS 3.x standard.

- *Package Model*—Specifies the package model name. The package model may be contained in the same file or it can be a separate file.

- *Pin Mapping*—Specifies the power and ground buses to which a driver is connected. This is important when modeling ground bounce or simultaneous switching noise.
- *Driver Schedule*—Specifies the switching sequence and time for referenced sub-models to produce a multi-stage driver.
- *Define Package Model*—Specifies the start of a package model description.
- *Number of Sections*—Specifies the number of sections that make up the connection between the die pad and the corresponding package pin. It may include the C4 bump, the connection between the bump pad and pin, and the pin itself.
- *Number of Pins*—Specifies to the IBIS parser the number of pins in the model.
- *Pin Numbers*—Specifies the names for the package pins and also defines pin ordering. If the *Number of Sections* keyword is used, *Pin Numbers* also list the elements for each section of the die to pin connection.
- *End Package Model*—Indicates the end of a package model description.

IBIS Models

AMD has developed I/O buffer models that represent the characteristics of the AMD-K6 processor family. The model files are specific to particular models of the AMD-K6 processor. Each model file contains a Standard I/O Model (K6STD) and a strong I/O Model (K6STG), and these models are assigned to their respective I/O pins. The description contained in each file specifies the AMD-K6 processor's model and stepping to which the model is applicable.

I/O Model

The IBIS Model files are available from the AMD web site at *http://www.amd.com*.