CS-51033

Low Voltage PFET Buck Controller

Description

The CS-51033 is a PFET switching regulator controller for use in DC-DC converters specializing in regulating 3.3V, ±5%, to output voltages as low as 1.25V. The CS-51033 can be used in the buck topology with a minimum number of external components. It consists of a 1A power driver for controlling the gate of a discrete P-channel transistor, a fixed frequency oscillator, short circuit protection timer, fast output voltage monitoring comparator, and output stage driver logic with latch.

The CS-51033 will be available in 8L SO and 8L PDIP plastic packages.

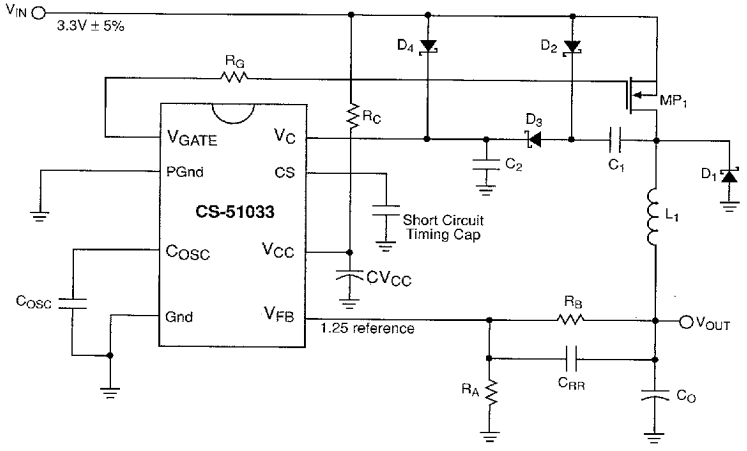
Features

- No Stability Compensation Required
- High Speed Oscillator (700kHz max)
- 1A Sink/Source Gate Drive
- Lossless Short Circuit Protection
- Programmable Soft Start

Absolute Maximum Ratings

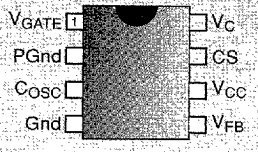
Power Supply Voltage, V_{CC} 3.465V
Driver Supply Voltage, V_C 16V
Driver Output Voltage, V_{GATE} 16V
C_{OSC}, CS, V_{FB} (Logic Pins) 3.465V
Peak Output Current 1A
Operating Junction Temperature, T_J ..... 150°C
Operating Temperature Range, T_A ..... -40° to 85°C
Storage Temperature Range, T_S ..... -65 to 150°C
ESD (Human Body Model) 2kV
Lead Temperature Soldering
Wave Solder (through hole styles only) ..... 10 sec. max, 260°C peak
Reflow (SMD styles only) ..... 60 sec. max above 183°C, 230°C peak

Typical Application Diagram



Package Options

8 Lead SO Narrow & PDIP



Cherry Semiconductor Corporation
2000 South County Trail
East Greenwich, Rhode Island 02818-1530
Tel: (401)885-3600 Fax (401)885-5786
email: info@cherry-semi.com
a CHERRY company

Electrical Characteristics: Specifications apply for $3.135 \le V_{CC} \le 3.465V$, $V_C = 5V$, $-40°C \le T_A \le 85°C$, $-40°C \le T_J \le 150°C$, unless otherwise specified.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
■ Oscillator	$C_{OSC} = 100pF$; $V_{FB} = 1.2V$; $V_{CS} = 2V$				
Max. Frequency		500			kHz
Trimmed Frequency	$C_{OSC} = 470pF$	160	200		kHz
Charge Current	$1.4V < VC_{OSC} < 2V$		120		µA
Discharge Current	$2.7V > VC_{OSC} > 2V$		730		µA
Maximum Duty Ratio	$1 - (t_{OFF}/t_{ON})$	80.0	83.3		%
■ Short Circuit Timer	$V_{FB} = 1.2V$; $C_S = 0.1µF$; $VC_{OSC} = 2V$				
Charge Current	$1V < V_{CS} < 2V$	175	264	325	µA
Fast Discharge Current	$V_{CS} = 2.55V$ from 2V; $V_{FB} = 1V$	40	66	80	µA
Slow Discharge Current	$V_{CS} = 2V$ from 2.55V; $V_{FB} = 1V$	4	6	10	µA
Start Fault Inhibit Time	$V_{CS} = 0V$ to 2.5V	0.754	1.000	1.450	ms
Run Fault Inhibit Time	$V_{CS} = 1.5V$ to 2.5V	0.277	0.380	0.630	ms
Valid Fault Time 1	$V_{CS} = 2.6V$ to 2.4V	0.25	0.30	0.50	ms
Valid Fault Time 2	$V_{CS} = 2.5V$ to 2.4V	0.06	0.15	0.37	ms
GATE Inhibit Time	$V_{CS} = 2.4V$ to 1.5V	9	15	15	ms
Fault OFF/ON Ratio	$\frac{\text{GATE Inhibit Time}}{\text{Run Fault Inhibit Time + Valid Fault Time 2}}$	22:1	28:1	36:1	
■ CS Comparator	$C_S = 100pF$; $V_{FB} = 1V$; $VC_{OSC} = 2V$				
Fault Enable C_S Voltage			2.5		V
Max. C_S Voltage	$V_{FB} = 1.5V$		2.6		V
Fault Detect Voltage	V_{CS} when GATE high		2.4		V
Fault Inhibit Voltage	Minimum V_{CS}		1.5		V
Hold Off Release Voltage	Drive ENABLE with $V_{CS} > 1V$	0.4	0.7	1.0	V
Regulator Threshold	$V_{CS} = 1.2V$	0.296	0.329	0.362	V
Voltage Clamp	$V_{CS} = 1.8V$	0.681	0.757	0.833	V
	$V_{CS} = 2.2V$	0.970	1.078	1.186	V
■ V_{FB} Comparator	$VC_{OSC} = V_{CS} = 2V$				
Regulator Threshold Voltage	$T_A = 25°C$	1.225	1.250	1.275	V
	$-40 \le T_J \le 150°C$	1.210	1.250	1.290	V
Fault Threshold Voltage	$T_A = 25°C$	1.12	1.15	1.17	V
	$-40 \le T_J \le 150°C$	1.10	1.15	1.19	V
Threshold Line Regulation	$3.135V < V_{CC} < 3.465V$		6	15	mV
Input Bias Current	$V_{FB} = 0V$		1	4	µA
Voltage Tracking	(Regulator Threshold Voltage - Fault Threshold Voltage)	80	100	120	mV
Overdrive				20	mV
■ Power Stage	$V_C = 5V$; $V_{FB} = 1.2V$				
GATE DC Low Saturation Voltage	$VC_{OSC} = 1V$; 200mA Sink		1.2	1.5	V
GATE DC High Saturation Voltage	$VC_{OSC} = 2.7V$; 200mA Source; $V_C = V_{GATE}$		1.5	2.0	V
Rise Time	$C_{GATE} = 1nF$; $1V < V_{GATE} < 4V$		30	60	ns
Fall Time	$C_{GATE} = 1nF$; $4V > V_{GATE} > 1V$		25	50	ns
■ Current Drain					
I_{CC}			3.50	2.55	mA
I_C			4.5	6.0	mA

Package Pin Description

PACKAGE PIN #	PIN SYMBOL	FUNCTION
8L SO Narrow & PDIP		
1	V_{GATE}	Driver pin to gate of external PFET.
2	PGnd	Output power stage ground connection.
3	C_{OSC}	Oscillator frequency programming capacitor.
4	Gnd	Logic ground.
5	V_{FB}	Feedback voltage input.
6	V_{CC}	Logic supply voltage.
7	CS	Soft start and fault timing capacitor.
8	V_C	Driver supply voltage.

Circuit Description

Theory of Operation

CONTROL SCHEME

The CS-51033 has a unique control scheme that does not need a current-sense resistor to control the PFET's pulse width. It simply monitors and controls the output ripple to determine when to turn on the PFET. This feature increases efficiency since most current-sense schemes need a 100mV drop across an external sense resistor resulting in I^2R power loses, which can become excessive at moderate to high load currents.

The CS-51033's method of control is very simple. If V_{FB} falls below the internal reference voltage of 1.25V during the oscillator's charge cycle, the CS-51033 turns on the PFET. The PFET gets turned off and remains off during the oscillator's discharge cycle setting the maximum duty cycle to 85.7%. The CS-51033 needs 7mV typical, 15mV maximum ripple on the V_{FB} to operate. Note that this method of control does not require any loop stability compensation, simplifying the power supply design.

STARTUP

The CS-51033 has an externally programmable softstart feature that allows the power supply to come up slowly, preventing voltage overshoot on the output. The following describes the startup procedure of the CS-51033. At startup, the voltage on all pins will be zero. Referring to Figures 1 and 2, the voltage on V_C will be a diode drop below V_{CC} as V_{CC} rises. This V_C voltage along with the internal resistor R_G will keep the PFET off by keeping the gate to source voltage equal to a diode drop.

As V_{CC} continues to rise, the oscillator capacitor (C_{OSC}) and the Softstart/Fault Timing capacitor (CS) begin to charge via internal current sources. Referring to the block diagram, C_{OSC} gets charged by the current source IC and CS gets charged by the I_{CS} source where

$$I_{CS} = I_T - \left(\frac{I_T}{55} + \frac{I_T}{5} \right).$$

The internal Holdoff Comparator (A7) ensures that the external PFET is off until $V_{CS} > 0.7V$ by preventing the GATE flip-flop (F2) from being set. This allows the oscillator to reach its operating frequency before enabling the drive output.

Softstart is obtained by clamping the V_{FB} comparator's (A6) reference input to approximately 1/2 V_{CS} during startup, permitting the control loop and the output regulation voltage to slowly start up and reduce overshoots. Referring to Figure 2, once the CS pin charges above the holdoff trip point of 0.7V, the low feedback to the V_{FB} Comparator is allowed to set the GATE flip-flop only during C_{OSC}'s charge cycle. Once the GATE flip-flop is set, V_{GATE} goes low and turns on the PFET device which activates the external V_C charge pump circuit and allows V_{FB} to rise. When V_{CS} exceeds 2.4V, the CS charge sense comparator (A4) sets the V_{FB} comparator reference to 1.25V completing the startup cycle.

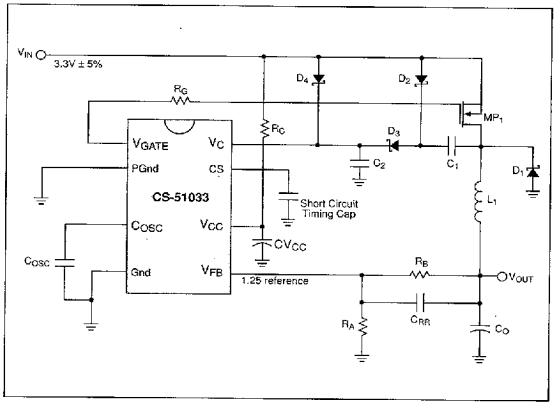


Figure 1. CS-51033 Typical Operating Circuit.

CHARGE PUMP CIRCUIT

Under worst case conditions, the V_{GATE} high side drive transistor will have a saturation voltage of 2V. Since the drive transistor's saturation voltage is equal to V_{GS}, 2V may be enough to keep the PFET at 100% duty cycle. An external charge pump circuit is needed to keep V_C at or above 5V to compensate for the driver saturation voltage and ensure that the PFET can be shut off.

The following is a discussion of how the charge pump circuit functions. Please refer to Figure 1. Once $3.3V_{IN}$ is applied, capacitors C2 and C5 will be charged to a V_{BE} below V_{IN} via diodes D1 and D2, respectively. This initial

stored charged across C2 provides the necessary power for the driver to pull down V_{GATE} and turn on the PFET. When the PFET turns on, its drain voltage will be approximately equal to $3.3V_{IN}$. Since C5 tries to maintain the voltage across itself, node 1 will also try to increase by 3.3V for an end result of 2*3.3V-VD2. C1 will end up transferring some of its stored charge to C2 via D3. V_C will equal

$$2 \times 3.3V - VD2 - VD3,$$

after a cycle of the PFET.

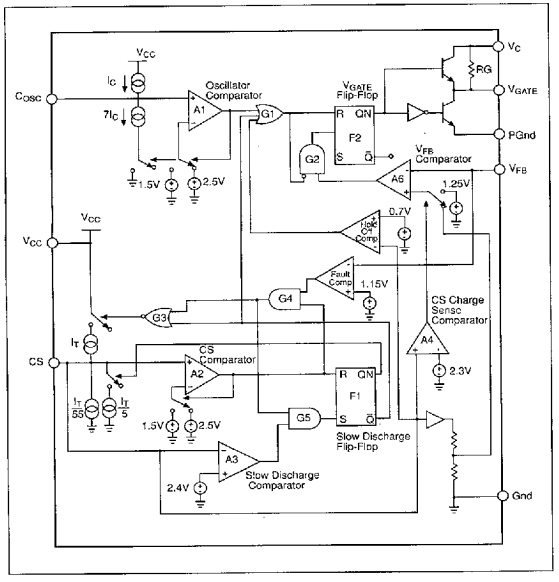


Figure 2. Simplified Functional Diagram

LOSSLESS SHORT CIRCUIT PROTECTION

The CS-51033's short circuit protection scheme is considered "lossless" since no sense resistor is needed. The controller compares the output DC voltage against the CS pin voltage to determine if a true fault is occurring. Please refer to Figures 2 and 3 for the following discussion. The CS cycle under a constant fault condition (sometimes referred to as hiccup mode) can be broken up into 3 sections; $t_{RESTART}$, $t_{FAST\ DISCHARGE}$, and t_{FAULT}.

- The $t_{RESTART}$ section of Figure 3 represents only 1.96% of the entire CS duty cycle. Note that the PFET operates under a short circuit condition because the internal fault circuitry is not enabled until the fault capacitor is charged to 2.5V. Referring to Figure 2, A2's low output keeps G4 disabled, blocking A5's high output.
- $t_{FAST\ DISCHARGE}$ makes up 0.9% of the entire CS duty cycle (labeled td2 in Figure 3) and it occurs once V_{CS} reaches 2.5V. The CS pin will be discharged from 2.5V to 2.4V during fast discharge mode. The purpose of this section is to reduce false faults due to transient on the V_{FB} pin (see S1 and S2 in Figure 3). If V_{FB} returns above 1.15V before CS has been discharged to 2.4V, a false fault has been detected and the CS pin will be allowed to charge back up to 2.6V where it will wait for the next instance where V_{FB} will go below 1.5V. Referring to Figure 2, once CS reaches 2.5V, A2's output will go high enabling G4. Now A5 can discharge the CS capacitor by turning off the charge current.
- The last section of the CS cycle is called t_{FAULT} which makes up 97.1% of the entire CS cycle. If a fault is still present when the CS pin is discharged to 2.4V, an active fault is detected and the discharge current is reduced by a factor of 12. The CS pin will then be slowly discharged from 2.4V to 1.5V while keeping the PFET gate driver disabled during the entire slow discharge time. This allows the average power dissipation of the PFET to be very low.

The short circuit current of this eval board is 100mA RMS. As seen in Figure 10, the CS period is approximately 6.5mS. Note that V_{GATE} is on for a very short period of time.

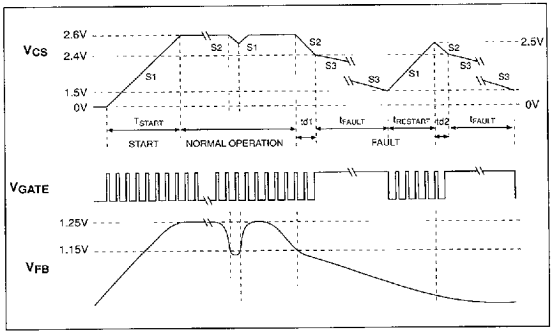


Figure 3. Voltage on start capacitor (V_{GS}), the gate (V_{GATE}), and in the feedback loop (V_{FB}), during startup, normal and fault conditions.

BUCK REGULATOR OPERATION

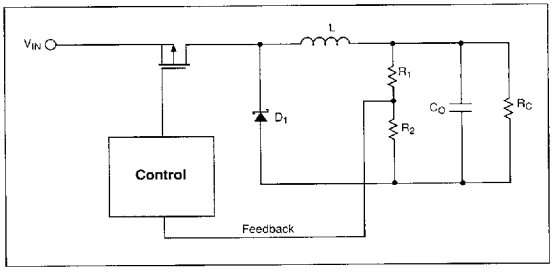


Figure 4. Buck Regulator Block Diagram

A block diagram of a typical buck regulator is shown in Figure 4. If we assume that the output transistor is initially off, the inductor current I_L is zero and the output voltage is at its nominal value. The current drawn by the load is supplied by the output capacitor C_O. When the voltage across C_O drops below the threshold established by the feedback resistors R1 and R2 and the reference voltage V_{REF}, the output transistor switches on and current flows through the inductor to the output. The inductor current rises at a rate determined by V/L. The duty cycle (or "on" time) for the CS-51033 is limited to 85.7.

Designing a Power Supply with the CS-51033

Design Example: 5V to 3.3V, 5A Buck Converter

Input Variables:

Oscillator Frequency ..... f_{SW} = 400kHz
Output Voltage ..... V_{ODC} = 1.5V
Diode Drop Voltage ..... V_D = 1.5V
Reference Voltage ..... V_{REF} = 1.25V
PFET Sat. Voltage ..... V_{SAT} = 0.2V
PFET Max Current ..... I_{MAX} = 2A
Fault Timer Ref. Voltage ..... $V_{THFAULT}$ = 1.15V
Comparator Hysteresis ..... HYST = 12mV
Comparator Bias Current ..... I_{IB} = 4µA
Fault Timer Charge Current ..... I_{CHRGT} = 264µA
Fault Timer Start Voltage ..... $V_{F(ENABLE)}$ = 2.5V
Max. Input Voltage Ripple ..... $V_{IN(RIP)}$ = 0.1V
Load Current ..... I_L = 1.5A
V_{FB} Resistor Divider Total ..... R_T = 1.8k

V_{IN} Input Capacitor Selection

$V_{IN(RIP)}$ is the maximum square wave voltage ripple the chip can withstand and regulate accurately.

(size capacitor greater than 200nF and for ESR requirements)

$$R_{IN} = V_{IN(RIP)} \frac{R_L}{V_{ODC}} \; ; \; \mathbf{R_{IN} = 0.02}$$

$$\mathbf{C_{IN} = 470\mu F}$$

Output Capacitor Selection

(size capacitor for ESR and transient load requirements)

$$\mathbf{C_O = 470\mu F}$$

$$I_{RIPPLE} = 0.15 \times \frac{V_{ODC}}{R_L} \; ; \text{Ripple Current} = 15\% \text{ of Load Current}$$

$$= 15\% \times 1.5A = 0.225A$$

$$R_{ESR} = \frac{V_{HYST}}{I_{RIPPLE}} \; ; \; \mathbf{R_{ESR} = 89m\Omega}$$

Inductor Selection

$$L = \left[\frac{R_{ESR}}{V_{HYST}\left[1 + \frac{V_{ODC} + V_D}{(V_{IN(MIN)} - V_{SAT} - V_{ODC})}\right] \times f_{SW}} \right] \times (V_D + V_{ODC})$$

$$I_L = \frac{V_{ODC}}{R_L} = 1.5A$$

L = 10µH; size inductor for 1.5A

Oscillator Capacitor Selection

$$C_{OSC} = \frac{9.429 \times 10^{-5}}{f_{SW}}$$

$$\mathbf{C_{OSC} \cong 220pF}$$

Feedback Resistor Selection

$$R_A = R_T \times \frac{V_{REF}}{V_{ODC}} = 1.5k$$

$$R_B = R_T - R_A = 300\Omega$$

Short Circuit Timer Capacitor Selection

$$C_S = R_L (1.05 \times 10^{-4}) \times \left| \ln\left(1 - \frac{V_{ODC}}{I_{MAX} \times R_L}\right) \right| \times 1.15 \times C_O$$

$$\mathbf{C_S \cong 0.1\mu F}$$

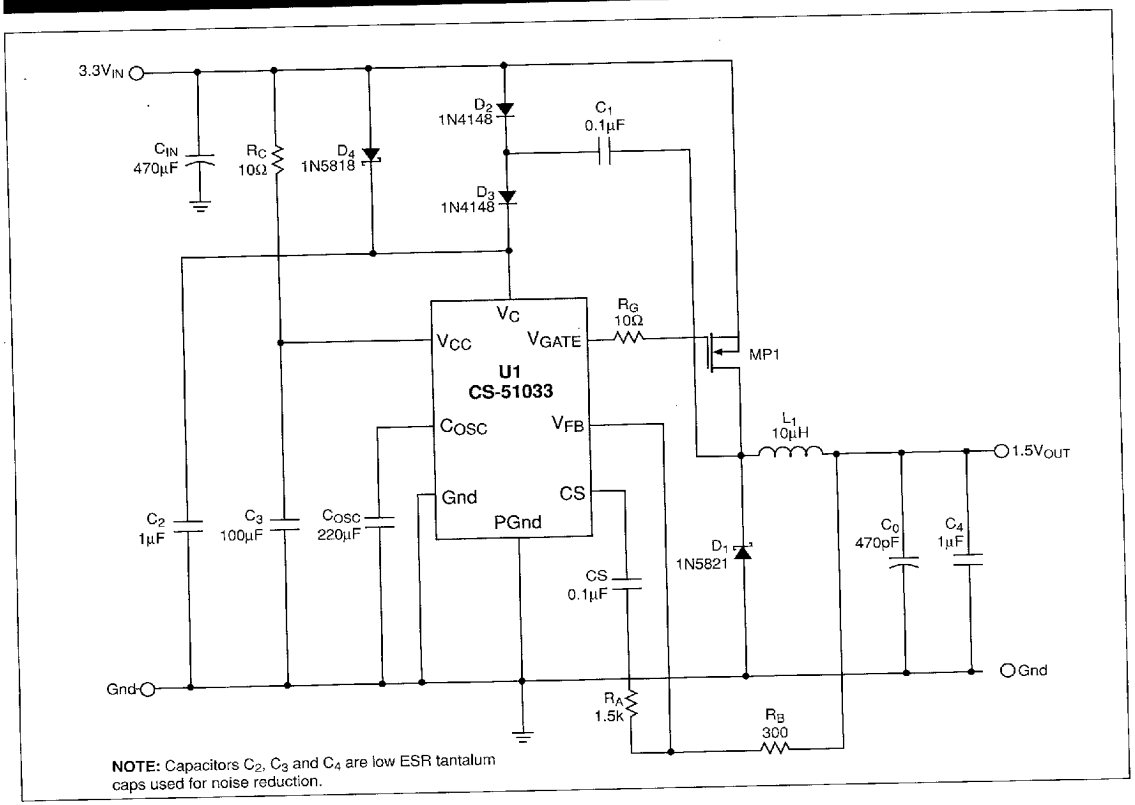


Figure 5. CS-51033 Application Diagram.

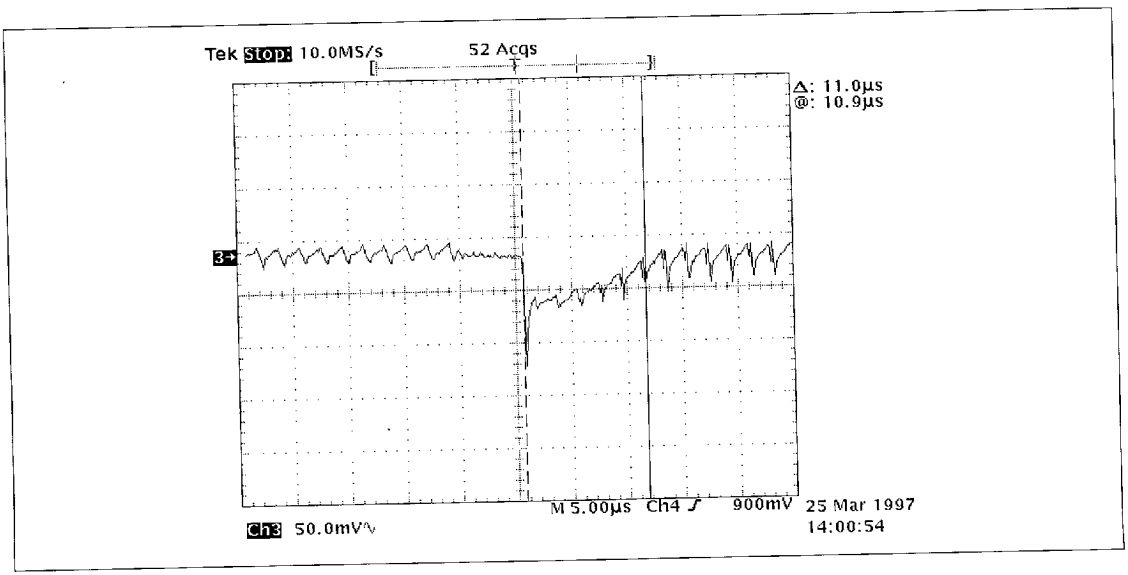


Figure 6. 3.3V to 1.5V, 1.5A converter response to 1.3A pulsed load.

Package Specification

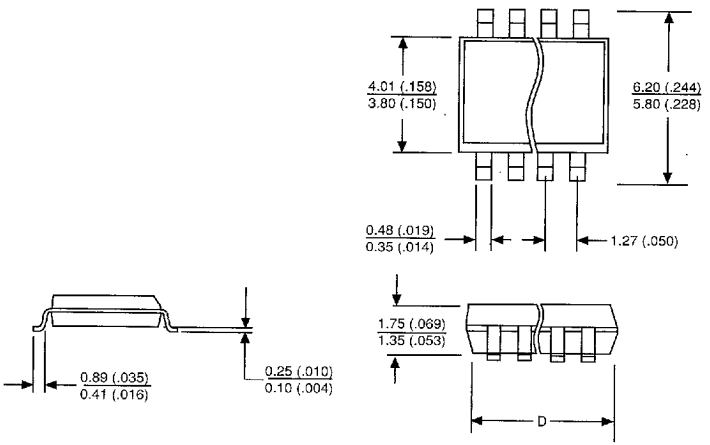
PACKAGE DIMENSIONS IN mm (INCHES)

Lead Count	D			
	Metric		English	
	Max	Min	Max	Min
8L SO Narrow	5.00	4.80	.197	.188
8L PDIP	9.40	9.14	.370	.360

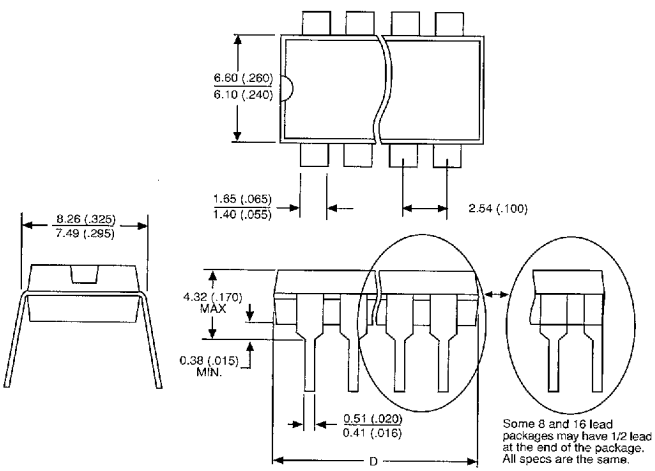
PACKAGE THERMAL DATA

Thermal Data		8L SO Narrow	8L PDIP	
$R_{\theta JC}$	typ	45	42	°C/W
$R_{\theta JA}$	typ	165	80	°C/W

8L SO Narrow; 150 mil wide



8L PDIP; 300 mil wide



Ordering Information

Part Number	Description
CS-51033D8	8L SO Narrow
CS-51033N8	8L PDIP

Advance

This product is in the early stages of the design process. CSC™ reserves the right to make changes to the specifications or discontinue development without notice. Please contact CSC for the latest available information.