CYPRESS SEMICONDUCTOR

CYM1610

16K x 16 Static RAM Module

Features

- **High-density 256K-bit SRAM module**
- **High-speed CMOS SRAMs**
  - **Access time of 12 ns**
- **Low active power**
  - **3W (max.)**
- **Hermetic SMD technology**
- **TTL-compatible inputs and outputs**
- **Low profile**
  - **Max. height of .215 in.**
- **Small PCB footprint**
  - **1.2 sq. in.**
- **JEDEC-defined pinout**
- **Independent byte select**
- **2V data retention (L version)**

Functional Description

The CYM1610 is a high-performance 256-kbit static RAM module organized as 16K words by 16 bits. This module is constructed from four 16K x 4 SRAMs in leadless chip carriers mounted on a ceramic substrate with pins.

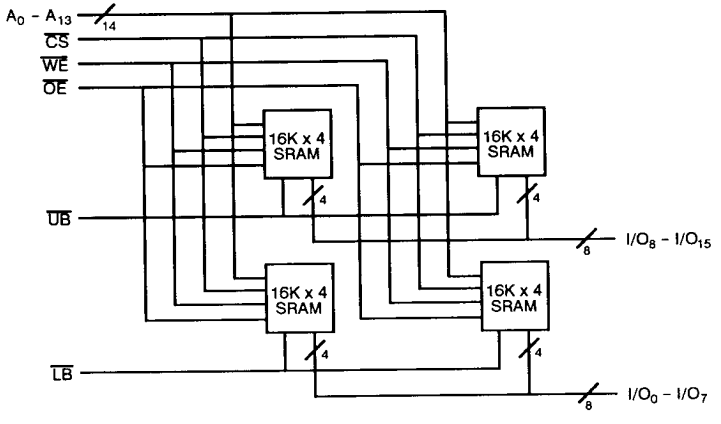
Selecting the device is achieved by a chip select input pin as well as two byte select pins ($\overline{UB}$, $\overline{LB}$) for independently selecting upper or lower byte for read or write operations.

Writing to the memory module is accomplished when the chip select ($\overline{CS}$), byte select ($\overline{UB}$, $\overline{LB}$) and write enable ($\overline{WE}$) inputs are LOW. Data on the input/output pins of the selected byte (I/O_8 – I/O_{15}, I/O_0 – I/O_7) is written into the memory location specified on the address pins (A_0 through A_{13}).

Reading the device is accomplished by taking chip select ($\overline{CS}$), byte select ($\overline{UB}$, $\overline{LB}$) and output enable ($\overline{OE}$) LOW, while $\overline{WE}$ remains inactive or HIGH. Under these conditions, the contents of the memory location specified on the address pins will appear on the appropriate data input/output pins.

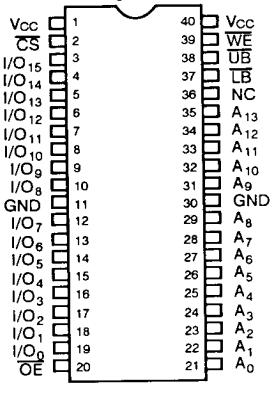
The input/output pins remain in a high-impedance state when chip select ($\overline{CS}$), byte select ($\overline{UB}$, $\overline{LB}$) or output enable ($\overline{OE}$) is HIGH, or write enable ($\overline{WE}$) is LOW.

Logic Block Diagram



Pin Configuration

DIP
Top View



Selection Guide

		1610HD-12	1610HD-15	1610HD-20	1610HD-25	1610HD-35	1610HD-45	1610HD-50
Maximum Access Time (ns)		12	15	20	25	35	45	50
Maximum Operating Current (mA)	Com'l	550	550	330	330	330	330	330
	Mil		550	550	360	330	330	330
Maximum Standby Current (mA)	Com'l	250	250	60	60	60	60	60
	Mil		250	250	60	60	60	60

Maximum Ratings

(Above which the useful life may be impaired)

Storage Temperature ..... −65°C to +150°C

Ambient Temperature with Power Applied ..... −55°C to +125°C

Supply Voltage to Ground Potential ..... −0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State ..... −0.5V to +7.0V

DC Input Voltage ..... −0.5V to +7.0V

Output Current into Outputs (Low) ..... 20 mA

Static Discharge Voltage ..... >2001V (Per MIL-STD-883 Method 3015.2)

Latch-Up Current ..... >200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ± 10%
Military	−55°C to +125°C	5V ± 10%

Electrical Characteristics Over the Operating Range

Parameters	Description	Test Conditions	1610HD-12 1610HD-15 1610HD-20M		1610HD-20C 1610HD-25 1610HD-35 1610HD-45 1610HD-50		Units
			Min.	Max.	Min.	Max.	
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = −4.0 mA	2.4		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 8.0 mA		0.4		0.4	V
V_{IH}	Input HIGH Voltage		2.2	V_{CC}	2.2	V_{CC}	V
V_{IL}	Input LOW Voltage		−0.5	0.8	−0.5	0.8	V
I_{IX}	Input Load Current	GND ≤ V_I ≤ V_{CC}	−15	+15	−15	+15	µA
I_{OZ}	Output Leakage Current	GND ≤ V_O ≤ V_{CC}, Output Disabled	−15	+15	−15	+15	µA
I_{OS}	Output Short Circuit Current [1]	V_{CC} = Max., V_{OUT} = GND		−350		−350	mA
I_{CCx16}	V_{CC} Operating Supply Current	V_{CC} = Max., I_{OUT} = 0 mA $\overline{CS}$, $\overline{UB}$, & $\overline{LB}$ = V_{IL}		550		330	mA
I_{CCx8}	V_{CC} Operating Supply Current	V_{CC} = Max., I_{OUT} = 0 mA $\overline{CS}$ = V_{IL}, $\overline{UB}$ or $\overline{LB}$ = V_{IL}		350		200	mA
I_{SB1}	Automatic $\overline{CS}$ Power-Down Current [2]	Max. V_{CC}, $\overline{CS}$ ≥ V_{IH}, Min. Duty Cycle = 100%		250		60	mA
I_{SB2}	Automatic $\overline{CS}$ Power-Down Current [2]	Max. V_{CC}, $\overline{CS}$ ≥ V_{CC} − 0.3V, V_{IN} ≥ V_{CC} − 0.3V or V_{IN} ≤ 0.3V		—		60	mA

Shaded area contains preliminary information.

Capacitance[3]

Parameters	Description	Test Conditions	Max.	Units
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 5.0V	35	pF
C_{OUT}	Output Capacitance		25	pF

Notes:

1. Not more than 1 output should be shorted at one time. Duration of the short circuit should not exceed 30 seconds.
2. A pull-up resistor to V_{CC} on the CE input is required to keep the device deselected during V_{CC} power-up, otherwise I_{SB} will exceed values given.
3. Tested on a sample basis.

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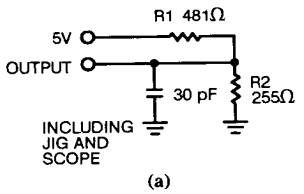
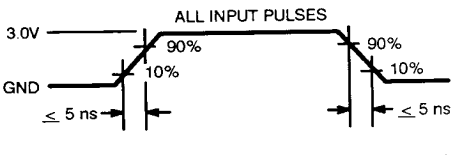
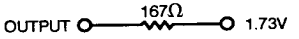
AC Test Loads and Waveforms





Equivalent to: THEVENIN EQUIVALENT



Switching Characteristics Over the Operating Range [4]

Parameters	Description	1610HD-12		1610HD-15		1610HD-20		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE								
t_{RC}	Read Cycle Time	12		15		20		ns
t_{AA}	Address to Data Valid		12		15		20	ns
t_{OHA}	Data Hold from Address Change	2		2		5		ns
t_{ACS}	$\overline{CS}$ LOW to Data Valid		12		15		20	ns
t_{DOE}	$\overline{OE}$ LOW to Data Valid		10		10		10	ns
t_{LZOE}	$\overline{OE}$ LOW to Low Z	3		2		3		ns
t_{HZOE}	$\overline{OE}$ HIGH to High Z		8		8		8	ns
t_{LZCS}	$\overline{CS}$ LOW to Low Z [6]	3		3		5		ns
t_{HZCS}	$\overline{CS}$ HIGH to High Z [5, 6]		8		8		8	ns
t_{PU}	$\overline{CS}$ LOW to Power-Up	0		0		0		ns
t_{PD}	$\overline{CS}$ HIGH to Power-Down		12		15		20	ns
WRITE CYCLE [7]								
t_{WC}	Write Cycle Time	12		15		20		ns
t_{SCS}	$\overline{CS}$ LOW to Write End	10		12		15		ns
t_{AW}	Address Set-Up to Write End	10		12		15		ns
t_{HA}	Address Hold from Write End	2		2		2		ns
t_{SA}	Address Set-Up to Write Start	0		0		2		ns
t_{PWE}	$\overline{WE}$ Pulse Width	10		12		15		ns
t_{SD}	Data Set-Up to Write End	10		10		10		ns
t_{HD}	Data Hold from Write End	2		2		2		ns
t_{LZWE}	$\overline{WE}$ HIGH to Low Z [6]	5		5		5		ns
t_{HZWE}	$\overline{WE}$ LOW to High Z [5, 6]	0	7	0	7	0	7	ns

Shaded area contains preliminary information.

Notes:

4. Test conditions assume signal transition times of 5 ns or less, timing reference levels of 1.5V, input levels of 0 to 3.0V and output loading of the specified I_{OL}/I_{OH} and 30-pF load capacitance.
5. t_{HZCS} and t_{HZWE} are specified with C_L = 5 pF as in part (b) of AC Test Loads. Transition is measured ±500 mV from steady state voltage.
6. At any given temperature and voltage condition, t_{HZCS} is less than t_{LZCS} for any given device. These parameters are guaranteed and not 100% tested.
7. The internal write time of the memory is defined by the overlap of $\overline{CS}$ LOW and $\overline{WE}$ LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.
8. $\overline{WE}$ is HIGH for read cycle.
9. Device is continuously selected, $\overline{CS}$ = V_{IL} and $\overline{OE}$ = V_{IL}.
10. Address valid prior to or coincident with $\overline{CS}$ transition low.
11. Data I/O will be high impedance if $\overline{OE}$ = V_{IH}.
12. If $\overline{CS}$ goes HIGH simultaneously with $\overline{WE}$ HIGH, the output remains in a high-impedance state.

Switching Characteristics Over the Operating Range (continued) [4]

Parameters	Description	1610HD-25		1610HD-35		1610HD-45		1610HD-50		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE										
t_{RC}	Read Cycle Time	25		35		45		50		ns
t_{AA}	Address to Data Valid		25		35		45		50	ns
t_{OHA}	Data Hold from Address Change	5		5		5		5		ns
t_{ACS}	$\overline{CS}$ LOW to Data Valid		25		35		45		50	ns
t_{DOE}	$\overline{OE}$ LOW to Data Valid		15		20		25		30	ns
t_{LZOE}	$\overline{OE}$ LOW to Low Z	5		5		5		5		ns
t_{HZOE}	$\overline{OE}$ HIGH to High Z		15		15		15		20	ns
t_{LZCS}	$\overline{CS}$ LOW to Low Z[6]	5		5		5		5		ns
t_{HZCS}	$\overline{CS}$ HIGH to High Z[5, 6]		10		15		15		20	ns
t_{PU}	$\overline{CS}$ LOW to Power-Up	0		0		0		0		ns
t_{PD}	$\overline{CS}$ HIGH to Power-Down		25		35		40		50	ns
WRITE CYCLE [7]										
t_{WC}	Write Cycle Time	25		35		45		50		ns
t_{SCS}	$\overline{CS}$ LOW to Write End	22		25		35		45		ns
t_{AW}	Address Set-Up to Write End	22		25		30		40		ns
t_{HA}	Address Hold from Write End	3		3		3		3		ns
t_{SA}	Address Set-Up to Write Start	4		4		4		4		ns
t_{PWE}	$\overline{WE}$ Pulse Width	18		25		30		30		ns
t_{SD}	Data Set-Up to Write End	13		15		15		20		ns
t_{HD}	Data Hold from Write End	3		5		5		5		ns
t_{LZWE}	$\overline{WE}$ HIGH to Low Z[6]	3		5		5		5		ns
t_{HZWE}	$\overline{WE}$ LOW to High Z[5, 6]	0	7	0	12	0	12	0	15	ns

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Data Retention Characteristics (L Version Only)

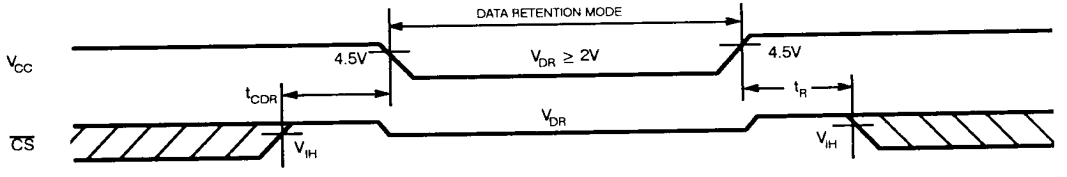
Parameter	Description	Test Conditions	CYM1610		Units
			Min.	Max.	
V_{DR}	V_{CC} for Retention Data	V_{CC} = 2.0V, $\overline{CS} \geq V_{CC} - 0.2V$ $V_{IN} \geq V_{CC} - 0.2V$ or $V_{IN} \leq 0.2V$	2.0		V
I_{CCDR}	Data Retention Current			4	mA
t_{CDR}[14]	Chip Deselect to Data Retention Time		0		ns
t_R[14]	Operation Recovery Time		t_{RC}[13]		ns
I_{LI}[14]	Input Leakage Current			8	µA

Notes:

13. t_{RC} = Read Cycle Time.

14. Guaranteed, not tested.

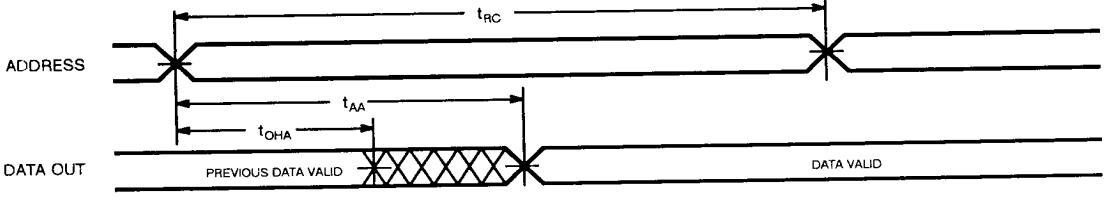
Data Retention Waveform



1610-7

Switching Waveforms[10]

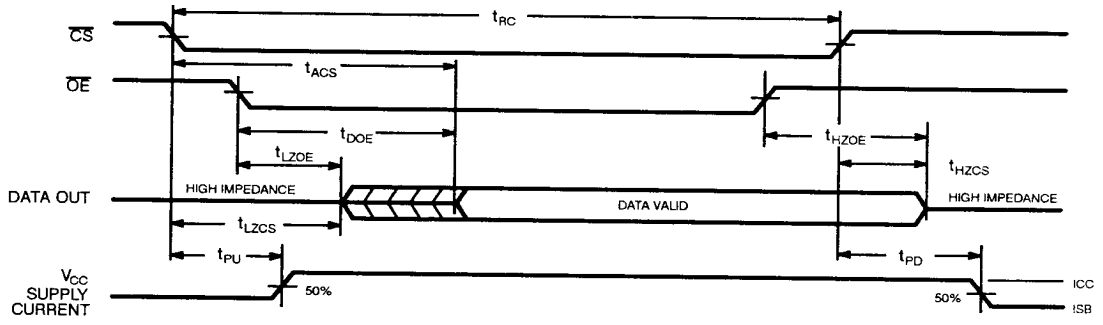
Read Cycle No. 1[7, 8]



1610-8

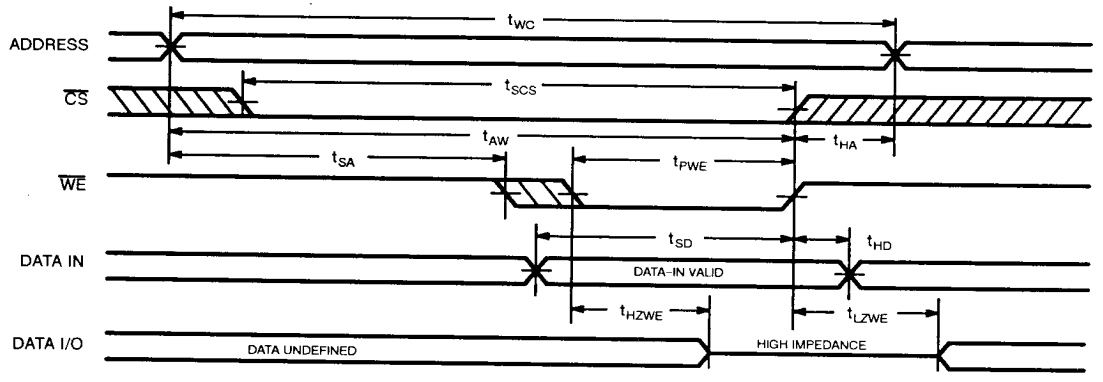
Switching Waveforms (continued)

Read Cycle No. 2[8, 10]



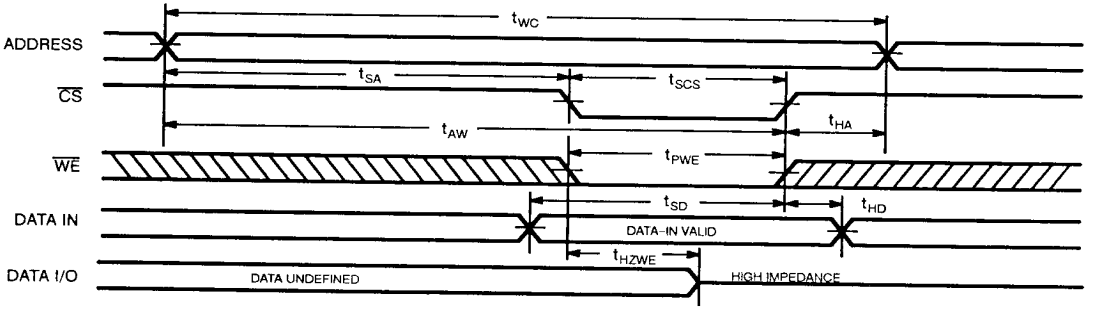
1610-9

Write Cycle No. 1 ($\overline{WE}$ Controlled)[7, 11]



1610-10

Write Cycle No. 2 ($\overline{CS}$ Controlled)[7, 11, 12]



1610-11

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Truth Table

$\overline{CS}$	$\overline{UB}$	$\overline{LB}$	$\overline{OE}$	$\overline{WE}$	Input/Outputs	Mode
H	X	X	X	X	High Z	Deselect/Power-Down
L	H	H	X	X	High Z	Deselect/Power-Down
L	L	L	L	H	Data Out_{0-15}	Read Word
L	H	L	L	H	Data Out_{0-7}	Read Lower Byte
L	L	H	L	H	Data Out_{8-15}	Read Upper Byte
L	L	L	X	L	Data In_{0-15}	Write Word
L	H	L	X	L	Data In_{0-7}	Write Lower Byte
L	L	H	X	L	Data In_{8-15}	Write Upper Byte
L	L	L	H	H	High Z	Deselect
L	H	L	H	H	High Z	Deselect
L	L	H	H	H	High Z	Deselect

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Ordering Information

Speed	Ordering Code	Package Type	Operating Range
12	CYM1610HD-12C	HD01	Commercial
15	CYM1610HD-15C	HD01	Commercial
	CYM1610HD-15MB	HD01	Military
20	CYM1610HD-20C	HD01	Commercial
	CYM1610LHD-20C	HD01	
	CYM1610HD-20MB	HD01	Military
25	CYM1610HD-25C	HD01	Commercial
	CYM1610LHD-25C	HD01	
	CYM1610HD-25MB	HD01	Military
	CYM1610LHD-25MB	HD01	
35	CYM1610HD-35C	HD01	Commercial
	CYM1610LHD-35C	HD01	
	CYM1610HD-35MB	HD01	Military
	CYM1610LHD-35MB	HD01	
45	CYM1610HD-45C	HD01	Commercial
	CYM1610LHD-45C	HD01	
	CYM1610HD-45MB	HD01	Military
	CYM1610LHD-45MB	HD01	
50	CYM1610HD-50C	HD01	Commercial
	CYM1610LHD-50C	HD01	
	CYM1610HD-50MB	HD01	Military
	CYM1610LHD-50MB	HD01	

Shaded area contains preliminary information.