Supertex inc.

ED−5
ED−9
ED−11
ED−15

Programmable Encoder / Decoder
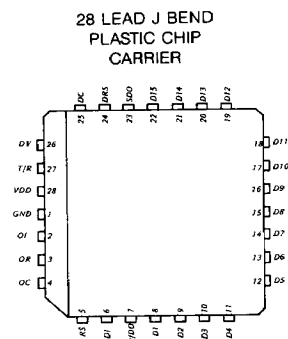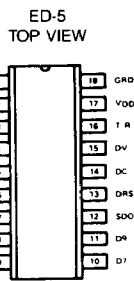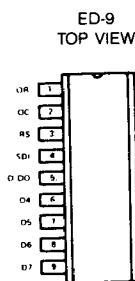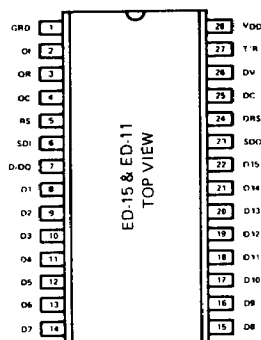
FEATURES

- Manchester Phase Encoding
- Encoder/Decoder in one circuit
- Schmidt Trigger Input for excellent noise rejection
- Built-in Oscillator using non-critical RC components
- Zener Diode to regulate the power supply
- Low Power, High Noise Immunity CMOS technology
- Ability to Decode Original Signals
- Automatic Preamble Generation

GENERAL DESCRIPTION

The ED series is a single monolithic chip using metal-gate CMOS technology for low cost, low power, high yield and high reliability. It is a dual purpose circuit, capable of working either as an encoder or as a decoder on its own transmissions in applications where exclusive recognition of a special code is required. It will decode 1 of 32,768 codes. In the transmit mode each circuit is capable of generating the possible codes by connecting the Data Inputs to VDD or GRD for a "1" or a "0". In the receive mode each circuit is capable of decoding the transmitted signal and simultaneously making a comparision to the local address code for identification.

ORDERING INFORMATION

DEVICE	PACKAGE	ORDER NO
ED-15	28-Pin Plastic DIP	ED-15P
	28-Pin Plastic Chip Carrier	ED-15PC
ED-11	28-Pin Plastic DIP	ED-11P
ED-9	18-Pin Plastic DIP	ED-9P
ED-5	18-Pin Plastic DIP	ED-5P

TYPICAL APPLICATIONS

- Smoke & Fire Alarm Control Systems
- Security Systems
- Theft Alarm Systems
- Digital Locks
- Digital Paging Systems
- Garage Door Openers
- Systems that require a Special Identification Code
- Pocket Pagers
- Recognition or Transmission

PIN CONFIGURATION

ABSOLUTE MAXIMUM RATINGS

Supply Voltage with respect to VSS 6.4V

Operating Temperature . . . . 0°C to +70°C

Storage Temperature . . . . −55°C to +150°C

Zener Current 100mA

NOTE: All Inputs except OI contain protection circuitry to prevent damage due to static charges. Care should be exercised to prevent application of voltages outside of the specification range. The OI has a special input protection circuit and special care should be taken with this input.

DC (STATIC) CHARACTERISTICS (V_{DD} = 5.0V ± 5%; GRD = 0.0V; T_A = 25°C)

SYMBOL	PARAMETER	MIN.	TYP (note 1)	MAX.	UNIT	CONDITION
VIH	Input High Voltage	V_{DD} −0.3		V_{DD} +0.3	V	"1" INPUT
VIL	Input Low Voltage	−0.3		0.3	V	"0" INPUT
ILKC	Input Leakage Current		0.1	2.0	μA	V_{IN} = 5.0V for pins T/R, SDI
ILC	Input Load Current	2.0	6.0	20.0	μA	V_{IN} = 5.0V for pins RS, D1−D15
VOH	Output High Voltage	V_{DD} −0.3			V	V_{DD} = 4.75V; I_{LOAD} = −100 μA
VOL	Output Low Voltage			0.3	V	V_{DD} = 4.75V; I_{LOAD} = 100 μA
IOH	Output High Current (Sourcing)	−1.0	−1.5		mA	V_{OH} = V_{DD} −1.0V
IOL	Output Low Current (Sinking)	1.0	3.0		mA	V_{OL} = 1.0V
VZ	Zener Voltage	5.5	6.4	7.0	V	I_Z = 10 μA (note 2)
		6.0	6.7	7.5	V	I_Z = 10 mA (note 2)
CIN	Input Capacitance			10	pfd	(note 2)
CONT	Output Capacitance			10	pfd	(note 2)
IDD	Drain Current			10	μA	V_{DD} = 5.0V; all inputs = GRD all ouputs floating

AC CHARACTERISTICS (V_{DD} = 5.0V ±5%; T_A = 25°C)

SYMBOL	PARAMETER	MIN	TYP (note 1)	MAX	UNIT	CONDITIONS
f_c	Clock Frequency	0		25	KHz	R = 150K; C = 100pF; Clock Period (t_c) = $\frac{1}{f_c}$
tSDI	Start Pulse Width	500			ns	
tDDO	DDO Delay from SDI		5		us	
tDC	Data Clock Pulse Width		.5t_c		sec	
tWORD	Full Cycle Word Length		130t_c		sec	
RR	Receiver Oscillator Resistor Tolerance from Transmitter Oscillator Resistor		±10		%	
CR	Receiver Oscillator Capacitor Tolerance from Transmitter Oscillator Capacitor		±10		%	

NOTES: 1. Typical values are those values measured in a production sample at V_{CC} = 5.0V.

2. This parameter is periodically sampled and is not 100% tested.

OPERATION

General

The ED-15 series mode of operation is controlled by the Transmit/Receive control input (T/R), when switched from VDD to GND, the circuit will automatically change the oscillator, Start/Data Input, and Data/Decode Output from Transmit to Receive mode.

The circuit contains an on-chip zener diode to clamp the power supply to around 6.7 volts. The circuit will operate from 4.0 volts to the zener voltage, but operation is recommended at 5 volts ± 5% in order to stabilize the time constants of the oscillator circuit. In order to use the on-chip zener diode, a current limiting resistor of 1K ohm or greater is required. If pull up resistors are used for the D_1-D_{15} drivers, the resistors should be tied to a voltage no higher than that on Pin 28 or 6 volts, whichever is lower.

Output drivers are capable of sinking or sourcing 1.0mA minimum at 1.0 volts VDS. All inputs are gate protected to both power supplies by internal diodes. The Data Inputs each have pull down resistors to ground so that only a "1" will have to be programmed. This allows the inputs to be programmed by using SPST switches or jumpers to VDD only. The Transmit/Receive input does not have a pull up or pull down resistor. The Start/Data Input also does not have a pull up or pull down resistor, but is applied to a Schmidt Trigger Input circuit to improve noise rejection.

BLOCK DIAGRAMS
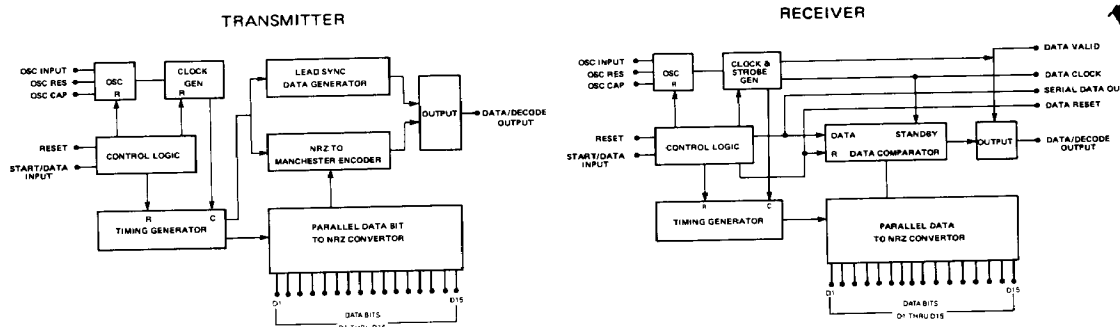
Encoder Function

This function is selected by connecting the Transmit/Receive control input to VDD. This enables the Transmit mode and the circuit will function as an encoder— sampling the 15 Data Input pins digital information and encoding this parallel data in NRZ format, combining it with the clock in Manchester Code (Phase Encoded) and presented to the D/DO pin for transmission. (Usually to another ED device used as the decoder circuit). The encoder will transmit the serial data each time the Start/Data input is activated.

This encoded Data word is transmitted in 2 parts. The first part is the preamble information which is a series of 12 "1"'s then a space indicating that the encoded Data is to follow. This preamble information is intended to be used to synchronize a phase locked loop at the receiver or used as a settling time for receivers that have automatic gain control. The second part contains the 15 bits of addresses and/or controls.

Decoder Function

The receive mode is selected by connecting the Transmit/Receive control input to ground. In this mode the circuit will work as a decoder, receiving the serial data in Manchester Coded format and recover the clock. The incoming data is converted to a 15-bit serial word. Compare it with the local data word by sampling the Data Inputs (15-bits). These bits are usually programmed to the expected Data that will be decoded. If the two data words match, the decoded output will become logic "1" state, but if the two words do not match the decoded output will stay low. Also if the words do not match but the bit stream was valid (i.e. 15-bits of proper timing) then only the output valid signal will go high. If at any time the bit sequence has the wrong timing, the local oscillator and internal comparison circuits will be reset and any new input pulses will be recognized as a new bit stream. Therefore, as with the receiver processing of the preamble information, the 12 bits will be recognized but during the 13th interval where no bit transition occurs, the circuit times—out and awaits the start bit of the data sequence.

ED-11 Option

The ED-11 differs from the ED-15 in that in the receive mode the ED-11 will only compare the first 11 bits and ignore the state of the last 4 bits — that is 2048 distinct address codes with 4 bits of that may be used for control data transmission.

ED-9 Option

The ED-9 is essentially an 18-pin packaging of the ED-15 die. The operation and function of this circuit is the same as the ED-15; the only difference being in the available pins. In the transmit mode the circuit is only capable of encoding 9 bits of data, the other 6 bits are not programmable and remain zero's. The pin configuration also drops DV, DC, DRS, and SDO such that the circuit can now only respond to a data match condition on the only output D/DO. In the receive mode the circuit can decode the same 9 bits of data, enabling up to 512 possible addresses.

ED-5 Option

The 18 pin packaging option of the ED-11 die is called the ED-5. In the transmit mode it is only capable of 5 bits of programmable code. All the other bits are held at zero. But in the receive mode, the circuit has the five (32) unlock code bits plus the last four transparent bits of the ED-11. The ED-5 also supplies the necessary output signals to process the 4 bits of control data.

PIN DEFINITION

LABEL	PIN NAME	FUNCTION
GND	Ground	Supply Potential negative side.
OI	Oscillator Input	This input is to drive the oscillator and is the tie point of the timing resistor (R_T), and the timing capacitor (C_T). It also is connected through a diode to an open drain P-channel device that turns on to V_{DD} when the oscillator is being reset. This input can exceed the power supplies and does during normal oscillator operation.
OR	Oscillator Resistor	Provides phase feedback to the RC timing circuit through the connected timing resistor. Note this pin is driven high during oscillator reset.
OC	Oscillator Capacitor	Capacitor connection of RC timing circuit provides phased feedback from the oscillator. This pin is driven low during oscillator reset.
RS	Reset Input	This input pin may be used to override the data transmission cycle or inhibiting a SDI input. It clears the D/DO to a low state and resets the internal oscillator and data comparison circuits. This pin may be left open (No Connection) when not used, or driven as an input, or an external capacitor (100pf) to VDD may be added for power-up reset. The Reset function is activated when this input is connected to VDD.
S/DI	Start/Data Input	Start/Data input is a dual function pin. It is used to start the oscillator which enables the transmission of the encoded word in the transmit mode. And in the receive mode, this input receives the serial coded information for processing and comparision.
D/DO	Data/Decode Output	Another dual purpose pin, this pin is the encoded sequence data output in the transmit mode and becomes the decode true output in the receive mode. It indicates that the incoming code has matched the local bit data input address.
D1 - D15	Data Bit Inputs	These inputs provide parallel input data to be sequentially transmitted. 18 pin package options have some pins omitted and hence these data positions will have logical zeros transmitted. In the receive mode these inputs become the parallel local address code for comparison with the incoming data. Note that with the ED-11 and ED-5 options, the data bits 11-15 are not used in the comparison when in the receive mode.
SDO	Serial Data Output	This output signal is a buffered S/DI signal after going through the input Schmidt Trigger — a delay circuit, and is the same polarity as the input and can be used to chain a number of receivers together. This output can be connected to the input of a 16 bit shift register (clocked by the DC pin) in a receiver system where data is to be recovered regardless of its comparison to a pre-set address word.
DRS	Data Reset Output	Data Reset can be used in the receive mode to reset an external data shift register since this signal pulse indicates that a new word has just begun processing.
DC	Data Clock Output	The Data Clock output may be used in a receive system since it is the recovered data sync pulses, also this output can be used to clock an external shift register where data is to be recovered.
DV	Data Valid Output	This output is triggered low at the start of any input and will remain low until a complete word has been processed. Note that this output simply signals that a valid word has been received and not that the code received has matched the local address code.
T/R	Transmit/ Receive	This is a control input to determine the operating mode. A logic high applied to this input puts it in the transmit mode, a logic low puts it in the receive mode.
VDD	VDD	Positive Supply Potential — This circuit contains an on-chip zener of approximately 6.7 volts across the supply terminals.

TRANSMIT AND RECEIVE DATA PATTERNS OF ED-SERIES DEVICES
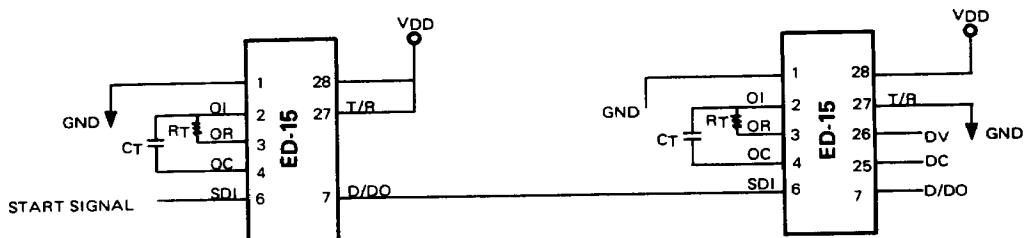
NOTE: Bit Sequence Code Format

X = Programmable
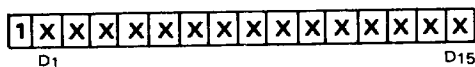
0 = Hardwired Internally Zero

1 = Hardwired Internally One
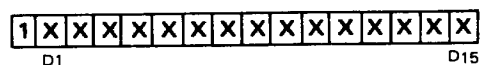
D = Don't Care in Receive Mode
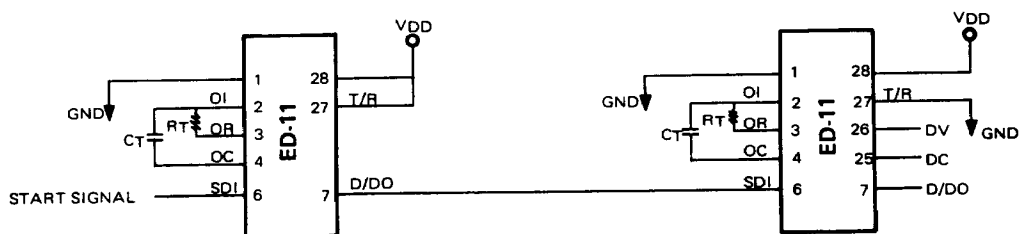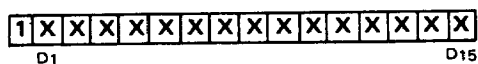
ED-15 to ED-15

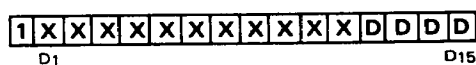### Transmitted Bit Sequence

Received Address Code

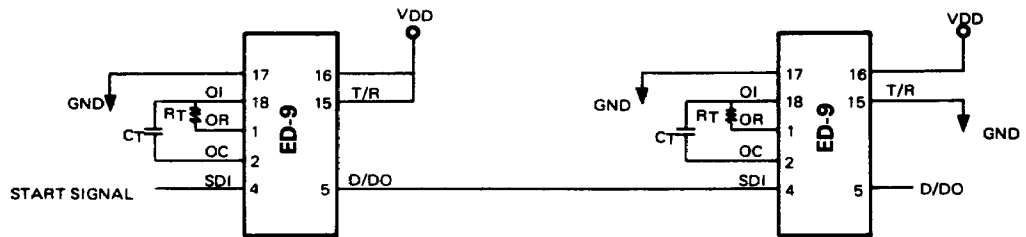## ED-11 to ED-11

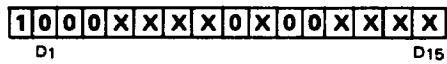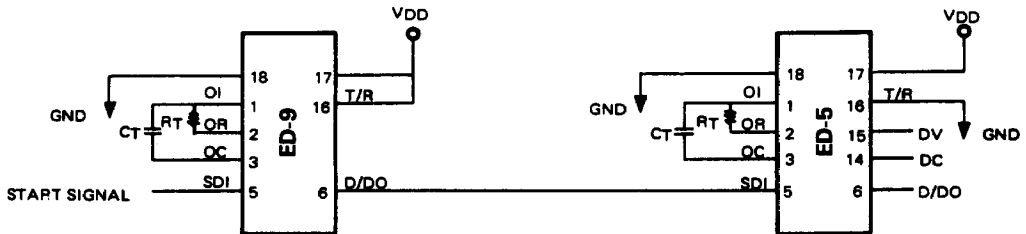### Transmitted Bit Sequence

Received Address Code

Note: When unused, the DV, DC, DRS and SDO pins should be left floating and **must not** be tied to either a power supply or to ground.
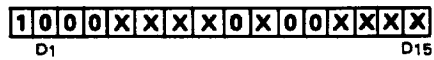
4-5

ED-9 to ED-9

Transmitted Bit Sequence

| 1 | 0 | 0 | 0 | X | X | X | X | 0 | X | 0 | 0 | X | X | X | X |

D1   D15

Received Address Code

| 1 | 0 | 0 | 0 | X | X | X | X | 0 | X | 0 | 0 | X | X | X | X |

D1   D15

ED-9 to ED-5

Transmitted Bit Sequence

| 1 | 0 | 0 | 0 | X | X | X | X | 0 | X | 0 | 0 | X | X | X |

D1   D15

Received Address Code

| 1 | 0 | 0 | 0 | X | X | X | 0 | X | 0 | 0 | D | D | D |

D1   D15

TIMING DIAGRAM – TRANSMIT MODE

TRIGGER IN

SDI

SDO

DATA RESET

DRS

DATA OUT

DDO

PREAMBLE BURST

DATA

INPUT BITS D$_1$ – D$_{15}$

T_{MIN} = 500ns
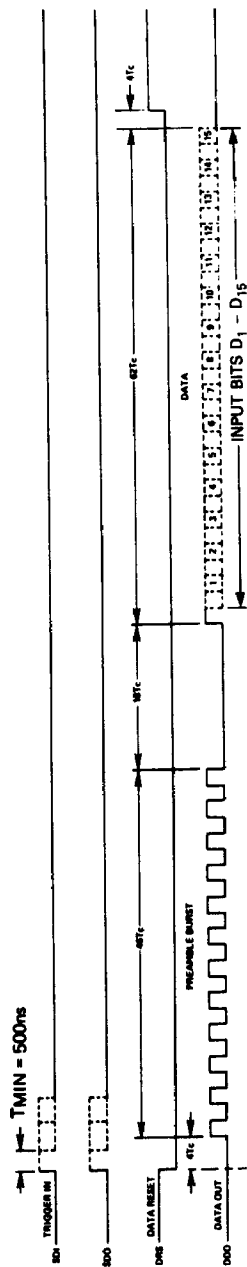
Total Time Required for Transmission of One Sequence = (DRS – 4Tc) = 130Tc

$$T_c = \frac{1}{\text{CLOCK FREQUENCY}}$$

TIMING DIAGRAM – RECEIVE MODE

DATA VALID

DV

DECODE OUTPUT

DDO

SERIAL DATA INPUT

SDI

DATA CLOCK

OC

DRS

SYNCHRONIZATION BURST

DATA

INPUT BITS D$_1$ – D$_{15}$

Goes hi if received Address compares to local data pattern

Stays low if Address does not compare
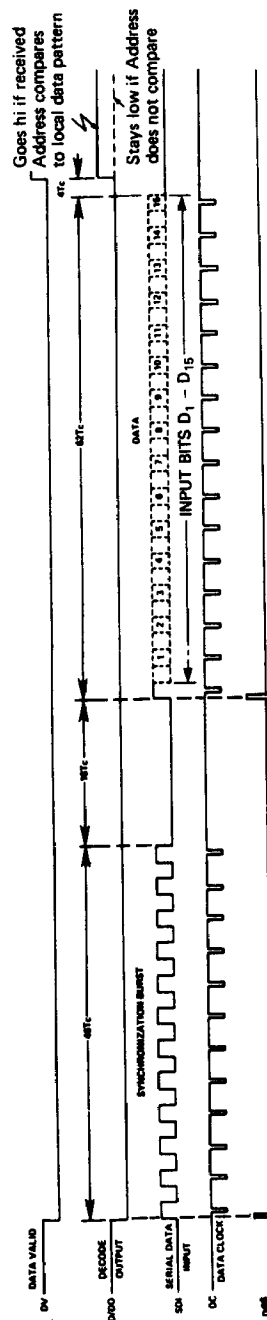
$$T_c = \frac{1}{\text{CLOCK FREQUENCY}}$$

TYPICAL PERFORMANCE CURVES (TA = 25°C unless otherwise noted)

I_{OL} vs V_{DD} vs V_{OL}
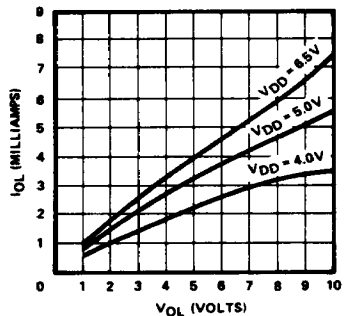
I_{OH} vs V_{DD} vs V_{OH}
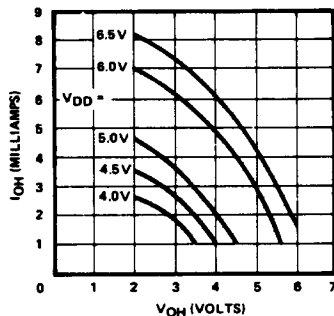
RESISTANCE vs OSCILLATOR FREQUENCY
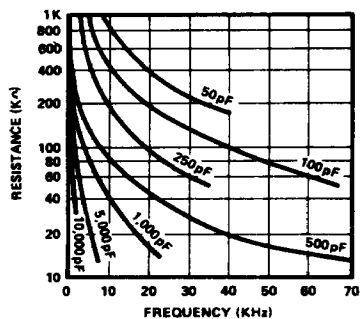
OPERATING FREQUENCY vs V_{DD}
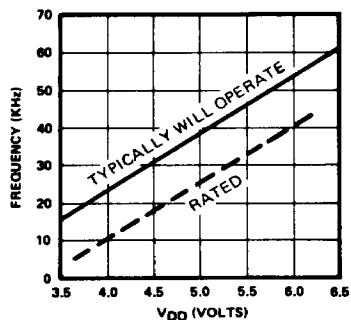
SDI INPUT V_{IL}/V_{IH} vs V_{DD}

I_{DD} vs V_{DD}

4-8