Integra™ L64754 ISDB-S DVB/DSS Satellite Receiver

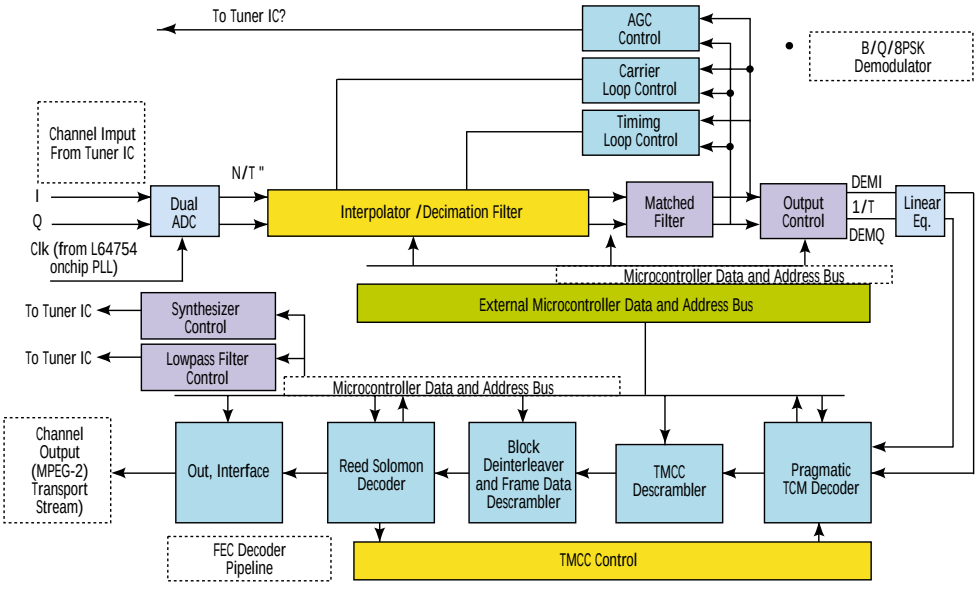
OVERVIEW

The L64754 is a satellite receiver demodulator designed specifically to meet the needs of Japanese satellite broadcast digital TV. Providing maximum integration and flexibility for system designers at a minimum cost, the L64754 chip reduces the number of external components required to build a system. LSI Logic fabricates the L64754 using its G12, 1.8 core/3.3 volt I/O, 0. I 8-micron, HCMOS process technology.

The L64754 demodulator interfaces with any tuner IC, which directly down-converts satellite signal from L-band to baseband, and includes an on-chip synthesizer controller. The L64754 generates control signals for a tuner IC synthesizer (using frequency information programmed into the L64754 configuration registers), and generates dual AGC control voltages for the two-stage automatic gain control on a tuner IC chip.

The L64754 satellite demodulator contains two main blocks: a BPSK/QPSK/8PSK demodulator and a concatenated FEC decoder.

The B/Q/8PSK demodulator performs demodulation for any of the three modulation formats, a method of extracting a digital signal from a phase-modulated analog signal. The B/Q/8PSK module is designed specifically for a satellite broadcast digital TV receiver, and is compliant with the Japanese ISDB-S standard. The demodulator works as per the European digital video broadcast (DVB-S) standard and the technical specifications for DSS systems.



Integra™ L64754 Block Diagram

FEATURES

- On-chip dual differential 6-bit A/D converters
- Variable data rate of 1 to 45 Mbaud
- Serial host interface compatible with the LSI Logic serial control bus interface
- Correction for Quadrature phase, amplitude imbalance
- Integrated PLL for clock synthesis for use of fundamental mode crystal
- Fast channel-switching mode
- Anti-aliasing filters
- On-chip digital clock synchronization
- Programmable matched filter
- Synthesizer control-programmable counters
- Power estimation for AGC control-dual AGC outputs to allow two-stage AGC
- On-chip C/N, BER estimators
- Bit-error monitoring for channel performance measurements for all possible ISDB-S/DVB/DSS rates
- On-chip block de-interleaver
- Power-down and Standby modes
- On-chip controller frees host processor

LSI LOGIC®

The Communications Company™

Integra™ L64754 ISDB-S, DVB/DSS Satellite Receiver

The Forward Error Correction (FEC) decoder pipeline is a complete FEC concatenated decoder utilizing a TCM inner code in ISDB-S mode and Viterbi inner code in DVB/DSS mode with Reed-Solomon outer code. The FEC decoding pipeline contains necessary synchronizations-de-interleaving and scrambling functions-for a complete decoding solution.

ISDB-S MODE:

- B/Q/8PSK demodulation for 28.86 Mbaud
- TMCC based synchronization
- Frame synchronization with input frequency error of less than +/- 720KHz for fast carrier acquisition
- Programmable frame and super frame synchronization, enabling fast and reliable frame acquisition
- On-chip digital carrier synchronization featuring AFC for coarse acquisition and frequency sweep for fine acquisition
- Pragmatic TCM decoder module for rates 1/2, 2/3, 3/4, 5/6, and 7/8
- (204/188), (64/48) Reed-Solomon decoder
- Mask control option for choice of transmission layers (i.e., supports “graceful degradation”, under severe environmental conditions)
- On-chip transport stream divider allowing user selection of one-of-eight (or all) interleaved TS streams
- Output PCR jitter less than IOOns

DVB/DSS MODE SUPPORTS:

- DVB and DSS system specifications
- Synchronous Parallel Interface protocol for FEC data output

REFERENCE DESIGN BOARD

To accelerate development of set-top box solutions, the L64754 is available with a developer’s kit that allows manufacturers to select the best option for their target market and application requirements. The kit provides the hardware and software components to shorten development cycles and to ensure fast time-to-market.

The reference design board consists of a complete evaluation board with a PC interface and MPEG-2 transport output. Software to enable system resting and code optimization is included, along with a manual that provides test and evaluation information and PC board layout. Complete micro code for the L64754’s micro controller is included, with the option of customizing the micro code.

For more information please call:

LSI Logic Corporation
North American Headquarters
Milpitas, CA
Tel: 866 574 5741

LSI Logic Europe Ltd.
European Headquarters
United Kingdom
Tel: 44 1344 426544
Fax: 44 1344 481039

LSI Logic KK Headquarters
Tokyo, Japan
Tel: 81 3 5463 7165
Fax 81 3 5463 7820

LSI: Logic web site:
www.lsilogic.com

Order No. I20096
1201.1k.JG.IK - Printed in USA

LSI LOGIC®

The Communications Company™