

PE3239

Product Description

Peregrine's PE3239 is a high performance integer-N PLL capable of frequency synthesis up to 2.2 GHz. The superior phase noise performance of the PE3239 is ideal for applications such as wireless local loop basestations, LMDS systems and other demanding terrestrial systems.

The PE3239 features a 10/11 dual modulus prescaler, counters, phase detector and a charge pump as shown in Figure 1. Counter values are programmable through a three wire serial interface.

Fabricated in Peregrine's patented UTSi® (Ultra Thin Silicon) CMOS technology, the PE3239 offers excellent RF performance with the economy and integration of conventional CMOS.

2.2 GHz Integer-N PLL for Low Phase Noise Applications

Features

- 2.2 GHz operation
- 10/11 prescaler
- Internal phase detector with charge pump
- Serial programmable
- Low power — 20 mA at 3 V
- Ultra-low phase noise
- Available in 20-lead TSSOP

Figure 1. Block Diagram

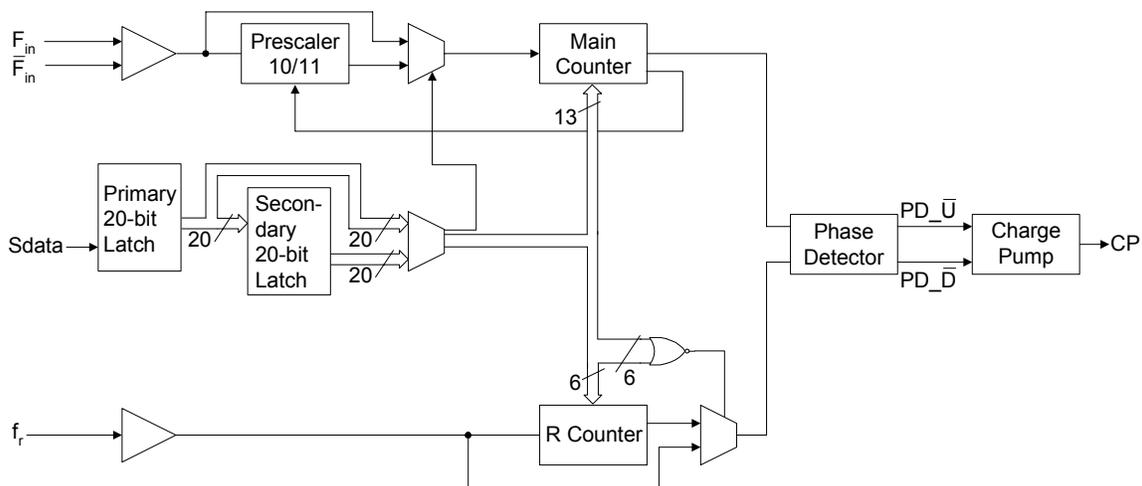
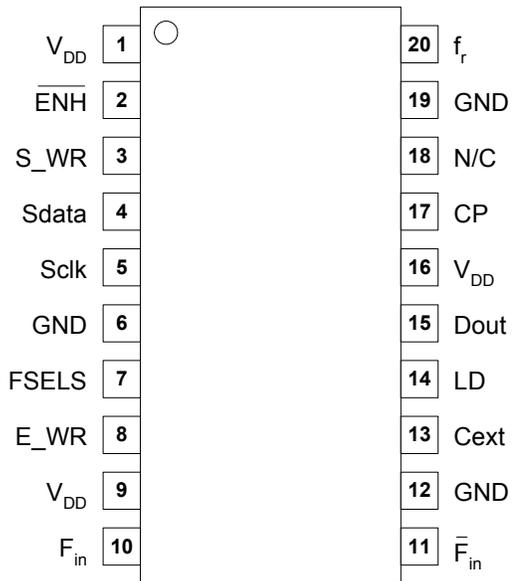


Figure 2. Pin Configuration

Table 1. Pin Descriptions

Pin No.	Pin Name	Type	Description
1	V _{DD}	(Note 1)	Power supply input. Input may range from 2.85 V to 3.15 V. Bypassing required.
2	ENH	Input	Enhancement mode. When asserted low (“0”), enhancement register bits are functional. Internal 70 kΩ pull-up resistor.
3	S _{WR}	Input	Serial load enable input. While S _{WR} is “low”, Sdata can be serially clocked. Primary register data are transferred to the secondary register on S _{WR} rising edge.
4	Sdata	Input	Binary serial data input. Input data entered MSB first.
5	Sclk	Input	Serial clock input. Sdata is clocked serially into the 20-bit primary register (E _{WR} “low”) or the 8-bit enhancement register (E _{WR} “high”) on the rising edge of Sclk.
6	GND		Ground.
7	FSELS	Input	Selects contents of primary register (FSELS=1) or secondary register (FSELS=0) for programming of internal counters. Internal 70 kΩ pull-down resistor.
8	E _{WR}	Input	Enhancement register write enable. While E _{WR} is “high”, Sdata can be serially clocked into the enhancement register on the rising edge of Sclk. Internal 70 kΩ pull-down resistor.
9	V _{DD}	(Note 1)	Same as pin 1.
10	F _{in}	Input	Prescaler input from the VCO. Max frequency input is 2.2 GHz.
11	F _{in}	Input	Prescaler complementary input. A bypass capacitor should be placed as close as possible to this pin and be connected in series with a 50 Ω resistor to the ground plane.
12	GND		Ground.
13	Cext	Output	Logical “NAND” of PD _U and PD _D terminated through an on chip, 2 kΩ series resistor. Connecting Cext to an external capacitor will low pass filter the input to the inverting amplifier used for driving LD.
14	LD	Output	Lock detect is an open drain logical inversion of CEXT. When the loop is in lock, LD is high impedance, otherwise LD is a logic low (“0”).
15	Dout	Output	Data out function, Dout, enabled in enhancement mode.
16	V _{DD}	(Note 1)	Same as pin 1.

Pin No.	Pin Name	Type	Description
17	CP	Output	Charge pump current is sourced when f_c leads f_p and sinked when f_c lags f_p .
18	NC	Output	No connection.
19	GND		Ground.
20	f_r	Input	Reference frequency input.

Note 1: V_{DD} pins 1, 9, and 16 are connected by diodes and must be supplied with the same positive voltage level.

Table 2. Absolute Maximum Ratings

Symbol	Parameter/Conditions	Min	Max	Units
V_{DD}	Supply voltage	-0.3	4.0	V
V_i	Voltage on any input	-0.3	$V_{DD} + 0.3$	V
I_i	DC into any input	-10	+10	mA
I_o	DC into any output	-10	+10	mA
T_{stg}	Storage temperature range	-65	150	°C

Table 3. Operating Ratings

Symbol	Parameter/Conditions	Min	Max	Units
V_{DD}	Supply voltage	2.85	3.15	V
T_A	Operating ambient temperature range	-40	85	°C

Table 4. ESD Ratings

Symbol	Parameter/Conditions	Level	Units
V_{ESD}	ESD voltage human body model (Note 1)	1000	V

Note 1: Periodically sampled, not 100% tested. Tested per MIL-STD-883, M3015 C2

Electrostatic Discharge (ESD) Precautions

When handling this UTSi device, observe the same precautions that you would use with other ESD-sensitive devices. Although this device contains circuitry to protect it from damage due to ESD, precautions should be taken to avoid exceeding the rating specified in Table 4.

Latch-Up Avoidance

Unlike conventional CMOS devices, UTSi CMOS devices are immune to latch-up.

Table 5. DC Characteristics
 $V_{DD} = 3.0\text{ V}$, $-40^\circ\text{ C} < T_A < 85^\circ\text{ C}$, unless otherwise specified

Symbol	Parameter	Conditions	Min	Typ	Max	Units
I_{DD}	Operational supply current; Prescaler enabled	$V_{DD} = 2.85\text{ to }3.15\text{ V}$		20	26	mA
Digital Inputs: S_WR, Sdata, Sclk						
V_{IH}	High level input voltage	$V_{DD} = 2.85\text{ to }3.15\text{ V}$	$0.7 \times V_{DD}$			V
V_{IL}	Low level input voltage	$V_{DD} = 2.85\text{ to }3.15\text{ V}$			$0.3 \times V_{DD}$	V
I_{IH}	High level input current	$V_{IH} = V_{DD} = 3.15\text{ V}$			+1	μA
I_{IL}	Low level input current	$V_{IL} = 0, V_{DD} = 3.15\text{ V}$	-1			μA
Digital Inputs: $\overline{\text{Enh}}$ (contains a 70 k Ω pull-up resistor)						
V_{IH}	High level input voltage	$V_{DD} = 2.85\text{ to }3.15\text{ V}$	$0.7 \times V_{DD}$			V
V_{IL}	Low level input voltage	$V_{DD} = 2.85\text{ to }3.15\text{ V}$			$0.3 \times V_{DD}$	V
I_{IH}	High level input current	$V_{IH} = V_{DD} = 3.15\text{ V}$			+1	μA
I_{IL}	Low level input current	$V_{IL} = 0, V_{DD} = 3.15\text{ V}$	-100			μA
Digital Inputs: FSELS, E_WR (contains a 70 k Ω pull-down resistor)						
V_{IH}	High level input voltage	$V_{DD} = 2.85\text{ to }3.15\text{ V}$	$0.7 \times V_{DD}$			V
V_{IL}	Low level input voltage	$V_{DD} = 2.85\text{ to }3.15\text{ V}$			$0.3 \times V_{DD}$	V
I_{IH}	High level input current	$V_{IH} = V_{DD} = 3.15\text{ V}$			+100	μA
I_{IL}	Low level input current	$V_{IL} = 0, V_{DD} = 3.15\text{ V}$	-1			μA
Reference Divider input: f_r						
I_{IHR}	High level input current	$V_{IH} = V_{DD} = 3.15\text{ V}$			+100	μA
I_{ILR}	Low level input current	$V_{IL} = 0, V_{DD} = 3.15\text{ V}$	-100			μA
Counter output: Dout						
V_{OLD}	Output voltage LOW	$I_{out} = 6\text{ mA}$			0.4	V
V_{OHD}	Output voltage HIGH	$I_{out} = -3\text{ mA}$	$V_{DD} - 0.4$			V
Lock detect outputs: (Cext, LD)						
V_{OLC}	Output voltage LOW, Cext	$I_{out} = 0.1\text{ mA}$			0.4	V
V_{OHC}	Output voltage HIGH, Cext	$I_{out} = -0.1\text{ mA}$	$V_{DD} - 0.4$			V
V_{OLLD}	Output voltage LOW, LD	$I_{out} = 1\text{ mA}$			0.4	V
Charge Pump output: CP						
$I_{CP} - \text{Source}$	Drive current	$V_{CP} = V_{DD} / 2$	-2.6	-2	-1.4	mA
$I_{CP} - \text{Sink}$	Drive current	$V_{CP} = V_{DD} / 2$	1.4	2	2.6	mA
I_{CPL}	Leakage current	$1.0\text{ V} < V_{CP} < V_{DD} - 1.0\text{ V}$	-1		1	μA
$I_{CP} - \text{Source}$ vs. $I_{CP} - \text{Sink}$	Sink vs. source mismatch	$V_{CP} = V_{DD} / 2, T_A = 25^\circ\text{ C}$			15	%
$I_{CP} \text{ vs. } V_{CP}$	Output current magnitude variation vs. voltage	$1.0\text{ V} < V_{CP} < V_{DD} - 1.0\text{ V}$ $T_A = 25^\circ\text{ C}$			15	%

Table 6. AC Characteristics

$V_{DD} = 3.0\text{ V}$, $-40^{\circ}\text{ C} < T_A < 85^{\circ}\text{ C}$, unless otherwise specified

Symbol	Parameter	Conditions	Min	Max	Units
Control Interface and Latches (see Figures 5, 6, 7)					
f_{Clk}	Serial data clock frequency	(Note 1)		10	MHz
t_{ClkH}	Serial clock HIGH time		30		ns
t_{ClkL}	Serial clock LOW time		30		ns
t_{DSU}	Sdata set-up time to Sclk rising edge		10		ns
t_{DHLd}	Sdata hold time after Sclk rising edge		10		ns
t_{PW}	S_WR pulse width		30		ns
t_{CWR}	Sclk rising edge to S_WR rising edge		30		ns
t_{CE}	Sclk falling edge to E_WR transition		30		ns
t_{WRC}	S_WR falling edge to Sclk rising edge		30		ns
t_{EC}	E_WR transition to Sclk rising edge		30		ns
Main Divider (Including Prescaler)					
F_{in}	Operating frequency		200	2200	MHz
P_{Fin}	Input level range	External AC coupling	-5	5	dBm
Main Divider (Prescaler Bypassed)					
F_{in}	Operating frequency		20	220	MHz
P_{Fin}	Input level range	External AC coupling	-5	5	dBm
Reference Divider					
f_r	Operating frequency	(Note 3)		100	MHz
P_{fr}	Reference input power (Note 2)	Single ended input	-2		dBm
Phase Detector					
f_c	Comparison frequency	(Note 3)		20	MHz

- Note 1:** fclk is verified during the functional pattern test. Serial programming sections of the functional pattern are clocked at 10 MHz to verify fclk specification.
- Note 2:** CMOS logic levels can be used to drive reference input if DC coupled. Voltage input needs to be a minimum of 0.5 Vp-p. For optimum phase noise performance, the reference input falling edge rate should be faster than 80mV/ns.
- Note 3:** Parameter is guaranteed through characterization only and is not tested.

Typical Performance Data ($V_{DD} = 3.00V$, $T_A = 25^\circ C$)

Figure 3. Typical RF Input Sensitivity

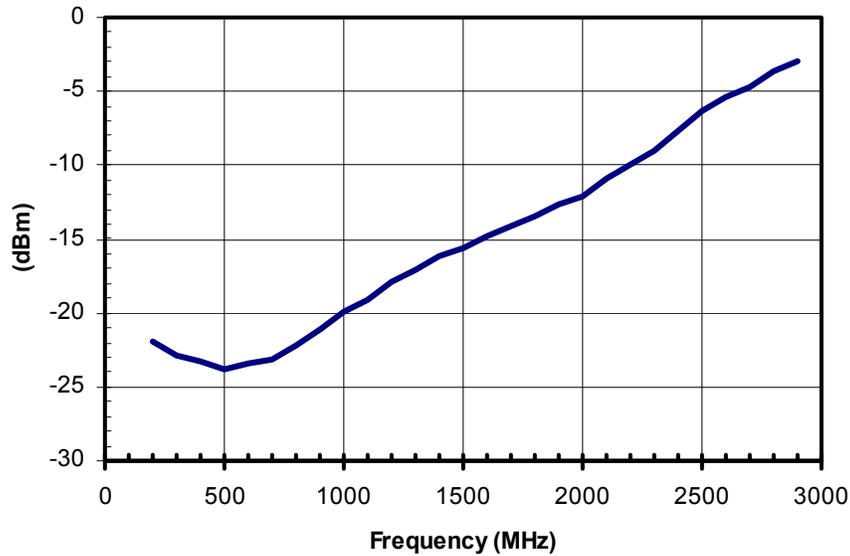
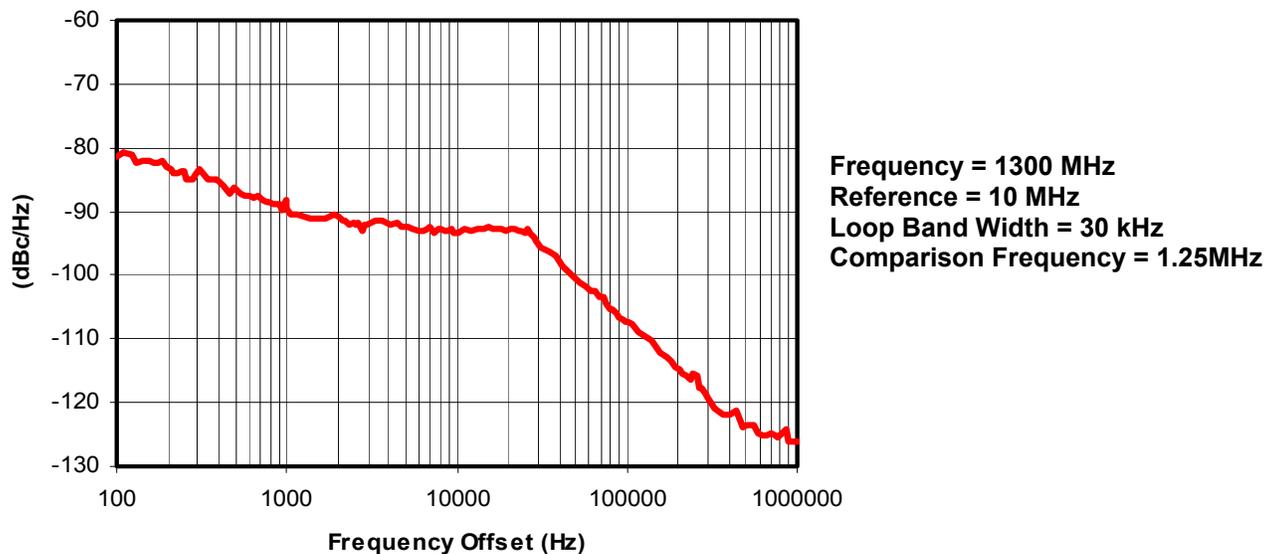


Figure 4. Typical Phase Noise Performance

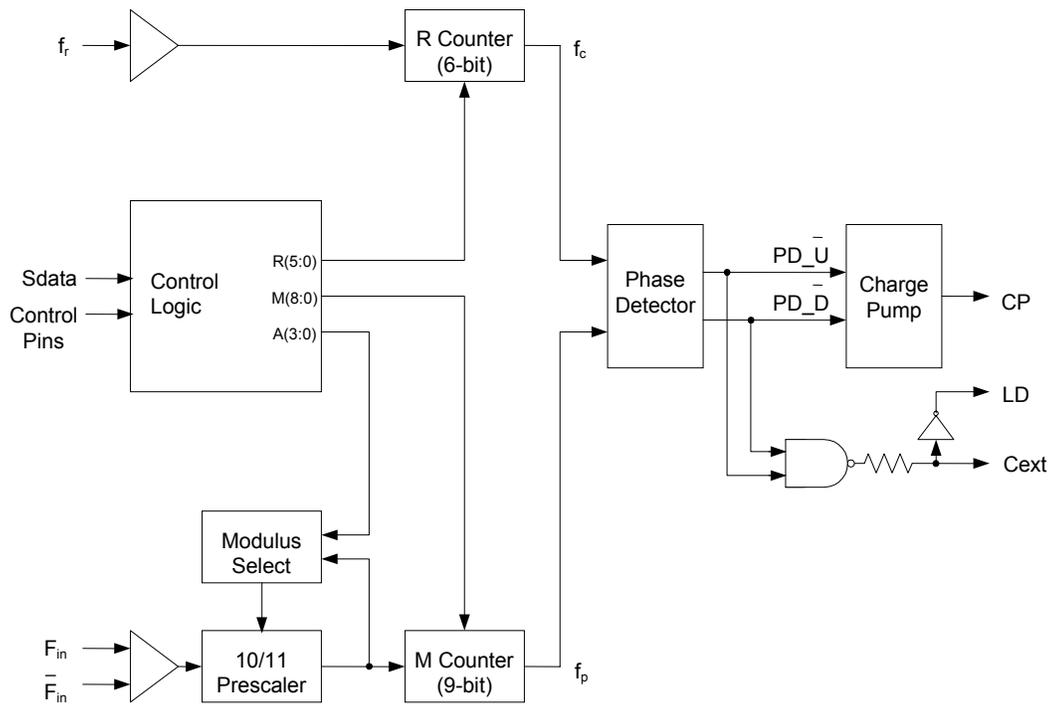


Functional Description

The PE3239 consists of a prescaler, counters, a phase detector, charge pump and control logic. The dual modulus prescaler divides the VCO frequency by either 10 or 11, depending on the value of the modulus select. Counters “R” and “M” divide the reference and prescaler output, respectively, by integer values stored in a 20-bit register. An additional counter (“A”) is used in the modulus select logic.

The phase-frequency detector generates up and down frequency control signals which direct the charge pump operation. The control logic includes a selectable chip interface. Data is written into the internal registers via the three wire serial bus. There are also various operational and test modes and a lock detect output.

Figure 5. Functional Block Diagram



Main Counter Chain

The main counter chain divides the RF input frequency, F_{in} , by an integer derived from the user defined values in the “M” and “A” counters. It is composed of the 10/11 dual modulus prescaler, modulus select logic, and 9 bit M counter. Setting $\overline{Pre_en}$ “low” enables the 10/11 prescaler. Setting $\overline{Pre_en}$ “high” allows F_{in} to bypass the prescaler and powers down the prescaler.

The output from the main counter chain, f_p , is related to the VCO frequency, F_{in} , by the following equation:

$$f_p = F_{in} / [10 \times (M + 1) + A] \quad (1)$$

where $A \leq M + 1, M \neq 0$

When the loop is locked, F_{in} is related to the reference frequency, f_r , by the following equation:

$$F_{in} = [10 \times (M + 1) + A] \times (f_r / (R+1)) \quad (2)$$

where $A \leq M + 1, M \neq 0$

A consequence of the upper limit on A is that F_{in} must be greater than or equal to $90 \times (f_r / (R+1))$ to obtain contiguous channels. Programming the M Counter with the minimum value of “1” will result in a minimum M Counter divide ratio of “2”.

Reference Counter

The reference counter chain divides the reference frequency, f_r , down to the phase detector comparison frequency, f_c .

The output frequency of the 6 bit R Counter is related to the reference frequency by the following equation:

$$f_c = f_r / (R + 1) \quad (3)$$

where $R \geq 0$

Note that programming R equal to “0” will pass the reference frequency, f_r , directly to the phase detector.

Register Programming

Serial Interface Mode

While the $\overline{E_WR}$ input is “low” and the $\overline{S_WR}$ input is “low”, serial input data (Sdata input), \overline{B}_0 to \overline{B}_{19} , are clocked serially into the primary register on the rising edge of Sclk, MSB (\overline{B}_0) first. The contents from the primary register are transferred into the secondary register on the rising edge of either $\overline{S_WR}$ according to the timing diagrams shown in Figure 6. Data are transferred to the counters as shown in Table 7 on page 9.

The double buffering provided by the primary and secondary registers allows for “ping-pong” counter control using the FSELS input. When FSELS is “high”, the primary register contents set the counter inputs. When FSELS is “low”, the secondary register contents are utilized.

While the $\overline{E_WR}$ input is “high” and the $\overline{S_WR}$ input is “low”, serial input data (Sdata input), \overline{B}_0 to \overline{B}_7 , are clocked serially into the enhancement register on the rising edge of Sclk, MSB (\overline{B}_0) first. The enhancement register is double buffered to prevent inadvertent control changes during serial loading, with buffer capture of the serially entered data performed on the falling edge of $\overline{E_WR}$ according to the timing diagram shown in Figure 6. After the falling edge of $\overline{E_WR}$, the data provide control bits as shown in Table 8 on page 9 will have their bit functionality enabled by asserting the \overline{Enh} input “low”.

Table 7. Primary Register Programming

Interface Mode	$\overline{\text{Enh}}$	R ₅	R ₄	M ₆	M ₇	$\overline{\text{Pre_en}}$	M ₆	M ₅	M ₄	M ₃	M ₂	M ₁	M ₀	R ₃	R ₂	R ₁	R ₀	A ₃	A ₂	A ₁	A ₀
Serial*	1	B ₀	B ₁	B ₂	B ₃	B ₄	B ₅	B ₆	B ₇	B ₈	B ₉	B ₁₀	B ₁₁	B ₁₂	B ₁₃	B ₁₄	B ₁₅	B ₁₆	B ₁₇	B ₁₈	B ₁₉

*Serial data clocked serially on Sclk rising edge while E_WR “low” and captured in secondary register on S_WR rising edge.



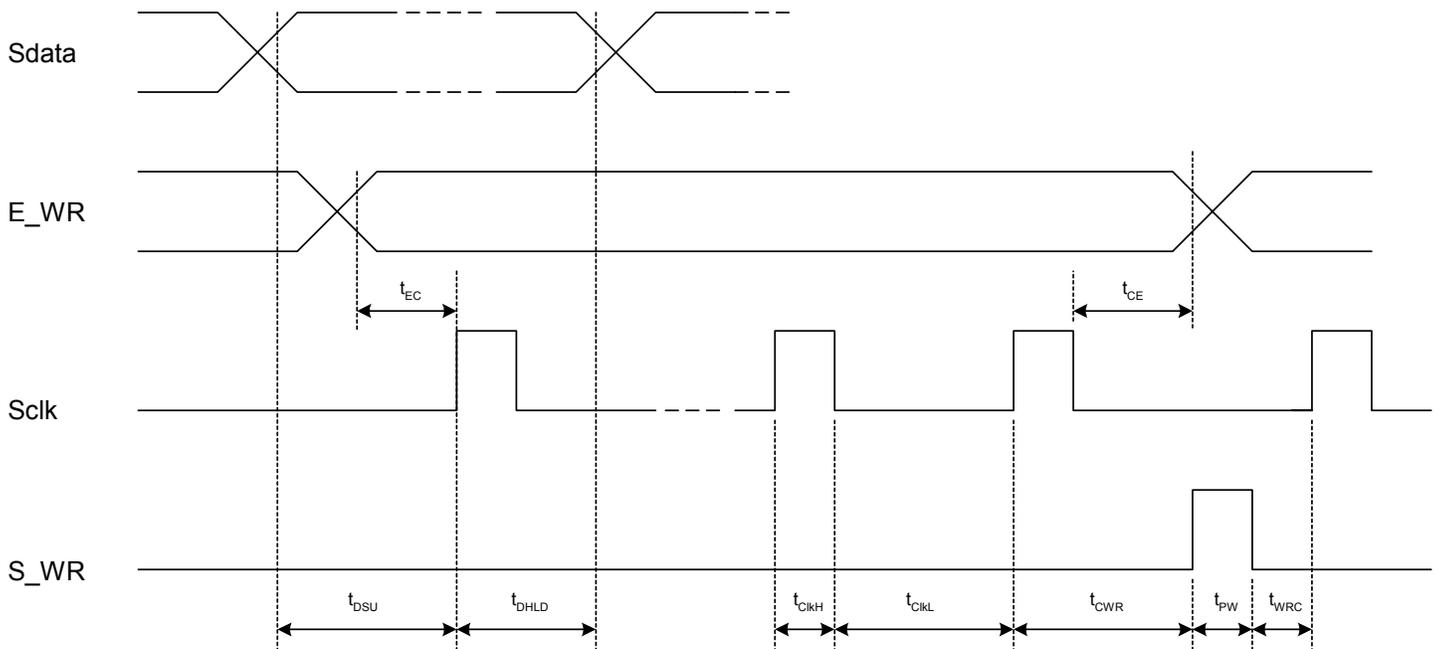
Table 8. Enhancement Register Programming

Interface Mode	$\overline{\text{Enh}}$	Reserved	Reserved	f _p Output	Power down	Counter load	MSEL output	f _c output	Reserved
Serial*	0	B ₀	B ₁	B ₂	B ₃	B ₄	B ₅	B ₆	B ₇

*Serial data clocked serially on Sclk rising edge while E_WR “high” and captured in the double buffer on E_WR falling edge.



Figure 6. Serial Interface Mode Timing Diagram



Enhancement Register

The functions of the enhancement register bits are shown below with all bits active “high”.

Table 9. Enhancement Register Bit Functionality

Bit Function		Description
Bit 0	Reserved**	
Bit 1	Reserved**	
Bit 2	f_p output	Drives the M counter output onto the Dout output.
Bit 3	Power down	Power down of all functions except programming interface.
Bit 4	Counter load	Immediate and continuous load of counter programming.
Bit 5	MSEL output	Drives the internal dual modulus prescaler modulus select (MSEL) onto the Dout output.
Bit 6	f_c output	Drives the reference counter output onto the Dout output
Bit 7	Reserved**	

** Program to 0

Phase Detector

The phase detector is triggered by rising edges from the main Counter (f_p) and the reference counter (f_c). It has two outputs, namely $PD_{\bar{U}}$ and $PD_{\bar{D}}$. If the divided VCO leads the divided reference in phase or frequency (f_p leads f_c), $PD_{\bar{D}}$ pulses “low”. If the divided reference leads the divided VCO in phase or frequency (f_c leads f_p), $PD_{\bar{U}}$ pulses “low”. The width of either pulse is directly proportional to phase offset between the two input signals, f_p and f_c .

The signals from the phase detector couple directly to a charge pump. $PD_{\bar{U}}$ controls a current source at pin CP with constant amplitude and pulse duration approximately the same as $PD_{\bar{U}}$. $PD_{\bar{D}}$ similarly drives a current sink at pin CP. The

current pulses from pin CP are low pass filtered externally and then connected to the VCO tune voltage. $PD_{\bar{U}}$ pulses result in a current source, which increases the VCO frequency and $PD_{\bar{D}}$ results in a current sink, which decreases VCO frequency when using a positive K_v VCO.

A lock detect output, LD is also provided, via the pin Cext. Cext is the logical “NAND” of $PD_{\bar{U}}$ and $PD_{\bar{D}}$ waveforms, which is driven through a series 2 kohm resistor. Connecting Cext to an external shunt capacitor provides low pass filtering of this signal. Cext also drives the input of an internal inverting comparator with an open drain output. Thus LD is an “AND” function of $PD_{\bar{U}}$ and $PD_{\bar{D}}$.

Figure 7. Typical PE3239 Loop Filter Application Example

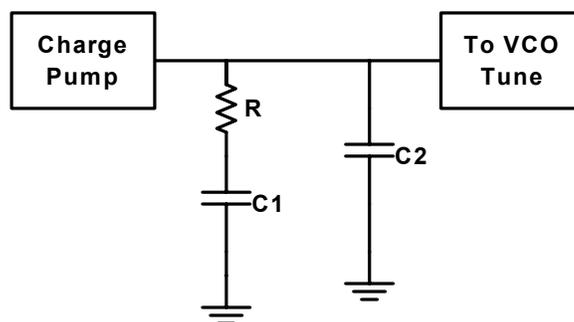


Figure 8. Package Drawing

20-lead TSSOP (JEDEC MO-153-AC)

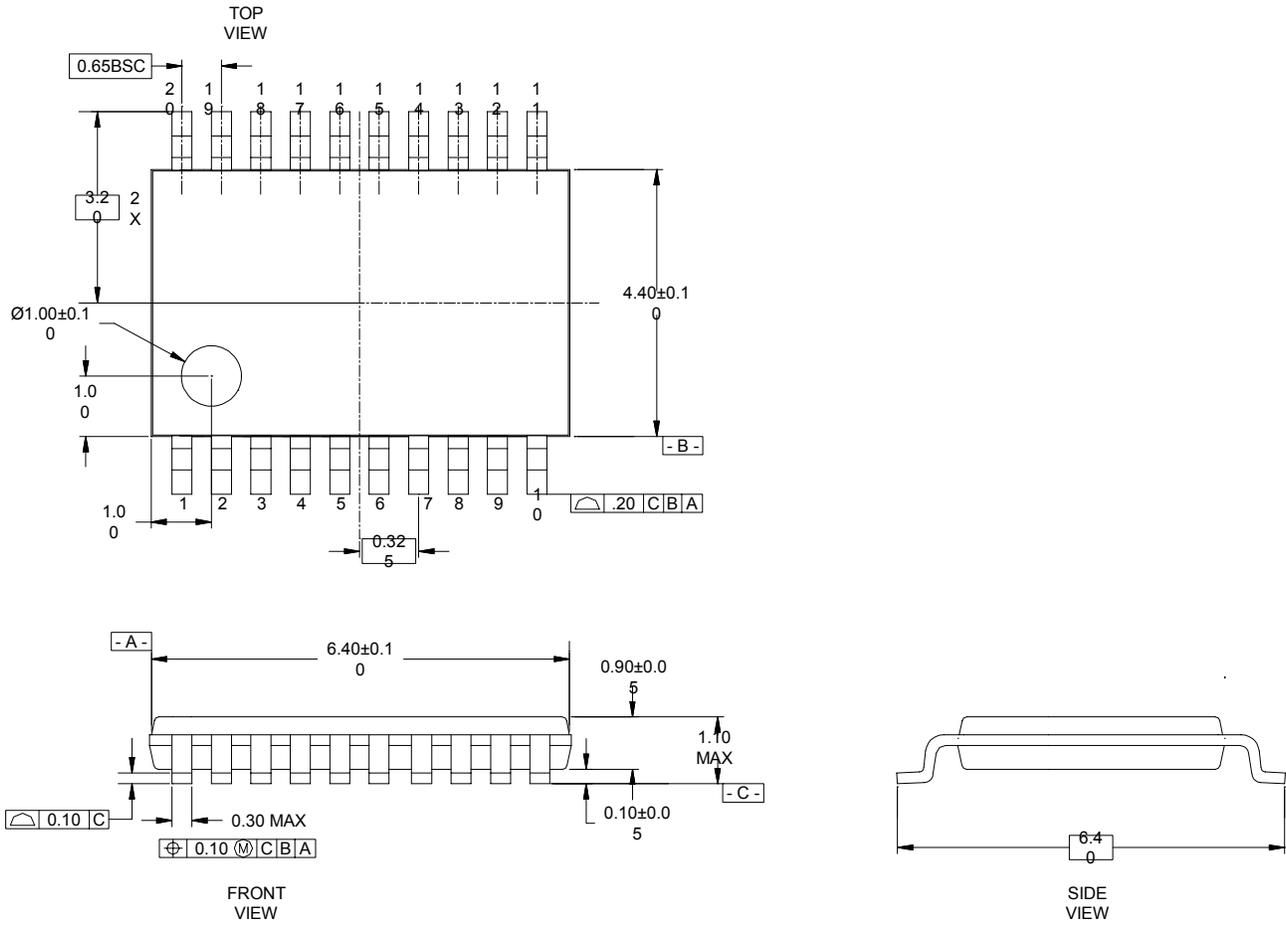


Table 10. Ordering Information

Order Code	Part Marking	Description	Package	Shipping Method
3239-11	PE3239	PE3239-20TSSOP-74A	20-lead TSSOP	74 units / Tube
3239-12	PE3239	PE3239-20TSSOP-2000C	20-lead TSSOP	2000 units / T&R
3239-00	PE3239EK	PE3239-20TSSOP-EVAL KIT	Evaluation Board	1 / Box

Sales Offices

United States

Peregrine Semiconductor Corp.

6175 Nancy Ridge Drive
San Diego, CA 92121
Tel 1-858-455-0660
Fax 1-858-455-0770

Europe

Peregrine Semiconductor Europe

Aix-En-Provence Office
Parc Club du Golf, bat 9
13856 Aix-En-Provence Cedex 3
France
Tel 33-0-4-4239-3360
Fax 33-0-4-4239-7227

Japan

Peregrine Semiconductor K.K.

The Imperial Tower, 15th floor
1-1-1 Uchisaiwaicho, Chiyoda-ku
Tokyo 100-0011 Japan
Tel: 03-3507-5755
Fax: 03-3507-5601

Australia

Peregrine Semiconductor Australia

8 Herb Elliot Ave.
Homebush, NSW 2140
Australia
Tel: 011-61-2-9763-4111
Fax: 011-61-2-9746-1501

For a list of representatives in your area, please refer to our Web site at: <http://www.peregrine-semi.com>

Data Sheet Identification

Advance Information

The product is in a formative or design stage. The data sheet contains design target specifications for product development. Specifications and features may change in any manner without notice.

Preliminary Specification

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