Advance Information

4K

X20C04

512 x 8 Bit

Nonvolatile Static RAM

T-46-23-37

FEATURES

- **High Reliability**
  - **—Endurance: 1,000,000 Store Operations**
  - **—Retention: 100 Years Minimum**
- **Power-on Recall**
  - **—E²PROM Data Automatically Recalled Into SRAM Upon Power-up**
- **Lock Out Inadvertent Store Operations**
- **Low Power CMOS**
  - **—Standby: 250µA**
- **Infinite E²PROM Array Recall, and RAM Read and Write Cycles**
- **Compatible with X2004**

DESCRIPTION

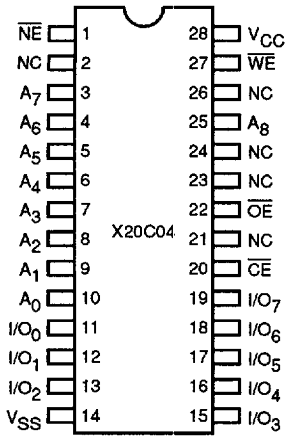
The Xicor X20C04 is a 512 x 8 NOVRAM featuring a static RAM overlaid bit-for-bit with a nonvolatile electrically erasable PROM (E²PROM). The X20C04 is fabricated with advanced CMOS floating gate technology to achieve low power and wide power-supply margin. The X20C04 features the JEDEC approved pinout for bytewide memories, compatible with industry standard RAMs, ROMs, EPROMS and E²PROMs.

The NOVRAM design allows data to be easily transferred from RAM to E²PROM (store) and E²PROM to RAM (recall). The store operation is completed in 5 ms or less and the recall operation is completed in 5 µs or less.

Xicor NOVRAMS are designed for unlimited write operations to RAM, either from the host or recalls from E²PROM, and a minimum 1,000,000 store operations to the E²PROM. Data retention is specified to be greater than 100 years.

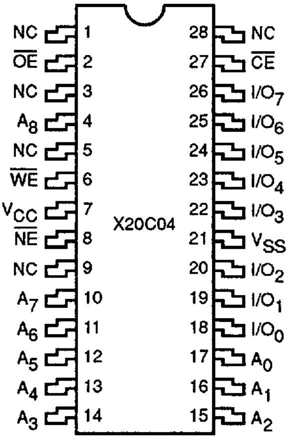
PIN CONFIGURATION

PLASTIC
CERDIP



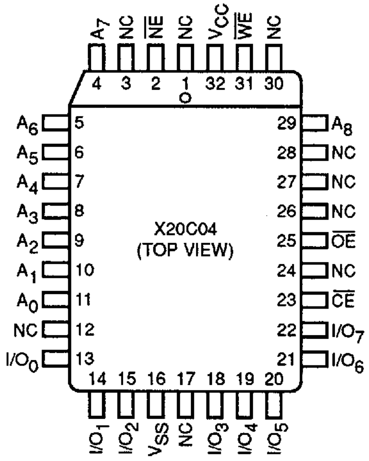
3825 FHD F02

SOIC



3825 FHD F16

LCC
PLCC



3825 FHD F03

PIN DESCRIPTIONS

Addresses (A_0–A_8)

The Address inputs select an 8-bit memory location during a read or write operation.

Chip Enable ($\overline{CE}$)

The Chip Enable input must be LOW to enable all read/write operations. When $\overline{CE}$ is HIGH, power consumption is reduced.

Output Enable ($\overline{OE}$)

The Output Enable input controls the data output buffers and is used to initiate read and recall operations. Output Enable LOW disables a store operation regardless of the state of $\overline{CE}$, $\overline{WE}$ or $\overline{NE}$.

Data In/Data Out (I/O_0–I/O_7)

Data is written to or read from the X20C04 through the I/O pins. The I/O pins are placed in the high impedance state when either $\overline{CE}$ or $\overline{OE}$ is HIGH or when $\overline{NE}$ is LOW.

Write Enable ($\overline{WE}$)

The Write Enable input controls the writing of data to both the static RAM and stores to the E²PROM.

Nonvolatile Enable ($\overline{NE}$)

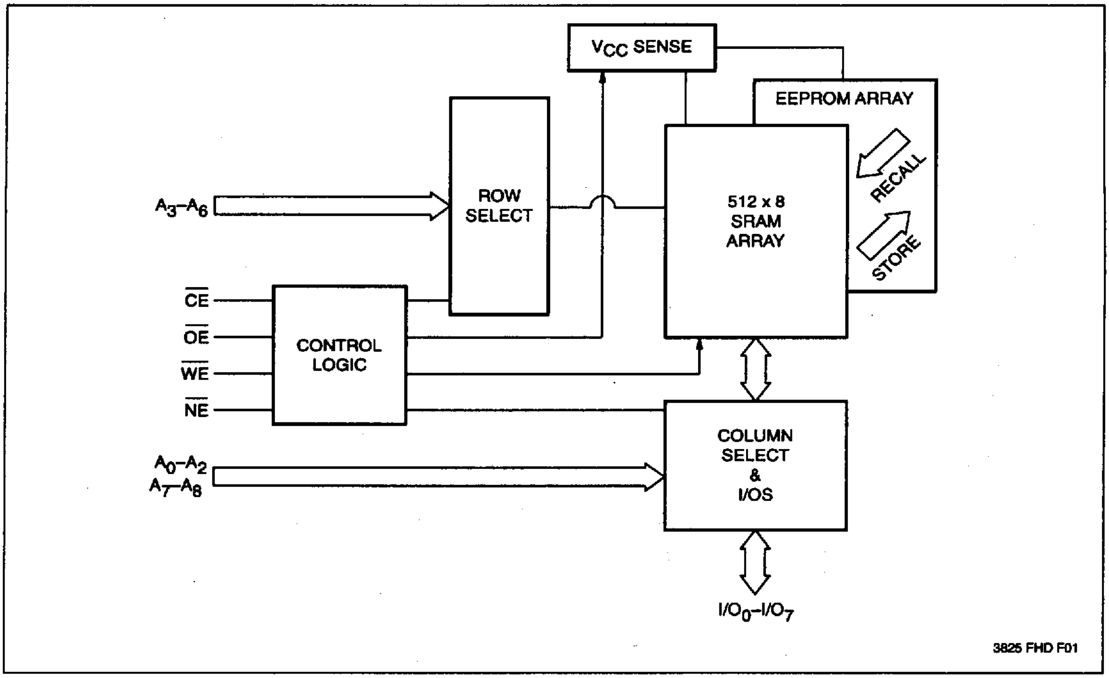
The Nonvolatile Enable input controls all accesses to the E²PROM array (store and recall functions).

PIN NAMES

Symbol	Description
A_0–A_8	Address Inputs
I/O_0–I/O_7	Data Input/Output
$\overline{WE}$	Write Enable
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
$\overline{NE}$	Nonvolatile Enable
V_{CC}	+5V
V_{SS}	Ground
NC	No Connect

3825 PGM T01

FUNCTIONAL DIAGRAM



DEVICE OPERATION

The $\overline{CE}$, $\overline{OE}$, $\overline{WE}$ and $\overline{NE}$ inputs control the X20C04 operation. The X20C04 byte-wide NOVRAM uses a 2-line control architecture to eliminate bus contention in a system environment. The I/O bus will be in a high impedance state when either $\overline{OE}$ or $\overline{CE}$ is HIGH, or when $\overline{NE}$ is LOW.

RAM Operations

RAM read and write operations are performed as they would be with any static RAM. A read operation requires $\overline{CE}$ and $\overline{OE}$ to be LOW with $\overline{WE}$ and $\overline{NE}$ HIGH. A write operation requires $\overline{CE}$ and $\overline{WE}$ to be LOW with $\overline{NE}$ HIGH. There is no limit to the number of read or write operations performed to the RAM portion of the X20C04.

Nonvolatile Operations

With $\overline{NE}$ LOW, recall operation is performed in the same manner as RAM read operation. A recall operation causes the entire contents of the E²PROM to be written into the RAM array. The time required for the operation to complete is 5µs or less. A store operation causes the entire contents of the RAM array to be stored in the nonvolatile E²PROM. The time for the operation to complete is 5 ms or less.

Power-Up Recall

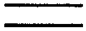
Upon power-up (V_{CC}), the X20C04 performs an automatic array recall. When V_{CC} minimum is reached, the recall is initiated, regardless of the state of $\overline{CE}$, $\overline{OE}$, $\overline{WE}$ and $\overline{NE}$.

Write Protection

The X20C04 has five write protect features that are employed to protect the contents of both the nonvolatile memory and the RAM.

- V_{CC} Sense—All functions are inhibited when V_{CC} is $\leq$ 3.5V.
- A RAM write is required before a Store Cycle is initiated.
- Write Inhibit—Holding either $\overline{OE}$ low, $\overline{WE}$ high, $\overline{CE}$ high or $\overline{NE}$ high during power up and power down will prevent an inadvertent store operation.
- Noise Protection—A combined $\overline{WE}$, $\overline{NE}$, $\overline{OE}$ and $\overline{CE}$ pulse of less than 20ns will not initiate a Store Cycle.
- Noise Protection—A combined $\overline{WE}$, $\overline{NE}$, $\overline{OE}$ and $\overline{CE}$ pulse of less than 20ns will not initiate a recall cycle.

SYMBOL TABLE

WAVEFORM	INPUTS	OUTPUTS
	Must be steady	Will be steady
	May change from Low to High	Will change from Low to High
	May change from High to Low	Will change from High to Low
	Don't Care: Changes Allowed	Changing: State Not Known
	N/A	Center Line is High Impedance

ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias ....–65°C to +135°C
Storage Temperature ....–65°C to +150°C
Voltage on any Pin with
Respect to Ground ....–1.0V to +7V
D.C. Output Current 10mA

*COMMENT

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and the functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

Temperature	Min.	Max.
Commercial	0°C	70°C
Industrial	–40°C	+85°C
Military	–55°C	+125°C

3825 PGM T02

Supply Voltage	Limits
X20C04	5V ±10%

3825 PGM T03

D.C. OPERATING CHARACTERISTICS (Over recommended operating conditions unless otherwise specified.)

Symbol	Parameter	Limits			Test Conditions
		Min.	Max.	Units	
I_{CC1}	V_{CC} Current (Active)		100	mA	$\overline{NE} = \overline{WE} = V_{IH}$, $\overline{CE} = \overline{OE} = V_{IL}$ Address Inputs = 0.4V/2.4V levels @ f = 5MHz. All I/Os = Open
I_{CC2}	V_{CC} Current During Store		10	mA	All Inputs = V_{IH} All I/Os = Open
I_{SB1}	V_{CC} Standby Current (TTL Input)		10	mA	$\overline{CE} = V_{IH}$ All Other Inputs = V_{IH}, All I/Os = Open
I_{SB2}	V_{CC} Standby Current (CMOS Input)		250	µA	All Inputs = $V_{CC} - 0.3$ All I/Os = Open
I_{LI}	Input Leakage Current		10	µA	V_{IN} = GND to V_{CC}
I_{LO}	Output Leakage Current		10	µA	V_{OUT} = GND to V_{CC}, $\overline{CE} = V_{IH}$
$V_{IL}^{(1)}$	Input Low Voltage	–1.0	0.8	V	
$V_{IH}^{(1)}$	Input High Voltage	2.0	$V_{CC} + 0.5$	V	
V_{OL}	Output Low Voltage		0.4	V	$I_{OL} = 2.1mA$
V_{OH}	Output High Voltage	2.4		V	$I_{OH} = -400\mu A$

3825 PGM T04

POWER-UP TIMING

Symbol	Parameter	Max.	Units
$t_{PUR}^{(2)}$	Power-Up to RAM Operation	100	µs
$t_{PUW}^{(2)}$	Power-Up to Nonvolatile Operation	5	ms

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CAPACITANCE $T_A = 25°C$, F = 1.0MHZ, $V_{CC} = 5V$.

Symbol	Test	Max.	Units	Conditions
$C_{I/O}^{(2)}$	Input/Output Capacitance	10	pF	$V_{I/O} = 0V$
$C_{IN}^{(2)}$	Input Capacitance	6	pF	$V_{IN} = 0V$

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Notes: (1) V_{IL} min. and V_{IH} max. are for reference only and are not tested.
(2) This parameter is periodically sampled and not 100% tested.

ENDURANCE AND DATA RETENTION

Parameter	Min.	Units
Endurance	100,000	Changes/Bit
Store Cycles	1,000,000	Store Cycles
Data Retention	100	Years

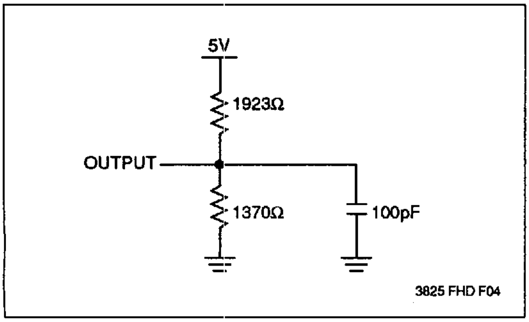
3825 PGM T07

MODE SELECTION

$\overline{CE}$	$\overline{WE}$	$\overline{NE}$	$\overline{OE}$	Mode	I/O	Power
H	X	X	X	Not Selected	Output High Z	Standby
L	H	H	L	Read RAM	Output Data	Active
L	L	H	X	Write "1" RAM	Input Data High	Active
L	L	H	X	Write "0" RAM	Input Data Low	Active
L	H	L	L	Array Recall	Output High Z	Active
L	L	L	H	Nonvolatile Storing	Output High Z	Active
L	H	H	H	Output Disabled	Output High Z	Active
L	L	L	L	Not Allowed	Output High Z	Active
L	H	L	H	No Operation	Output High Z	Active

3825 PGM T09

EQUIVALENT A.C. LOAD CIRCUIT



3825 FHD F04

A.C. CONDITIONS OF TEST

Input Pulse Levels	0V to 3.0V
Input Rise and Fall Times	10 ns
Input and Output Timing Levels	1.5V

3825 PGM T08

A.C. CHARACTERISTICS (Over the recommended operating conditions unless otherwise specified)

Read Cycle Limits

Symbol	Parameter	X20C04-15		X20C04-20		X20C04-25		X20C04		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t_{RC}	Read Cycle Time	150		200		250		300		ns
t_{CE}	Chip Enable Access Time		150		200		250		300	ns
t_{AA}	Address Access Time		150		200		250		300	ns
t_{OE}	Output Enable Access Time		50		70		100		150	ns
$t_{LZ}^{(3)}$	Chip Enable to Output in Low Z	0		0		0		0		ns
$t_{OLZ}^{(3)}$	Output Enable to Output in Low Z	0		0		0		0		ns
$t_{HZ}^{(3)}$	Chip Disable to Output in High Z		80		100		100		100	ns
$t_{OHZ}^{(3)}$	Output Disable to Output in High Z		80		100		100		100	ns
t_{OH}	Output Hold From Address Change	0		0		0		0		ns

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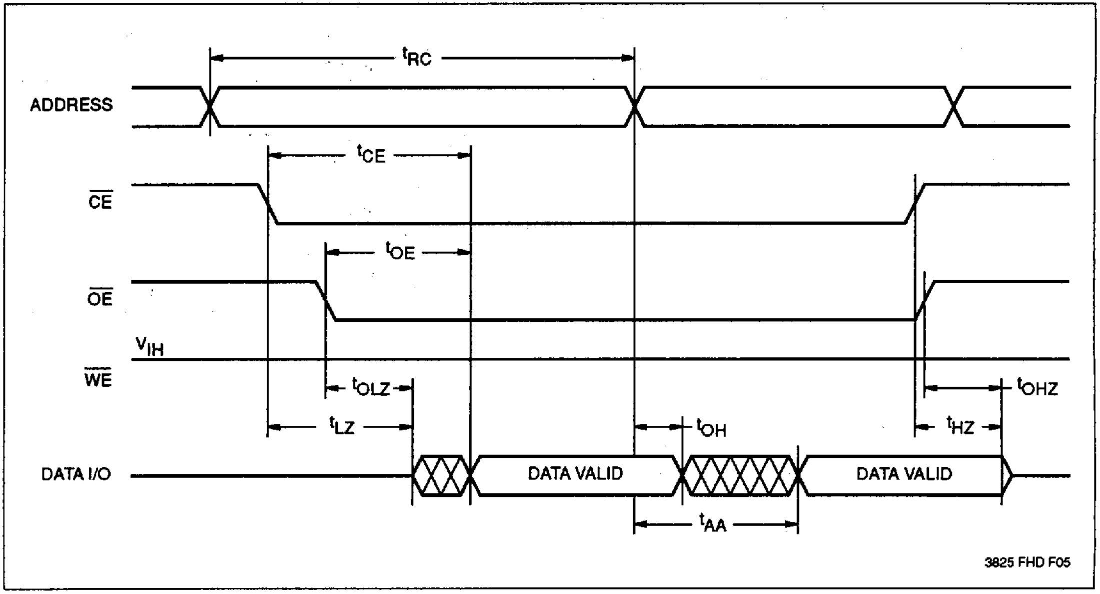
Read Cycle



Note: (3) t_{LZ} min., t_{HZ}, t_{OLZ} min., and t_{OHZ} are periodically sampled and not 100% tested. t_{HZ} max. and t_{OHZ} max. are measured, with C_L = 5pF from the point when $\overline{CE}$ or $\overline{OE}$ return high (whichever occurs first) to the time when the outptus are no longer driven.

Write Cycle Limits

Symbol	Parameter	X20C04-15		X20C04-20		X20C04-25		X20C04		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t_{WC}	Write Cycle Time	150		200		250		300		ns
t_{CW}	Chip Enable to End of Write Input	150		200		250		300		ns
t_{AS}	Address Setup Time	0		0		0		0		ns
t_{WP}	Write Pulse Width	100		120		150		200		ns
t_{WR}	Write Recovery Time	0		0		0		0		ns
t_{DW}	Data Setup to End of Write	100		120		150		200		ns
t_{DH}	Data Hold Time	0		0		0		0		ns
t_{WZ}(4)	Write Enable to Output in High Z		80		100		100		100	ns
t_{OW}(4)	Output Active from End of Write	5		5		5		5		ns
t_{OZ}(4)	Output Enable to Output in High Z		80		100		100		100	ns

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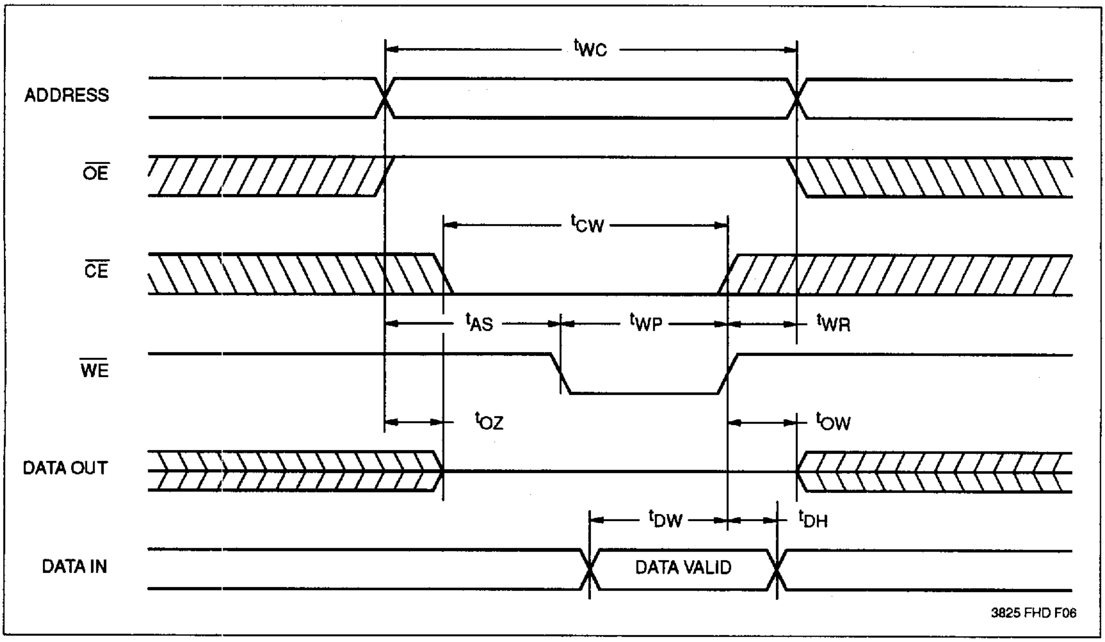
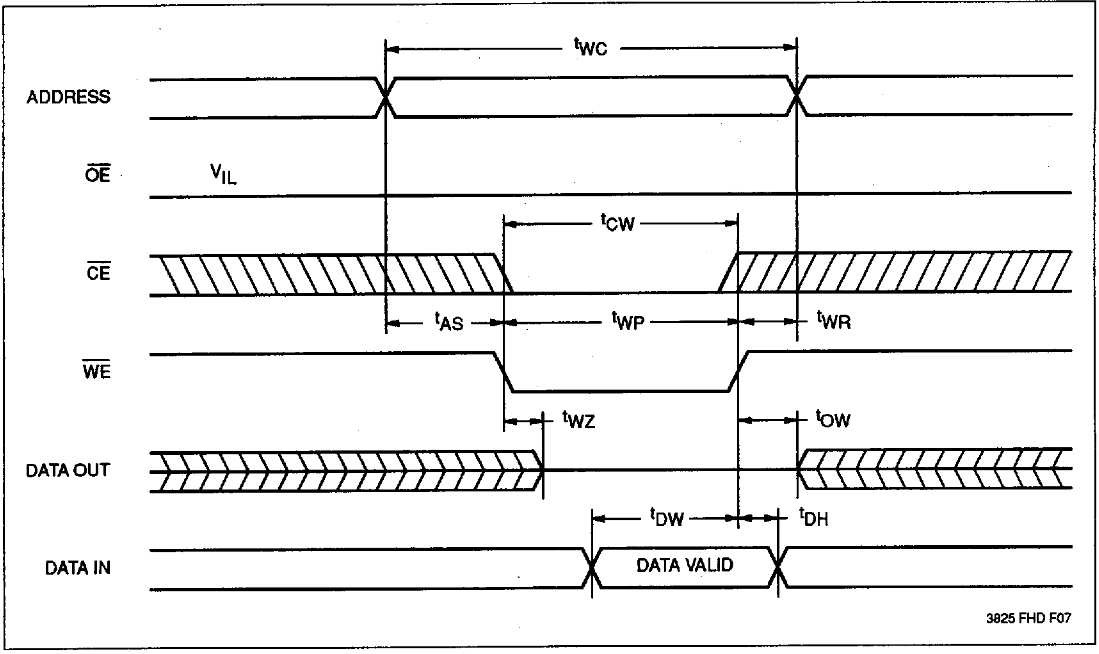
$\overline{\text{WE}}$ Controlled Write Cycle



Note: (4) t_{WZ}, t_{OW}, and t_{OZ} are periodically sampled and not 100% tested.

$\overline{CE}$ Controlled Write Cycle



STORE CYCLE LIMITS

Symbol	Parameter	X20C04-15		X20C04-20		X20C04-25		X20C04		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t_{STC}	Store Cycle Time		5		5		5		5	ms
t_{SP}	Store Pulse Width	100		120		150		200		ns
t_{NHZ}	Nonvolatile Enable to Output in High Z		80		100		100		100	ns
t_{OEST}	Output Enable From End of Store	10		10		10		10		ns
t_{SOE}	$\overline{OE}$ Disable to Store Function	20		20		20		20		ns
t_{NS}	$\overline{NE}$ Setup Time from $\overline{WE}$	0		0		0		0		ns

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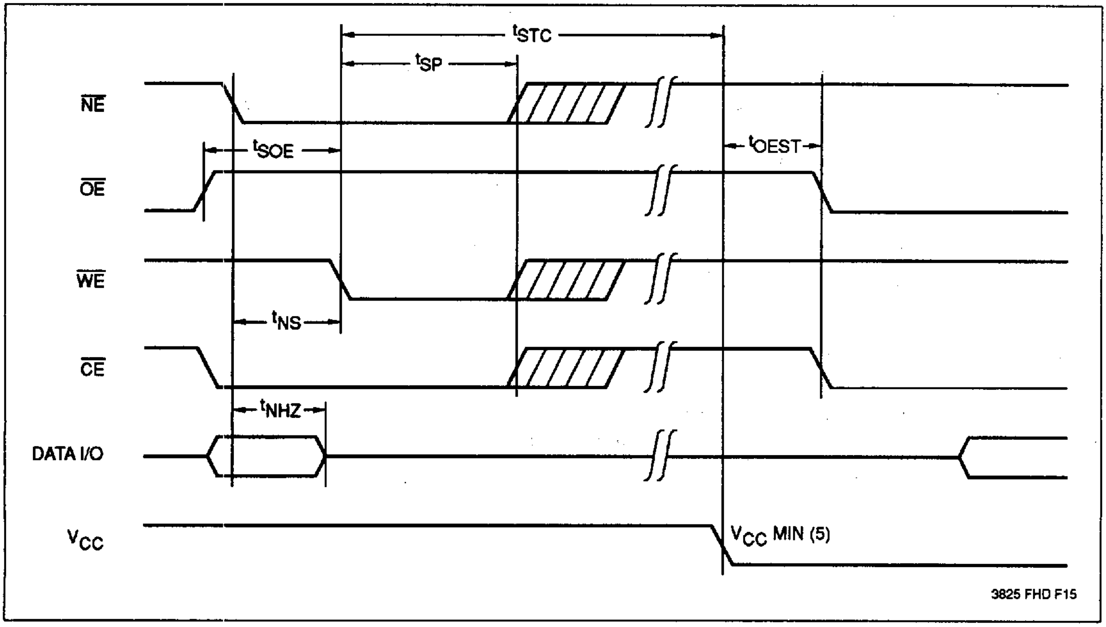
Store Timing



3825 FHD F15

Note: (5) X20C04 V_{CC} Min. = 4.5V

The Store Pulse Width (t_{SP}) is a minimum time that $\overline{NE}$, $\overline{WE}$ and $\overline{CE}$ must be LOW simultaneously. To insure data integrity, $\overline{NE}$ and $\overline{CE}$ must return HIGH after initiation of and throughout the duration (t_{STC}) of the Store operation. During t_{STC}, $\overline{OE}$ and $\overline{WE}$ may go LOW providing the host system access to other devices in the system.

ARRAY RECALL CYCLE LIMITS

Symbol	Parameter	X20C04-15		X20C04-20		X20C04-25		X20C04		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t_{RCC}	Array Recall Cycle Time		5		5		5		5	µs
t_{RCP}(6)	Recall Pulse Width to InitiateRecall	100		120		150		200		ns
t_{RWE}	$\overline{WE}$ Setup Time to $\overline{NE}$	0		0		0		0		ns

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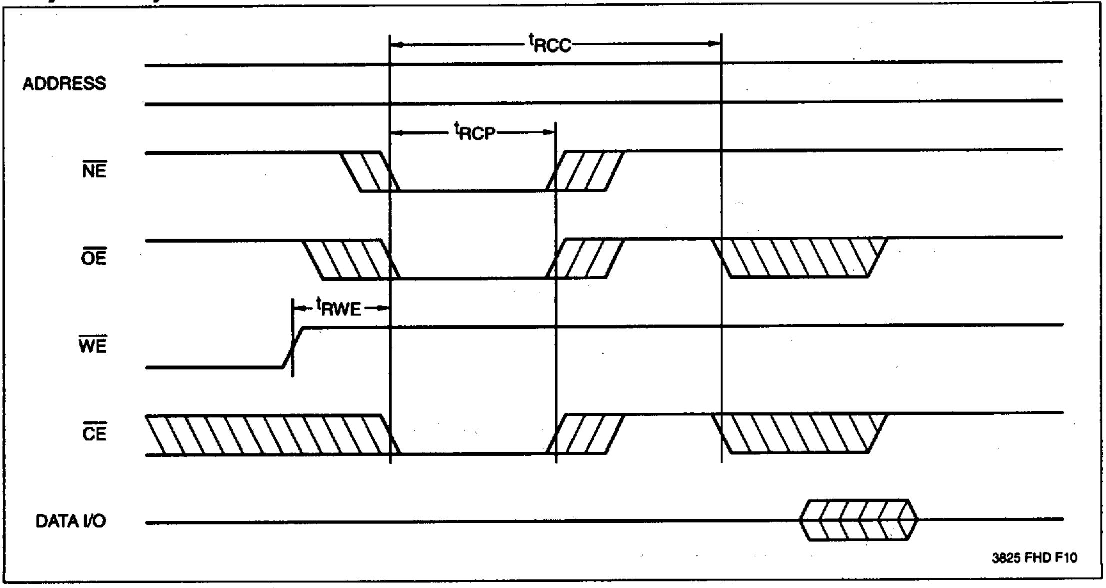
Array Recall Cycle



Note: (6) The Recall Pulse Width (t_{RCP}) is a minimum time that $\overline{NE}$, $\overline{OE}$ and $\overline{CE}$ must be LOW simultaneously. To insure data integrity, $\overline{NE}$ and $\overline{CE}$ must return HIGH after initiation of and through the duration (t_{RCC}) of the Recall operation. During t_{RCC}, $\overline{OE}$ and $\overline{WE}$ may go LOW providing the host access to other devices in the system.