REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Add device types 04, 05, and 06. Modify boilerplate to include rad hard requirements. Editorial changes throughout.	96-03-13	Monica L. Poelking
B	Add device types 07, 08, and 09. Update boilerplate. Editorial changes throughout. - tvn	98-08-27	Monica L. Poelking
C	In table I, change I_{IN} limits; add footnote to I_{DDQ}; add t_c in power-up master reset timing section; add footnote to V_{OS} and V_{DIS}. Correct the JTAG timing waveforms. Change footnote 3/ in table III. – tvn	99-04-28	Monica L. Poelking

REV	B	B	B	C																
SHEET	35	36	37	38																
REV	C	B	B	B	B	B	B	B	B	B	B	B	B	C	B	C	B	B	B	B
SHEET	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34

REV STATUS OF SHEETS	REV	C	B	B	B	B	B	C	C	C	C	C	C	C	C
	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14

PMIC N/A	PREPARED BY Thomas M. Hess	**DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS, OHIO 43216**
STANDARD MICROCIRCUIT THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE AMSC N/A	CHECKED BY Thomas M. Hess	
	APPROVED BY Monica L. Poelking	MICROCIRCUIT, DIGITAL, CMOS, SERIAL MICROCODED MULTI-MODE INTELLIGENT TERMINAL AND TRANSCEIVER, SILICON
	DRAWING APPROVAL DATE 95-03-31	
	REVISION LEVEL C	SIZE **A** / CAGE CODE **67268** / **5962-94663**
		SHEET 1 OF 38

DSCC FORM 2233
APR 97

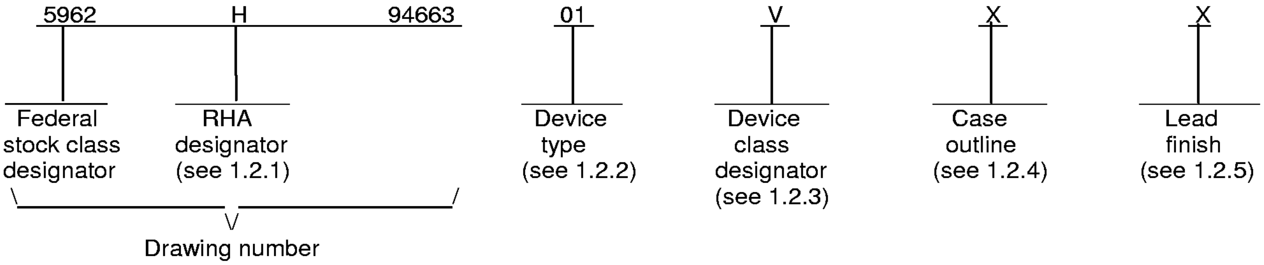
5962-E267-99

DISTRIBUTION STATEMENT A. Approved for public release; distribution is unlimited.

1. SCOPE

1.1 Scope. This drawing documents two product assurance class levels consisting of high reliability (device classes Q and M) and space application (device class V). A choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). When available, a choice of Radiation Hardness Assurance (RHA) levels are reflected in the PIN.

1.2 PIN. The PIN is as shown in the following example:



1.2.1 RHA designator. Device classes Q and V RHA marked devices meet the MIL-PRF-38535 specified RHA levels and are marked with the appropriate RHA designator. Device class M RHA marked devices meet the MIL-PRF-38535, appendix A specified RHA levels and are marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device type(s). The device type(s) identify the circuit function as follows:

Device type	Generic number	Circuit function
01	69151-LX15	Serial microcoded multi-mode intelligent terminal with 15-volt transceiver
02	69151-DX	Serial microcoded multi-mode intelligent terminal with 5-volt transceiver
03	69151-LX12	Serial microcoded multi-mode intelligent terminal with 12-volt transceiver
04	69151-LXE15	Enhanced serial microcoded multi-mode intelligent terminal with 15-volt transceiver radiation hardened
05	69151-DXE	Enhanced serial microcoded multi-mode intelligent terminal with 5-volt transceiver radiation hardened
06	69151-LXE12	Enhanced serial microcoded multi-mode intelligent terminal with 12-volt transceiver
07	69151-LXE15	Enhanced serial microcoded multi-mode intelligent terminal with 15-volt transceiver
08	69151-DXE	Enhanced serial microcoded multi-mode intelligent terminal with 5-volt transceiver
09	69151-LXE12	Enhanced serial microcoded multi-mode intelligent terminal with 12-volt transceiver

1.2.3 Device class designator. The device class designator is a single letter identifying the product assurance level as follows:

Device class	Device requirements documentation
M	Vendor self-certification to the requirements for MIL-STD-883 compliant, non-JAN class level B microcircuits in accordance with MIL-PRF-38535, appendix A
Q or V	Certification and qualification to MIL-PRF-38535

1.2.4 Case outline(s). The case outline(s) are as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
X	See figure 1	100	Pin grid array [1]
Y	See figure 1	100	Leaded chip carrier with nonconductive tier bar

1.2.5 Lead finish. The lead finish is as specified in MIL-PRF-38535 for device classes Q and V or MIL-PRF-38535, appendix A for device class M.

1.3 Absolute maximum ratings. [2]

Storage temperature range (T_{STG})	-65 C to +150 C
Operating case temperature range (T_C)	-55 C to +125 C
Transceiver supply voltage (V_{EE}):	
Device types 01, 03, 04, 06, 07, 09	-22 V dc
Transceiver supply voltage range (V_{CC}):	
Device types 02, 05, 08	-0.3 V dc to +7.0 V dc
Logic supply voltage range (V_{DD})	-0.3 V dc to +7.0 V dc
Input voltage range (V_{DR}):	
Device types 01, 03, 04, 06, 07, 09	42 $V_{P,L-L}$
Device types 02, 05, 08	10 $V_{P,L-L}$
Maximum power dissipation (P_D)	5 W
Logic voltage on any pin range ($V_{I/O}$)	-0.3 V dc to V_{DD} + 0.3 V dc
Logic latch-up immunity (I_{LU})	150 mA
Logic input current (I_I)	10 mA
Output current (I_O):	
Device types 01, 03, 04, 06, 07, 09	190 mA
Device types 02, 05, 08	1000 mA
Maximum junction temperature (T_J)	+150 C
Receiver common mode input voltage range (V_{IC}):	
Device types 01, 03, 04, 06, 07, 09	-11 V dc to +11 V dc
Device types 02, 05, 08	-5 V dc to +5 V dc
Lead temperature (soldering, 5 seconds)	+300 C
Thermal resistance junction-to-case ($_{JC}$): [3]	
Cases X and Y	7 C/W

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[1] This package contains 96 terminals on the bottom and 4 terminals on top of the package, see figure 1.

[2] Stress outside the listed absolute maximum rating may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions beyond limits indicated in the operational sections of this specification is not recommended. Exposure to absolute maximum rating conditions for extended periods affect device reliability.

[3] Per MIL-STD-883, Method 1012.

1.4 Recommended operating conditions.

Transceiver supply voltage range (V_{CC}):	
Device types 01, 03, 04, 06, 07, 09	+4.75 V dc to +5.5 V dc
Device type 02	+4.75 V dc to +5.25 V dc
Device types 05, 08	+4.5 V dc to +5.5 V dc
Logic supply voltage range (V_{DD})	+4.5 V dc to +5.5 V dc
Transceiver supply voltage range (V_{EE}):	
Device types 01, 04, 07	-15 V dc
Device types 03, 06, 09	-12 V dc
Receiver differential voltage (V_{DR}):	
Device types 01, 03, 04, 06, 07, 09	40 V_{P-P}
Device types 02, 05, 08	8.0 V_{P-P}
Logic dc input voltage range (V_{IN})	0 V dc to V_{DD}
Receiver common mode input voltage (V_{IC}):	
Device types 01, 03, 04, 06, 07, 09	10 V dc
Device types 02, 05, 08	5.0 V dc
Driver peak output current (I_O):	
Device types 01, 03, 04, 06, 07, 09	180 mA
Device types 02, 05, 08	700 mA
Serial data rate range (S_D)	0 to 1 MHz
Clock duty cycle (D_C)	50 5%
Case operating temperature range (T_C)	-55 C to +125 C
Operating frequency (F_{IN})	24 MHz 0.01%
Radiation features:	
Total dose	
Device type 04	100k Rads (Si)
Device type 05	1M Rads (Si)
Single event phenomenon (SEP) effective linear energy threshold, no upsets	[1]
Neutron fluence (TM 1017)	[1]

1.5 Digital logic testing for device classes Q and V.

Fault coverage measurement of manufacturing logic tests (MIL-STD-883, test method 5012)	95.12 percent

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those listed in the issue of the Department of Defense Index of Specifications and Standards (DoDISS) and supplement thereto, cited in the solicitation.

SPECIFICATION

DEPARTMENT OF DEFENSE

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

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[1] Values will be added when they become available. Rad hard devices have not yet been tested for neutron or SEP.

STANDARDS

DEPARTMENT OF DEFENSE

MIL-STD-883 -	Test Methods and Procedures for Microelectronics.
MIL-STD-973 -	Configuration Management.
MIL-STD-1835 -	Interface Standard For Microcircuit Case Outlines.

HANDBOOKS

DEPARTMENT OF DEFENSE

MIL-HDBK-103 -	List of Standard Microcircuit Drawings (SMD's).
MIL-HDBK-780 -	Standard Microcircuit Drawings.

(Unless otherwise indicated, copies of the specification, standards, and handbooks are available from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

2.2 Non-Government publications. The following document(s) form a part of this document to the extent specified herein. Unless otherwise specified, the issues of the documents which are DOD adopted are those listed in the issue of the DODISS cited in the solicitation. Unless otherwise specified, the issues of documents not listed in the DODISS are the issues of the documents cited in the solicitation.

INSTITUTE OF ELECTRICAL AND ELECTRONICS ENGINEERS (IEEE)

IEEE Standard 1149.1 - IEEE Standard Test Access Port and Boundary Scan Architecture.

(Applications for copies should be addressed to the Institute of Electrical and Electronics Engineers, 445 Hoes Lane, Piscataway, NJ 08854-4150.)

(Non-Government standards and other publications are normally available from the organizations that prepare or distribute the documents. These documents may also be available in or through libraries or other informational services.)

2.3 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device classes Q and V shall be in accordance with MIL-PRF-38535 and as specified herein or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein. The individual item requirements for device class M shall be in accordance with MIL-PRF-38535, appendix A for non-JAN class level B devices and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535 and herein for device classes Q and V or MIL-PRF-38535, appendix A and herein for device class M.

3.2.1 Case outlines. The case outlines shall be in accordance with 1.2.4 and figure 1 herein.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 2.

3.2.3 Block diagram. The block diagram shall be as specified on figure 3.

3.2.4 Boundary scan instruction codes. The boundary scan instruction codes shall be as specified on figure 4.

3.2.5 Timing waveforms. The timing waveforms shall be as specified on figure 5.

3.2.6 Radiation exposure connections. The radiation exposure connections shall be as specified on figure 6.

3.3 Electrical performance characteristics and postirradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and postirradiation parameter limits are as specified in table IA and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table IIA. The electrical tests for each subgroup are defined in table IA.

3.5 Marking. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked as listed in MIL-HDBK-103. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device. For RHA product using this option, the RHA designator shall still be marked. Marking for device classes Q and V shall be in accordance with MIL-PRF-38535. Marking for device class M shall be in accordance with MIL-PRF-38535, appendix A.

3.5.1 Certification/compliance mark. The certification mark for device classes Q and V shall be a "QML" or "Q" as required in MIL-PRF-38535. The compliance mark for device class M shall be a "C" as required in MIL-PRF-38535, appendix A.

3.6 Certificate of compliance. For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.6.1 herein). For device class M, a certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-HDBK-103 (see 6.6.2 herein). The certificate of compliance submitted to DSCC-VA prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device classes Q and V, the requirements of MIL-PRF-38535 and herein or for device class M, the requirements of MIL-PRF-38535, appendix A and herein.

3.7 Certificate of conformance. A certificate of conformance as required for device classes Q and V in MIL-PRF-38535 or for device class M in MIL-PRF-38535, appendix A shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change for device class M. For device class M, notification to DSCC-VA of change of product (see 6.2 herein) involving devices acquired to this drawing is required for any change as defined in MIL-STD-973.

3.9 Verification and review for device class M. For device class M, DSCC, DSCC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

3.10 Microcircuit group assignment for device class M. Device class M devices covered by this drawing shall be in microcircuit group number H (see MIL-PRF-38535, appendix A).

3.11 IEEE 1149.1 compliance. Theses devices shall be compliant to IEEE 1149.1.

TABLE IA. Electrical performance characteristics.

Test	Symbol	Test conditions 1/ -55 C T_C +125 C 4.5 V V_{DD} 5.5 V unless otherwise specified		Device type	Group A subgroups	Limits		Unit
						Min	Max	
Low level input voltage	V_{IL1}			All	1, 2, 3		0.8	V
Low level input voltage, TCK only	V_{IL2}			01, 02 03, 04 05, 06	1, 2, 3		0.8	
				07, 08 09	1, 2, 3		0.7	
High level input voltage	V_{IH}			All	1, 2, 3	2.2		V
Low level input voltage 2/	V_{ILC}			All	1, 2, 3		$0.3V_{DD}$	V
High level input voltage 2/	V_{IHC}			All	1, 2, 3	$0.7V_{DD}$		V
Low level output voltage	V_{OL}	Output loads	I_{OL} = 4.0 mA	All	1, 2, 3		0.4	V
			I_{OL} = 1.0 A 3/				0.05	
High level output voltage	V_{OH}	Output loads	I_{OH} = 4.0 mA	All	1, 2, 3	2.4		V
			I_{OH} = 1.0 A 3/			V_{DD}-0.05		
Input leakage current	I_{IN}	TTL driven inputs	$V_{IN} = V_{DD}$ or V_{SS}	All	1, 2, 3	-10	+10	A
		Inputs with pull-up resistors	$V_{IN} = V_{DD}$			-10	+10	
			$V_{IN} = V_{SS}$	01, 02, 03, 04, 05, 06	1, 2, 3	-900	-150	
				07, 08, 09		-167	-27	
Three-state output leakage current, TTL loaded outputs, single-drive buffer	I_{OZ}	$V_O = V_{DD}$ or V_{SS}		All	1, 2, 3	-10	+10	A
Short-circuit output current, output loads	I_{OS} 4/ 5/	V_{DD} = 5.5 V, V_O = 0 V V_{DD} = 5.5 V, $V_O = V_{DD}$		All	1, 2, 3	-100	+100	mA
Input capacitance	C_{IN}	f = 1 MHz at 0 V See 4.4.1c		All	4		45	pF
Output capacitance	C_{OUT}			All	4		45	
Bi-directional capacitance 6/	C_{IO}			All	4		45	
Quiescent current 7/ 8/	I_{DDQ}	f = 0 MHz		All	1, 3		35	A
					2		1	mA
Standby operating current	I_{DDS}	f = 24 MHz		All	1, 2, 3		40	mA

See footnotes at end of table.

TABLE IA. Electrical performance characteristics - Continued.

Test	Symbol	Test conditions 1/ -55 C T_C +125 C 4.5 V V_{DD} 5.5 V unless otherwise specified		Device type	Group A subgroups	Limits		Unit
						Min	Max	
V_{CC} supply current	I_{CC}	V_{EE} = -12 V V_{CC} = 5 V	0% duty cycle (non-transmitting)	03, 06 09	1, 2, 3		140	mA
			50% duty cycle (f = 1 MHz) 9/				140	
			100% duty cycle (f = 1 MHz) 9/				140	
		V_{EE} = -15 V V_{CC} = 5 V	0% duty cycle (non-transmitting)	01, 04 07			140	
			50% duty cycle (f = 1 MHz) 9/				140	
			100% duty cycle (f = 1 MHz) 9/				140	
		V_{CC} = 5 V	0% duty cycle (non-transmitting)	02, 05 08	1, 2, 3		55	
			25% duty cycle 10/				250	
			50% duty cycle (f = 1 MHz) 10/				410	
			87.5% duty cycle (f = 1 MHz) 10/				650	
			100% duty cycle (f = 500 kHz)	02			855	
I_{EE} supply current	I_{EE}	V_{EE} = -12 V V_{CC} = 5 V	0% duty cycle (non-transmitting)	03, 06 09	1, 2, 3		80	mA
			50% duty cycle (f = 1 MHz)) 9/				180	
			100% duty cycle (f = 1 MHz)) 9/				270	
		V_{EE} = -15 V V_{CC} = 5 V	0% duty cycle (non-transmitting)	01, 04 07			80	
			50% duty cycle (f = 1 MHz)) 9/				180	
			100% duty cycle (f = 1 MHz)) 9/				270	
Functional tests		See 4.4.1b		All	7, 8			

See footnotes at end of table.

TABLE IA. Electrical performance characteristics - Continued.

Test	Symbol	Test conditions 1/ -55 C T_C +125 C 4.5 V V_{DD} 5.5 V unless otherwise specified	Device type	Group A subgroups	Limits		Unit
					Min	Max	
Register write timing							
Address setup time 9/	t_a	V_{CC} = minimum See figure 5	All	9, 10, 11	0		ns
Data setup time 9/	t_b		All	9, 10, 11	10		
Data hold time 9/	t_c		All	9, 10, 11	8		
Address hold time 9/	t_d		All	9, 10, 11	8		
$\overline{CS}$ to $\overline{CS}$ 9/	t_e		All	9, 10, 11	105		
Access delay 9/ 11/ 12/	t_f		All	9, 10, 11	85		
RD/$\overline{WR}$ assertion to $\overline{CS}$ assertion 10/	t_g		All	9, 10, 11	0		
$\overline{CS}$ negation to RD/$\overline{WR}$ negation 10/	t_h		All	9, 10, 11	0		
$\overline{CS}$ assertion to output enable 9/	t_i		All	9, 10, 11	0	40	
$\overline{CS}$ negation to output three-state 10/	t_j		All	9, 10, 11	5	35	
Register read timing							
Address setup time 9/	t_a	V_{CC} = minimum See figure 5	All	9, 10, 11	0		ns
$\overline{CS}$ assertion to output enable data valid 9/	t_b		All	9, 10, 11		95	
$\overline{CS}$ negation to output disabled 10/	t_c		All	9, 10, 11	5	35	
Address hold time 9/	t_d		All	9, 10, 11	0		
$\overline{CS}$ assertion to output enable data invalid 9/	t_e		All	9, 10, 11	0	40	
Access delay 9/ 11/ 12/	t_f		All	9, 10, 11	45		
$\overline{CS}$ to $\overline{CS}$ 9/	t_g		All	9, 10, 11	105		
Memory write timing							
Address propagation delay	t_a	V_{CC} = minimum See figure 5	01, 02 03, 04 05, 06	9, 10, 11	0	18	ns
			07, 08 09	9, 10, 11	0	21	
Address valid to $\overline{RCS}$, $\overline{RWR}$ assertion 9/	t_b		All	9, 10, 11	15	35	

See footnotes at end of table.

TABLE IA. Electrical performance characteristics - Continued.

Test	Symbol	Test conditions 1/ -55 C T_C +125 C 4.5 V V_{DD} 5.5 V unless otherwise specified	Device type	Group A subgroups	Limits		Unit
					Min	Max	
Memory write timing - Continued							
$\overline{\text{DTACK}}$ setup time 9/	t_c	V_{CC} = minimum See figure 5	All	9, 10, 11	10		ns
$\overline{\text{RCS}}$ and $\overline{\text{RWR}}$ hold time 9/ 13/	t_d		All	9, 10, 11	20	50	
Data propagation delay 9/	t_e		All	9, 10, 11	20	60	
Address hold time 9/	t_g		All	9, 10, 11	10	30	
$\overline{\text{DTACK}}$ hold time 9/	t_h		All	9, 10, 11	10		
$\overline{\text{RWR}}$ and $\overline{\text{RCS}}$ pulse width ($\overline{\text{DTACK}}$ tied to ground)	t_i		01, 02 03, 04 05, 06	9, 10, 11	34		
			07, 08 09	9, 10, 11	32		
$\overline{\text{RWR}}$ and $\overline{\text{RCS}}$ to $\overline{\text{DMACK}}$ 10/	t_j		All	9, 10, 11	15	125	
Data hold time 10/	t_k		All	9, 10, 11	10	40	
Memory read timing							
Address propagation delay	t_a	V_{CC} = minimum See figure 5	01, 02 03, 04 05, 06	9, 10, 11	0	18	ns
			07, 08 09	9, 10, 11	0	21	
Address valid to $\overline{\text{RCS}}$, $\overline{\text{RRD}}$ assertion 9/	t_b		All	9, 10, 11	15	35	
$\overline{\text{DTACK}}$ setup time 9/	t_c		All	9, 10, 11	10		
$\overline{\text{RCS}}$ and $\overline{\text{RRD}}$ hold time 9/ 13/	t_d		All	9, 10, 11	20	50	
Data setup delay 9/	t_e		01, 02 03, 04 05, 06	9, 10, 11	12		
			07, 08 09	9, 10, 11	10		
Data hold delay	t_f		01, 02 03, 04 05, 06	9, 10, 11	0		
			07, 08 09	9, 10, 11	2		
Address hold time 9/	t_g		All	9, 10, 11	10	30	

See footnotes at end of table.

TABLE IA. Electrical performance characteristics - Continued.

Test	Symbol	Test conditions 1/ -55 C T_C +125 C 4.5 V V_{DD} 5.5 V unless otherwise specified		Device type	Group A subgroups	Limits		Unit
						Min	Max	
Memory read timing - Continued								
$\overline{\text{DTACK}}$ hold time	t_h	V_{CC} = minimum See figure 5		All	9, 10, 11	10		ns
$\overline{\text{RRD}}$ and $\overline{\text{RCS}}$ pulse width ($\overline{\text{DTACK}}$ tied to ground)	t_i			01, 02 03, 04 05, 06	9, 10, 11	34		
				07, 08 09	9, 10, 11	32		
$\overline{\text{RRD}}$ and $\overline{\text{RCS}}$ to $\overline{\text{DMACK}}$ 10/	t_j			All	9, 10, 11	15	45	
DMA timing								
$\overline{\text{TERACT}}$ assertion to $\overline{\text{DMAR}}$ assertion 9/	t_a	V_{CC} = minimum See figure 5		All	9, 10, 11	5		s
$\overline{\text{DMAR}}$ assertion to $\overline{\text{DMACK}}$ negation 9/	t_b		Bus controller	01, 02 03	9, 10, 11		7	
				04, 05 06, 07 08, 09	9, 10, 11		16	
			Remote terminal	All	9, 10, 11		7	
			Remote terminal with monitor	All	9, 10, 11		7	
			Monitor	All	9, 10, 11		7	
$\overline{\text{DMAG}}$ assertion to $\overline{\text{DMACK}}$ assertion 9/	t_c			01, 02 03, 04 05, 06	9, 10, 11	0	30	ns
				07, 08 09	9, 10, 11	5	30	
$\overline{\text{DMAG}}$ assertion to $\overline{\text{DMAR}}$ negation 10/	t_d			All	9, 10, 11	0	35	
$\overline{\text{DMACK}}$ assertion to address bus active	t_e			01, 02 03, 04 05, 06	9, 10, 11	0	5	
				07, 08 09	9, 10, 11	-5	5	
$\overline{\text{DMACK}}$ assertion to $\overline{\text{DMAG}}$ negation 9/	t_f			All	9, 10, 11	10		
$\overline{\text{DMACK}}$ negation to $\overline{\text{DMAR}}$ assertion 9/	t_g			All	9, 10, 11	500		

See footnotes at end of table.

TABLE IA. Electrical performance characteristics - Continued.

Test	Symbol	Test conditions 1/ -55 C T_C +125 C 4.5 V V_{DD} 5.5 V unless otherwise specified	Device type	Group A subgroups	Limits		Unit
					Min	Max	
DMA timing - Continued							
$\overline{\text{DMACK}}$ assertion to RAM control active (negated)	t_h	V_{CC} = minimum See figure 5	01, 02 03, 04 05, 06	9, 10, 11	0	5	ns
			07, 08 09		-5	5	
$\overline{\text{DMACK}}$ negation to address three-state 10/	t_i		All	9, 10, 11		5	
$\overline{\text{DMACK}}$ negation to RAM control disabled 10/	t_j		All	9, 10, 11		5	
Power-up master reset timing							
$\overline{\text{MRST}}$ pulse width 9/	t_a	V_{CC} = minimum See figure 5	All	9, 10, 11	500		ns
$\overline{\text{MRST}}$ negation to $\overline{\text{ROMEN}}$ assertion 9/	t_b		All	9, 10, 11		5	s
$\overline{\text{MRST}}$ negation to $\overline{\text{READY}}$ assertion 9/	t_c		All	9, 10, 11		10	s
$\overline{\text{DMACK}}$ negation to $\overline{\text{ROMEN}}$ negation 9/	t_d		All	9, 10, 11		500	ns
JTAG timing							
TCK frequency		See figure 5	All	9, 10, 11		1	MHz
TCK period	t_a		All	9, 10, 11	1000		ns
TCK high time	t_b		All	9, 10, 11	1/2t_a		
TCK low time	t_c		All	9, 10, 11	1/2t_a		
TCK rise time	t_d		All	9, 10, 11		5	
TCK fall time	t_e		All	9, 10, 11		5	
TDI, TMS setup time	t_f		All	9, 10, 11	250		
TDI, TMS hold time	t_g		All	9, 10, 11	250		
TDO valid delay	t_h		All	9, 10, 11	250		
Receiver electrical characteristics							
Differential (receiver) input impedance 10/	R_{IZ}	V_{CC} = minimum, see figure 5 Input f = 1 MHz (no transformer in circuit)	01, 03 04, 06 07, 09	1, 2, 3	15		k
Common mode input voltage 10/	V_{IC}	V_{CC} = minimum, see figure 5 Direct-coupled stub, input 1.2 V_{PP} , 200 ns rise/fall time 25 ns, f = 1 MHz	01, 03 04, 06 07, 09	1, 2, 3	-10	+10	V
			02, 05 08	1, 2, 3	-5	+5	
Common mode rejection ratio 10/	CMRR	V_{CC} = minimum, see figure 5	All	1, 2, 3	Pass/Fail 14/		N/A

See footnotes at end of table.

TABLE IA. Electrical performance characteristics - Continued.

Test	Symbol	Test conditions 1/ -55 C T_C +125 C 4.5 V V_{DD} 5.5 V unless otherwise specified	Device type	Group A subgroups	Limits		Unit
					Min	Max	
Receiver electrical characteristics - Continued							
Input threshold voltage (no response)	V_{TH1}	V_{CC} = minimum, see figure 5 Transformer-coupled stub, input at f = 1 MHz, rise/fall time 200 ns (receiver output 0 1 transition) 10/	All	1, 2, 3		0.20	$V_{PP,L-L}$
		V_{CC} = minimum, see figure 5 Direct-coupled stub, input at f = 1 MHz, rise/fall time 200 ns (receiver output 0 1 transition)	All	1, 2, 3		0.28	
Input threshold voltage (response)	V_{TH2}	V_{CC} = minimum, see figure 5 Transformer-coupled stub, input at f = 1 MHz, rise/fall time 200 ns (receiver output 0 1 transition) 10/	All	1, 2, 3	0.86	14.0	$V_{PP,L-L}$
		V_{CC} = minimum, see figure 5 Direct-coupled stub, input at f = 1 MHz, rise/fall time 200 ns (receiver output 0 1transition)	All	1, 2, 3	1.20	20.0 10/	
Differential input voltage level	V_{IDR}	V_{CC} = minimum, see figure 5	02	1, 2, 3		8.0	V_{P-P}
Transmitter electrical characteristics							
Output voltage swing	V_O	V_{CC} = minimum, see figure 5 Transformer-coupled stub, point A, input f = 1 MHz, R_L = 70 10/	All	1, 2, 3	18	27	$V_{PP,L-L}$
		V_{CC} = minimum, see figure 5 Direct-coupled stub, point A, input f = 1 MHz, R_L = 35	All	1, 2, 3	6.0	9	
		V_{CC} = minimum, see figure 5 Point A, input f = 1 MHz, R_L = 35 10/	All	1, 2, 3	6.0	20	
Output noise voltage differential 10/	V_{NS}	V_{CC} = minimum, see figure 5 Transformer-coupled stub, point A, input f = DC to 10 MHz, R_L = 70	All	1, 2, 3		14	mV-RMS_{L-L}
		V_{CC} = minimum, see figure 5 Direct-coupled stub, point A, input f = DC to 10 MHz, R_L = 35	All	1, 2, 3		5	

See footnotes at end of table.

TABLE IA. Electrical performance characteristics - Continued.

Test	Symbol	Test conditions 1/ -55 C T_C +125 C 4.5 V V_{DD} 5.5 V unless otherwise specified	Device type	Group A subgroups	Limits		Unit
					Min	Max	
Transmitter electrical characteristics - Continued							
Output symmetry 15/	V_{OS}	V_{CC} = minimum Transformer-coupled stub, point A, R_L = 70 , measurement taken 2.5 s after end of transmission 10/	All	1, 2, 3	-250	+250	$mV_{PP,L-L}$
		V_{CC} = minimum Direct-coupled stub, point A, R_L = 35 , measurement taken 2.5 s after end of transmission 16/	All	1, 2, 3	-90	+90	
Output voltage distortion (overshoot or ring)	V_{DIS}	V_{CC} = minimum, see figure 5 Transformer-coupled stub, point A, R_L = 70 10/	01, 03 04, 05 06, 07 08, 09	1, 2, 3	-900	+900	$mV_{peak,L-L}$
			02	1, 2, 3	-2.0	+2.0	$V_{peak,L-L}$
		V_{CC} = minimum, see figure 5 Direct-coupled stub, point A, R_L = 35 16/	01, 03 04, 05 06, 07 08, 09	1, 2, 3	-300	+300	$mV_{peak,L-L}$
			02	1, 2, 3	-1.0	+1.0	$V_{peak,L-L}$
Terminal input impedance 10/	T_{IZ}	V_{CC} = minimum, see figure 5 Transformer-coupled stub, point A, input f = 75 kHz to 1 MHz, (power on or power off, non-transmitting, R_L removed from circuit)	All	1, 2, 3	1		k
		V_{CC} = minimum, see figure 5 Direct-coupled stub, point A, input f = 75 kHz to 1 MHz, (power on or power off, non-transmitting, R_L removed from circuit)	All	1, 2, 3	2		
AC electrical characteristics							
Transmitter output rise/fall time	t_R, t_F	V_{CC} = minimum, see figure 5 Input f = 1 MHz 50% duty cycle: direct-coupled, R_L = 35 , output at 10% through 90% points TXOUT, $\overline{\text{TXOUT}}$	All	9, 10, 11	100	300	ns
Zero crossing distortion	t_{RZCD}	V_{CC} = minimum, see figure 5 Direct-coupled stuff, Input f = 1 MHz, 3 V_{PP} (skew input 150 ns), rise/fall time 200 ns	All	9, 10, 11	-150	+150	

See footnotes at end of table.

TABLE IA. Electrical performance characteristics - Continued.

Test	Symbol	Test conditions 1/ -55 C T_C +125 C 4.5 V V_{DD} 5.5 V unless otherwise specified	Device type	Group A subgroups	Limits		Unit
					Min	Max	
AC electrical characteristics - Continued							
Zero crossing stability	t_{TZCS}	V_{CC} = minimum, see figure 5 Input TXIN and $\overline{\text{TXIN}}$ should create transmitter output zero crossings at 500 ns, 1000 ns, 1500 ns, and 2000 ns. These zero crossings should not deviate more than 25 ns	All	9, 10, 11	-25	+25	ns

1/ Device type 04 supplied to this drawing will meet all levels M, D, L, R of irradiation. Device type 05 supplied to this drawing will meet all levels M, D, L, R, F, G, and H of irradiation. However, these devices are only tested at the 'R' and 'H' level, respectively. Pre and post irradiation values are identical unless otherwise specified in table IA. When performing post irradiation electrical measurements for any RHA level, T_A = +25 C. All testing to be performed using worst case test conditions unless otherwise specified. GND may not vary from 0 V by more than 50 mV. Unless otherwise specified, V_{CC} = 5.0 V 5% for device type 02; V_{CC} = 5.0 V 10% for device types 05 and 08; V_{CC} = 5.0 V +10%, -5% and V_{EE} = -12.0 V or -15.0 V 5% for device types 01, 03, 04, 06, 07, and 09.

2/ 24 MHz input only.

3/ The worst case test condition is when IOL and IOH = 4.0 mA.

4/ Supplied as a design limit but not guaranteed or tested.

5/ Not more than one output may be shorted at a time for maximum duration of one second.

6/ For all pins except CHA, $\overline{\text{CHA}}$, CHB, $\overline{\text{CHB}}$.

7/ All inputs tied to V_{DD}.

8/ Post irradiation limit is 1.0 mA.

9/ For device types 07, 08, and 09, this parameter is guaranteed, but not tested.

10/ Guaranteed by characterization but not tested.

11/ Read cycle followed by a read cycle - minimum 45 ns.
Read cycle followed by a write cycle - minimum 45 ns.
Write cycle followed by a read cycle - minimum 85 ns.
Write cycle followed by a write cycle - minimum 85 ns.

12/ Minimum pulse width from latter rising edge of RD/$\overline{\text{WR}}$ or $\overline{\text{CS}}$ to first falling edge.

13/ Pulse width duration is measured with respect to the device recognizing $\overline{\text{DTACK}}$ assertion.

14/ Pass/fail criteria per the test method described in MIL-STD-1553, appendix A. RT validation test plan, section 5.1.2.2, common mode rejection.

15/ Test in accordance with the method described in MIL-STD-1553B output symmetry, section 4.5.2.1.1.4.

16/ Tested on deivce types 07, 08, and 09 only.

TABLE IB. SEP test limits. 1/ 2/ 3/

Device type	T_A = Temperature 10 C 4/	V_{DD} = 4.5 V		Bias for latch-up test V_{DD} = 5.5 V no latch-up LET = 4/
		Effective LET no upsets [MeV/(mg/cm^2)]	Maximum device cross section LET = 120 (m^2)	
04, 05	+25 C	5/	5/	5/

1/ Devices that contain cross-coupled resistance must be tested at the maximum rated T_A.

2/ For SEP test conditions, see 4.4.4.5 herein.

3/ Technology characterization and model verification supplemented by in-line data may be used in lieu of end-of-line testing. Test plan must be approved by TRB and qualifying activity.

4/ Worst case temperature T_A = +125 C.

5/ Values will be added when they become available. These devices have not yet been tested for SEP.

Case X

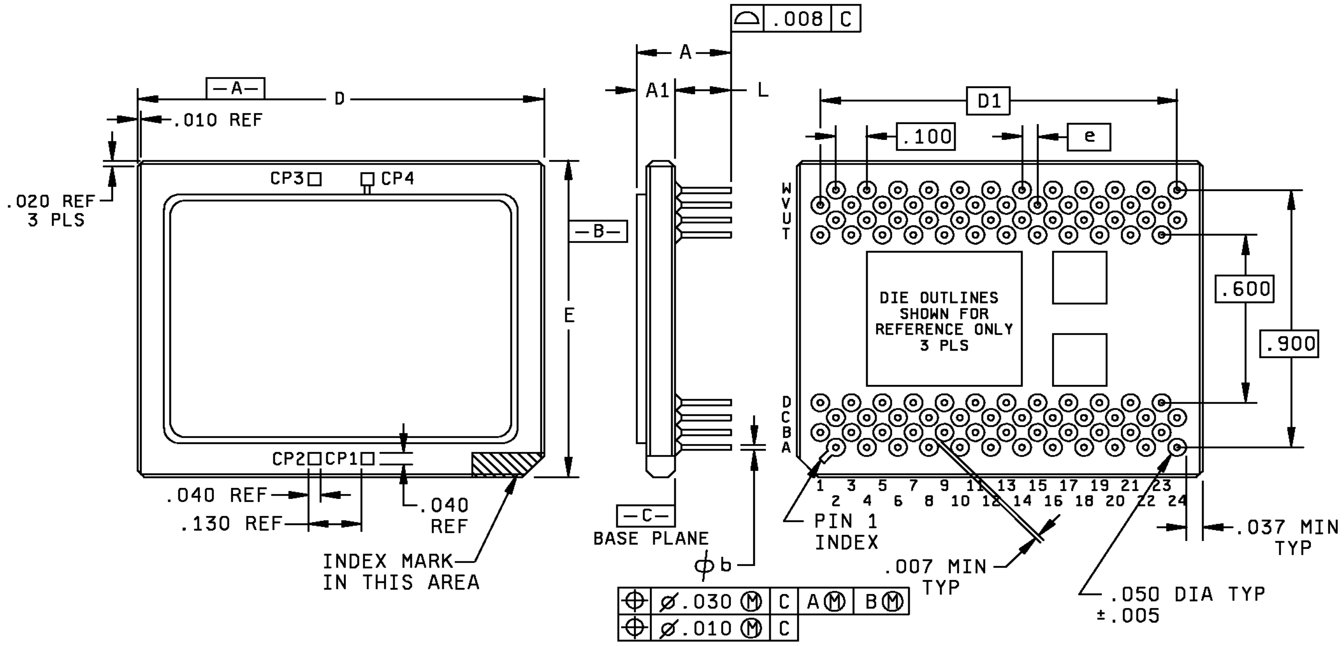


FIGURE 1. Case outlines.

Case X				
Symbol	Millimeters		Inches	
	Min	Max	Min	Max
A	6.85	8.00	.270	.315
A1	2.54	3.17	.100	.125
b	0.40	0.50	.016	.020
D	32.89	33.66	1.295	1.325
D1	29.21 BSC		1.150 BSC	
E	26.54	27.30	1.045	1.075
e	1.27 BSC		.050 BSC	
L	4.37	4.77	.172	.188

NOTE: The US Government preferred system of measurement is the metric SI system. However, this item was originally designed using inch-pound units of measurements. In the event of conflict between the metric and inch-pound units, the inch-pound units shall take precedence.

FIGURE 1. Case outlines - Continued.

Case Y

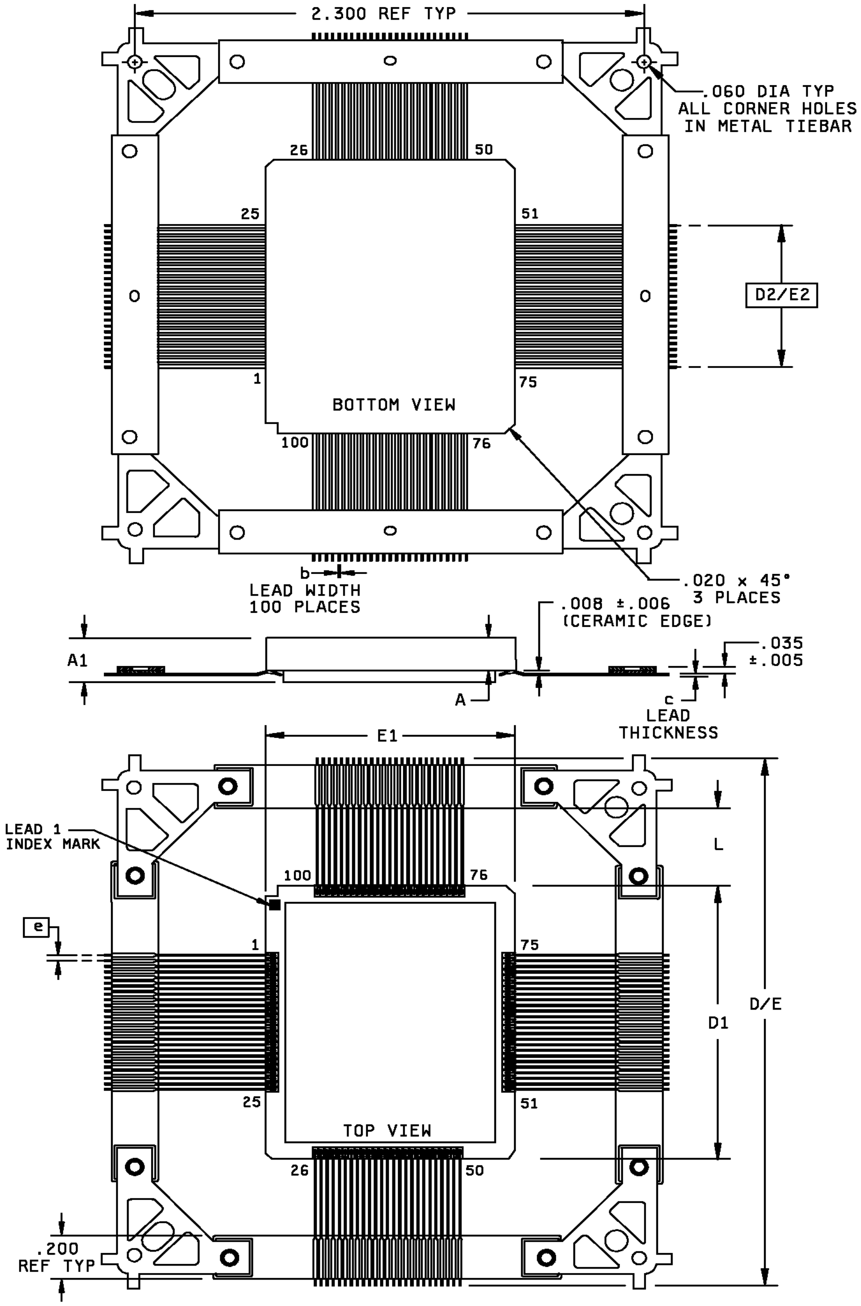


FIGURE 1. Case outlines - Continued.

Case Y				
Symbol	Millimeters		Inches	
	Min	Max	Min	Max
A		2.66		.105
A1	2.28	3.30	.090	.130
b	0.152	0.254	.006	.010
c	0.1270	0.1905	.0050	.0075
D/E		65.532		2.580
D1	33.91	34.67	1.335	1.365
D2/E2	15.24 BSC		.600 BSC	
E1	24.64	25.40	.970	1.000
e	0.635 BSC		.025 BSC	
L	13.34		.525	

NOTE: The US Government preferred system of measurement is the metric SI system. However, this item was originally designed using inch-pound units of measurements. In the event of conflict between the metric and inch-pound units, the inch-pound units shall take precedence.

FIGURE 1. Case outlines - Continued.

Device type	All						
Case outline	X						
Terminal number	Terminal symbol	Terminal number	Terminal symbol	Terminal number	Terminal symbol	Terminal number	Terminal symbol
A2	A15	C2	A12	T1	A3	V1	V_{SS}
A4	A14	C4	V_{DD}	T3	A4	V3	$\overline{\text{RRD}}$
A6	A13	C6	A8	T5	V_{DD}	V5	D14
A8	$\overline{\text{ROMEN}}$	C8	V_{SS}	T7	A6	V7	$\overline{\text{DTACK}}$
A10	$\overline{\text{CS}}$	C10	$\overline{\text{DMAG}}$	T9	24 MHz	V9	D13
A12	MSEL0	C12	$\overline{\text{YF\_INT}}$	T11	V_{SS}	V11	D15
A14	TCK	C14	TMS	T13	$\overline{\text{LOCK}}$	V13	D9
A16	TDI	C16	$\text{A}/\overline{\text{B}}$ STD	T15	$\overline{\text{READY}}$	V15	D10
A18	TDO	C18	$\overline{\text{CHB}}$	T17	GND	V17	D8
A20	RTA2	C20	GND	T19	V_{CC}	V19	D1
A22	RTA0	C22	CHB	T21	V_{EE} 1/	V21	D2
A24	GND	C24	V_{CC}	T23	V_{EE} 1/	V23	D0
B1	V_{DD}	D1	A9	U2	A1	W2	A5
B3	A11	D3	A7	U4	V_{DD}	W4	$\overline{\text{RWR}}$
B5	A10	D5	V_{SS}	U6	A2	W6	A0
B7	$\overline{\text{DMACK}}$	D7	V_{DD}	U8	V_{SS}	W8	TCLK
B9	$\overline{\text{AUTOEN}}$	D9	$\overline{\text{MSG\_INT}}$	U10	D12	W10	V_{DD}
B11	$\text{RD}/\overline{\text{WR}}$	D11	V_{SS}	U12	D11	W12	$\overline{\text{RCS}}$
B13	MSEL1	D13	$\overline{\text{DMAR}}$	U14	$\overline{\text{SSYSF}}$	W14	D5
B15	$\overline{\text{TRST}}$	D15	$\overline{\text{MRST}}$	U16	$\overline{\text{TERACT}}$	W16	D6
B17	RTA4	D17	GND	U18	$\overline{\text{CHA}}$	W18	D7
B19	RTA3	D19	V_{CC}	U20	GND	W20	D4
B21	RTA1	D21	V_{EE} 1/	U22	CHA	W22	D3
B23	RTPTY	D23	V_{EE} 1/	U24	V_{CC}	W24	GND
Terminal located on top of package							
CP1	V_{DDQ}	CP2	V_{SSQ}	CP3	V_{DD}	CP4	V_{SS}

1/ Device types 01, 03, 04, 06, 07, and 09 only. For device types 02, 05, and 08, this is a N/C (no connection).

FIGURE 2. Terminal connections.

Device type	All						
Case outline	Y						
Terminal number	Terminal symbol	Terminal number	Terminal symbol	Terminal number	Terminal symbol	Terminal number	Terminal symbol
1	$\overline{\text{DMACK}}$	26	A15	51	TDI	76	V_{DD}
2	$\overline{\text{DMAG}}$	27	V_{EE} 1/	52	TDO	77	V_{SS}
3	$\overline{\text{DMAR}}$	28	V_{EE} 1/	53	$\overline{\text{TRST}}$	78	$\overline{\text{ROMEN}}$
4	$\overline{\text{DTACK}}$	29	GND	54	RTPTY	79	$\overline{\text{AUTOEN}}$
5	V_{SS}	30	V_{CC}	55	RTA0	80	$\overline{\text{CS}}$
6	$\overline{\text{RRD}}$	31	GND	56	RTA1	81	RD/$\overline{\text{WR}}$
7	$\overline{\text{RWR}}$	32	CHA	57	RTA2	82	D0
8	$\overline{\text{RCS}}$	33	$\overline{\text{CHA}}$	58	RTA3	83	D1
9	V_{DD}	34	GND	59	RTA4	84	D2
10	V_{SS}	35	V_{CC}	60	V_{DD}	85	D3
11	A0	36	V_{CC}	61	V_{SS}	86	D4
12	A1	37	GND	62	V_{DD}	87	D5
13	A2	38	GND	63	$\overline{\text{TERACT}}$	88	D6
14	A3	39	V_{CC}	64	$\overline{\text{READY}}$	89	D7
15	A4	40	V_{CC}	65	$\overline{\text{MSG\_INT}}$	90	D8
16	A5	41	GND	66	$\overline{\text{YF\_INT}}$	91	D9
17	A6	42	CHB	67	V_{SS}	92	D10
18	A7	43	$\overline{\text{CHB}}$	68	TCLK	93	D11
19	A8	44	GND	69	$\overline{\text{LOCK}}$	94	D12
20	A9	45	V_{CC}	70	A/$\overline{\text{B}}$ STD	95	D13
21	A10	46	GND	71	MSEL0	96	D14
22	A11	47	V_{EE} 1/	72	MSEL1	97	D15
23	A12	48	V_{EE} 1/	73	$\overline{\text{MRST}}$	98	V_{SS}
24	A13	49	TCK	74	24 MHz	99	V_{DD}
25	A14	50	TMS	75	$\overline{\text{SSYSF}}$	100	V_{DD}

1/ Device types 01, 03, 04, 06, 07, and 09 only. For device types 02, 05, and 08, this is a N/C (no connection).

FIGURE 2. Terminal connections - Continued.

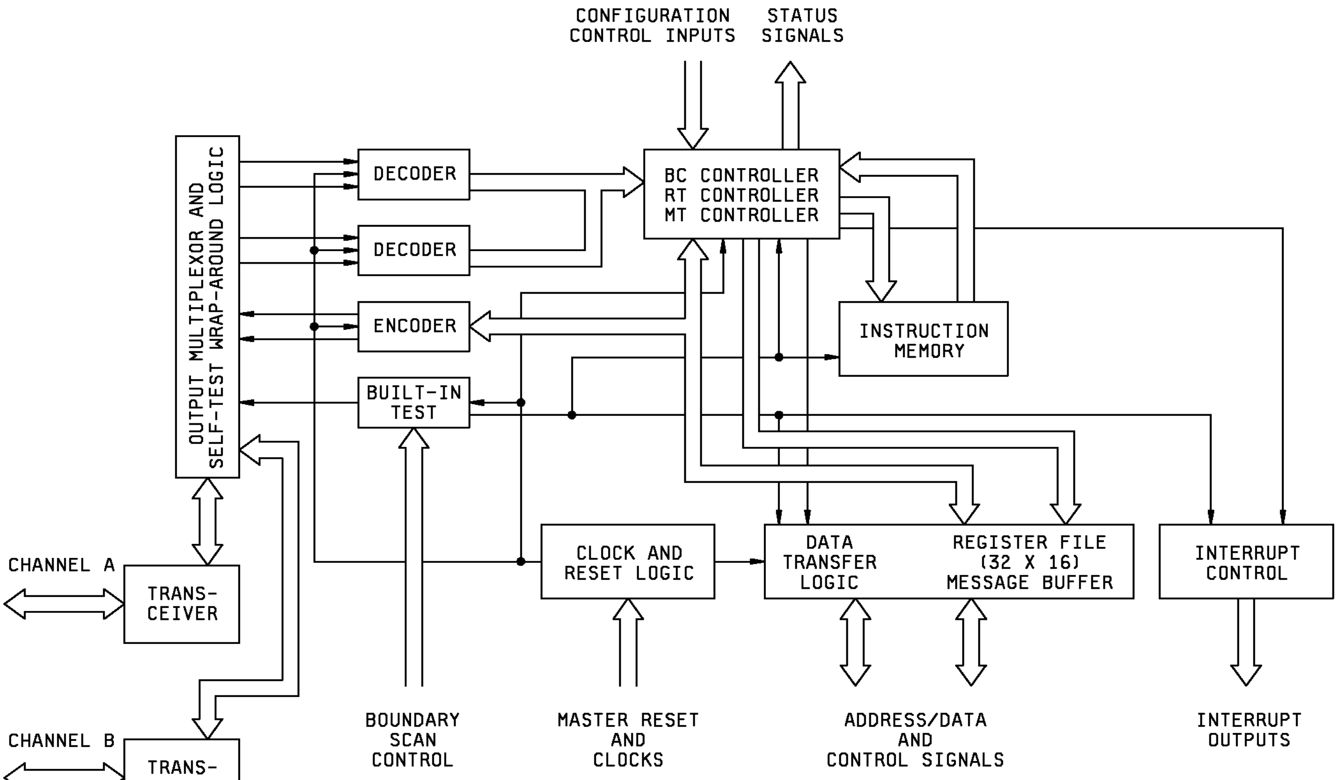
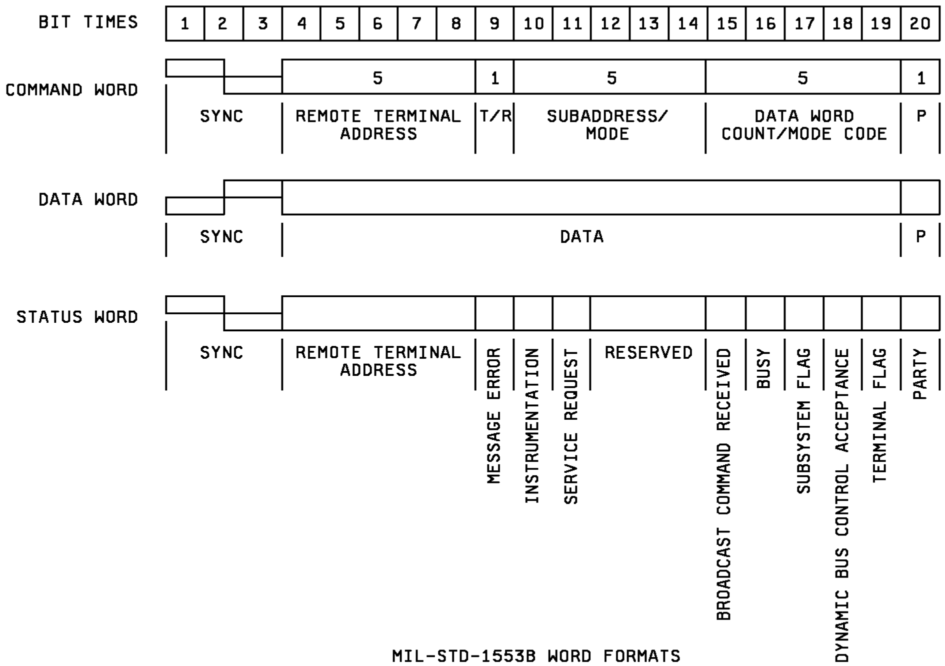


FIGURE 3. Block diagram.

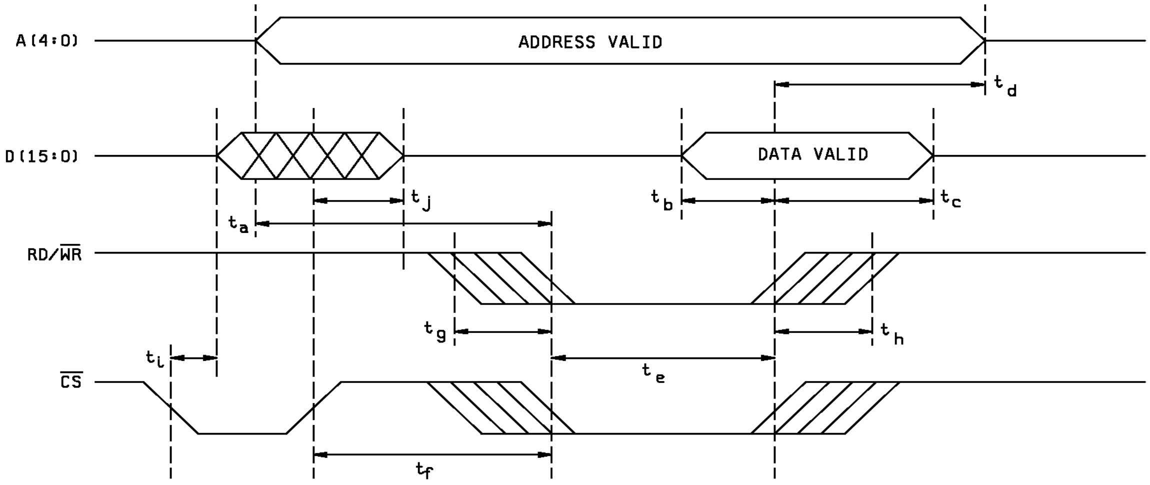
Device types 01, 02, 03, 04, 05, 06	
Instruction name	Instruction code
BYPASS	1111
SAMPLE/PRELOAD	0010
EXTEST	0000
INTEST	0001
RUNBIST	0111
IDCODE	0100
GL-TRISTATE	0011
INTERNAL-SCAN	0101
PRIVATE	0110
USER-SELECTABLE	1000 1110

Device types 07, 08, 09	
Instruction name	Instruction code
BYPASS	1111
SAMPLE/PRELOAD	0010
EXTEST	0000

FIGURE 4. Boundary scan instruction codes.

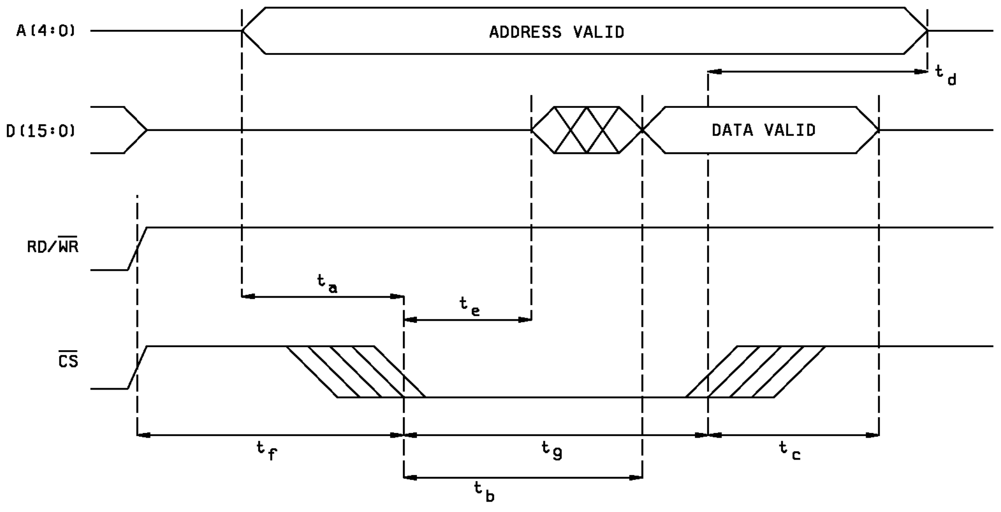


MIL-STD-1553B WORD FORMATS

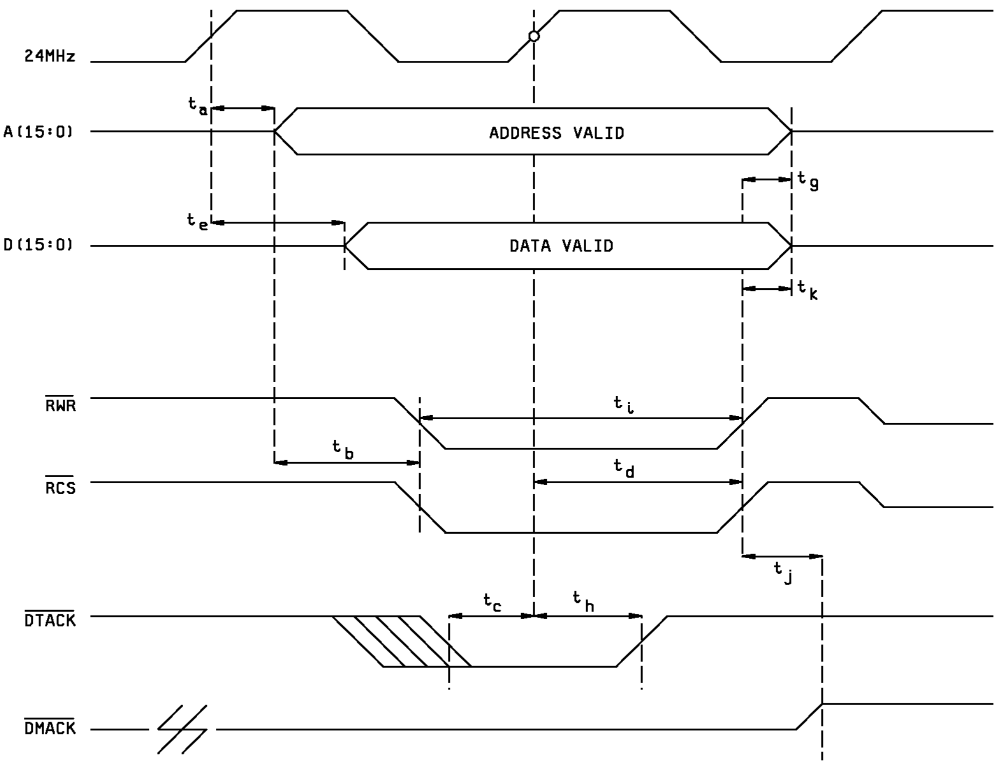


REGISTER WRITE TIMING

FIGURE 5. Timing waveforms.

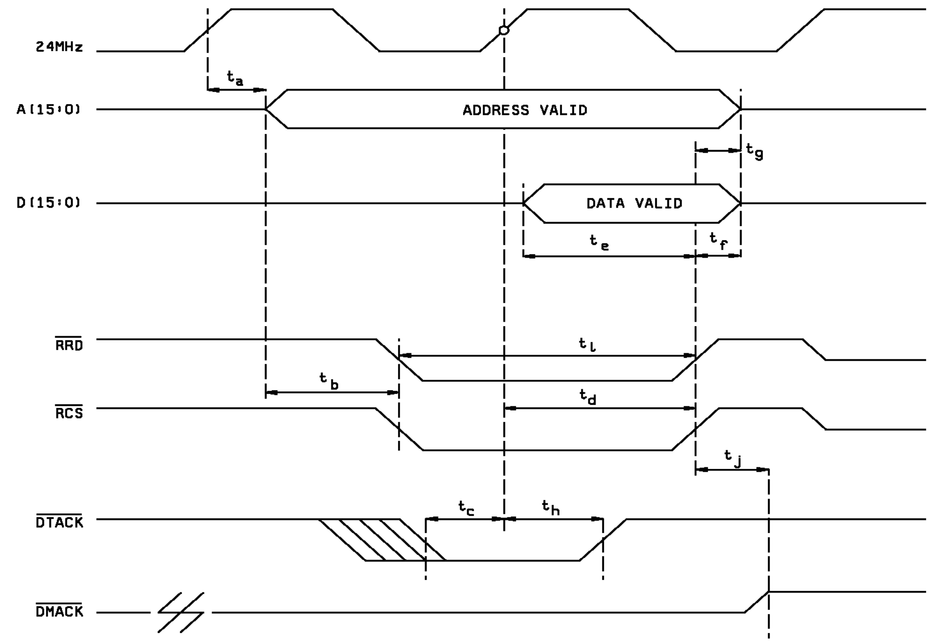


REGISTER READ TIMING

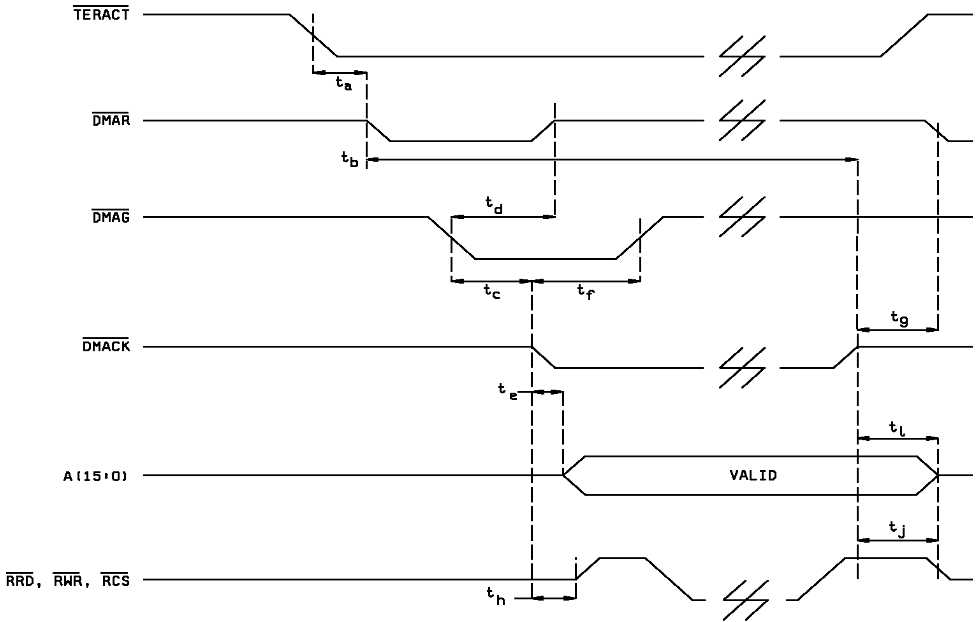


MEMORY WRITE TIMING

FIGURE 5. Timing waveforms - Continued.

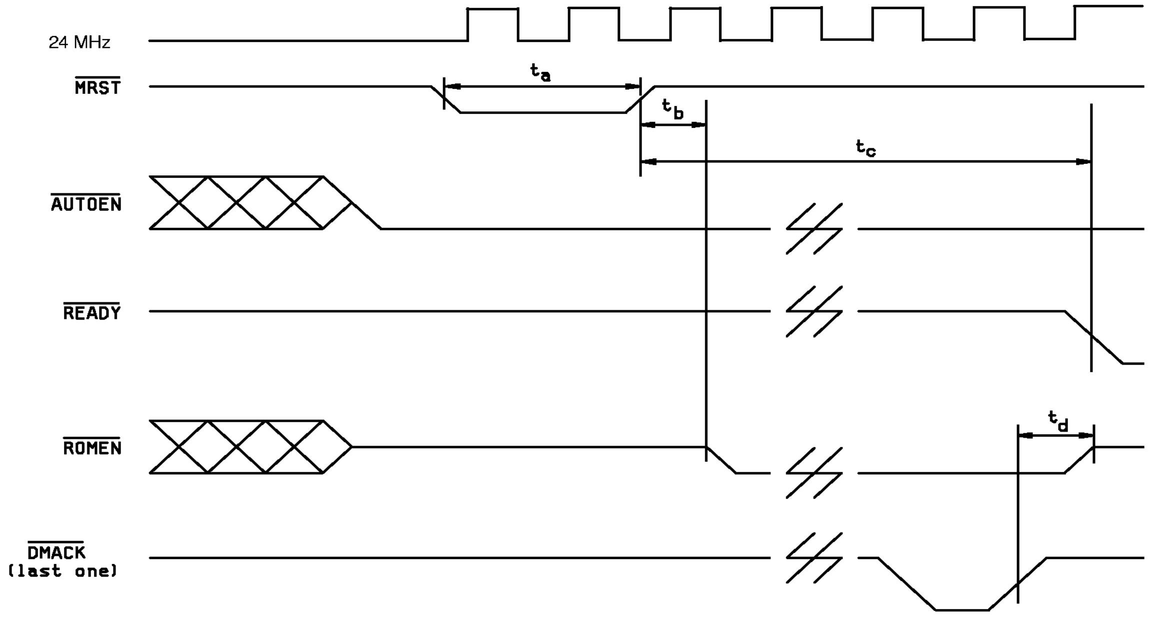


MEMORY READ TIMING

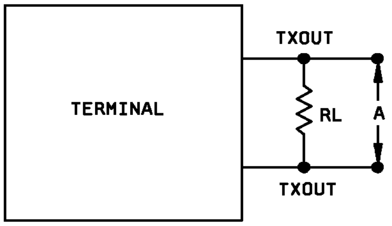


DMA TIMING

FIGURE 5. Timing waveforms - Continued.



POWER-UP MASTER RESET TIMING

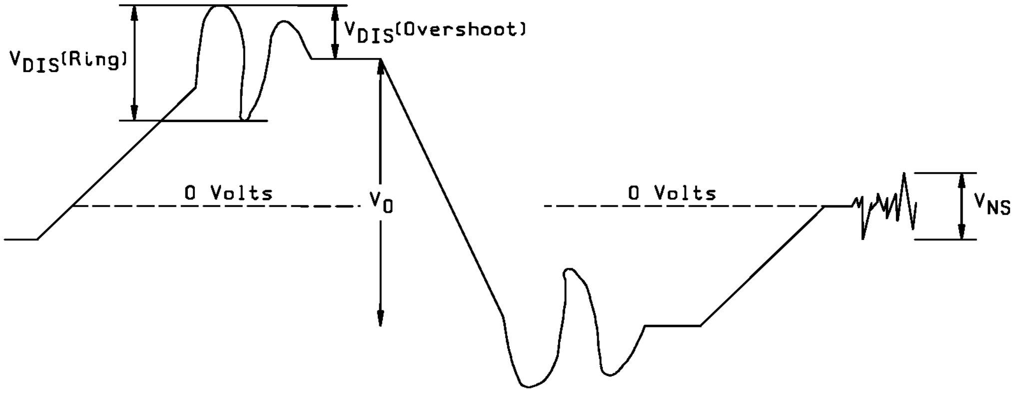


TRANSCEIVER TEST CIRCUIT MIL-STD-1553B

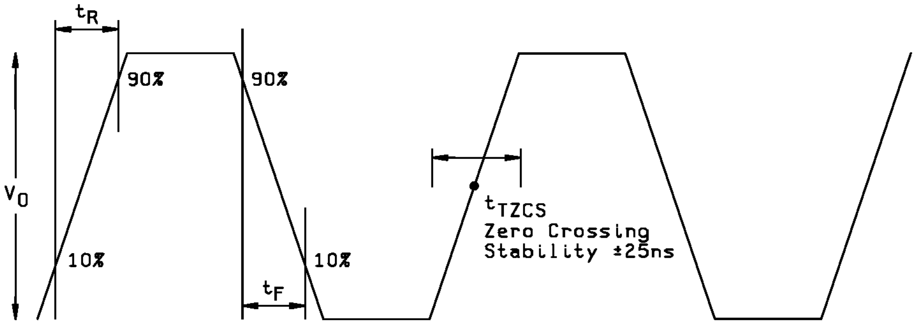
NOTES:

1. Transformer coupled stub:
   Terminal is defined as transceiver plus isolation transformer.
2. Direct coupled stub:
   Terminal is defined as transceiver plus isolation transformer and fault resistors.

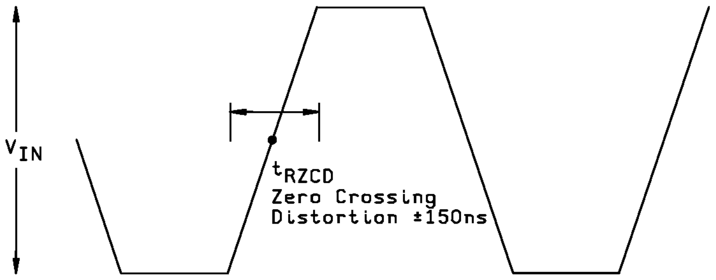
FIGURE 5. Timing waveforms - Continued.



TRANSMITTER OUTPUT CHARACTERISTICS(V_{DIS}, V_{NS}, V_O)



TRANSMITTER OUTPUT ZERO CROSSING STABILITY(t_{TZCS}, t_R, t_F)



RECEIVER INPUT ZERO CROSSING DISTORTION(t_{RZCD})

FIGURE 5. Timing waveforms - Continued.

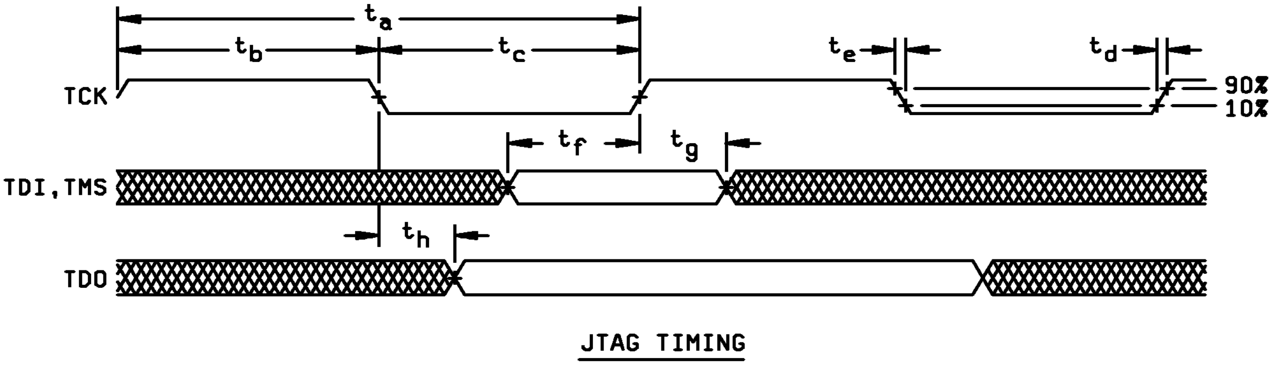


FIGURE 5. Timing waveforms - Continued.

Case outline	Open	V_{CC} = 5.5 V	V_{DD} = 5.5 V	V_{EE} = -15 V 1/	Ground
X	A2, A4, A6, A8, A18, B3, B5, B7, C2, C6, C12, C18, C22, D1, D3, D9, D13, T7, T15, U16, U18, U22, V3, W2, W4, W12	C24, D19, T19, U24	A10, A12, A14, A16, A20, A22, B1, B9, B11, B13, B15, B17, B19, B21, B23, C4, C10, C14, C16, D7, D15, T1, T3, T5, T9, T13, U2, U4, U6, U10, U12, U14, V5, V7, V9, V11, V13, V15, V17, V19, V21, V23, W6, W8, W10, W14, W16, W18, W20, W22	D21, D23, T21, T23	A24, C8, C20, D5, D11, D17, T11, T17, U8, U20, V1, W24
Y	1, 3, 6, 7, 8, 16, 17, 18, 19, 20, 21, 22, 23, 24, 25, 26, 32, 33, 42, 43, 52, 63, 64, 65, 66, 78	30, 35, 36, 39, 40, 45	2, 4, 9, 11, 12, 13, 14, 15, 49, 50, 51, 53, 54, 55, 56, 57, 58, 59, 60, 62, 68, 69, 70, 71, 72, 73, 74, 75, 76, 79, 80, 81, 82, 83, 84, 85, 86, 87, 88, 89, 90, 91, 92, 93, 94, 95, 96, 97, 99, 100	27, 28, 47, 48	5, 10, 29, 31, 34, 37, 38, 41, 44, 46, 61, 67, 77, 98

1/ For device types 01, 03, 04, 06, and 07 only. For device types 02, 05, and 08, these pins are open.

FIGURE 6. Radiation exposure connections.

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. For device classes Q and V, sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein. For device class M, sampling and inspection procedures shall be in accordance with MIL-PRF-38535, appendix A.

4.2 Screening. For device classes Q and V, screening shall be in accordance with MIL-PRF-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection. For device class M, screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection.

4.2.1 Additional criteria for device class M.

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition A, B, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015.

(2) T_A = +125 C, minimum.

b. Interim and final electrical test parameters shall be as specified in table IIA herein.

4.2.2 Additional criteria for device classes Q and V.

a. The burn-in test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The burn-in test circuit shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015 of MIL-STD-883.

b. Interim and final electrical test parameters shall be as specified in table IIA herein.

c. Additional screening for device class V beyond the requirements of device class Q shall be as specified in MIL-PRF-38535, appendix B.

4.3 Qualification inspection for device classes Q and V. Qualification inspection for device classes Q and V shall be in accordance with MIL-PRF-38535. Inspections to be performed shall be those specified in MIL-PRF-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4 Conformance inspection. Technology conformance inspection for classes Q and V shall be in accordance with MIL-PRF-38535 including groups A, B, C, D, and E inspections and as specified herein except where option 2 of MIL-PRF-38535 permits alternate in-line control testing. Quality conformance inspection for device class M shall be in accordance with MIL-PRF-38535, appendix A and as specified herein. Inspections to be performed for device class M shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4.1 Group A inspection.

a. Tests shall be as specified in table IIA herein.

b. For device class M, subgroups 7 and 8 tests shall be sufficient to verify the functionality of the device. For device classes Q and V, subgroups 7 and 8 shall include verifying the functionality of the device; these tests shall have been fault graded in accordance with MIL-STD-883, test method 5012 (see 1.5 herein).

c. Subgroup 4 (C_{IN}, C_{OUT}, and C_{IO}) shall be measured only for the initial test and after process or design changes which may affect input capacitance. A minimum sample of 5 devices with zero failures shall be required.

TABLE IIA. Electrical test requirements.

Test requirements	Subgroups (in accordance with MIL-STD-883, method 5005, table I)	Subgroups (in accordance with MIL-PRF-38535, table III)	
	Device class M	Device class Q	Device class V
Interim electrical parameters (see 4.2)	---	---	---
Final electrical parameters (see 4.2)	1, 2, 3, 7, 8, 9, 10, 11 1/	1, 2, 3, 7, 8, 9, 10, 11 1/	1, 2, 3, 7, 8, 9, 10, 11 2/ 3/
Group A test requirements (see 4.4)	1, 2, 3, 4, 7, 8, 9, 10, 11	1, 2, 3, 4, 7, 8, 9, 10, 11	1, 2, 3, 4, 7, 8, 9, 10, 11
Group C end-point electrical parameters (see 4.4)	1, 7, 9	1, 7, 9	1, 7, 9
Group D end-point electrical parameters (see 4.4)	1, 7, 9	1, 7, 9	1, 7, 9
Group E end-point electrical parameters (see 4.4)	1, 7, 9	1, 7, 9	1, 7, 9

1/ PDA applies to subgroup 1.

2/ PDA applies to subgroups 1 and 7.

3/ Delta limits, as specified in table IIB herein, shall be required when specified and the delta values shall be completed with reference to the zero hour electrical parameters.

TABLE IIB. Burn-in and operating life test, delta parameters (+25 C).

Parameter	Symbol	Delta limits
Quiescent current	I_{DDQ}	10% of measured values or 35 A whichever is greater

NOTE: If the device is tested at or below 35 A, no deltas are required.

4.4.2 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table IIA herein.

4.4.2.1 Additional criteria for device class M. Steady-state life test conditions, method 1005 of MIL-STD-883:

a. Test condition A, B, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005 of MIL-STD-883.

b. T_A = +125 C, minimum.

c. Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

4.4.2.2 Additional criteria for device classes Q and V. The steady-state life test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The test circuit shall be maintained under document revision level control by the device manufacturer's TRB in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005 of MIL-STD-883.

4.4.3 Group D inspection. The group D inspection end-point electrical parameters shall be as specified in table IIA herein.

4.4.4 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein). RHA levels for device classes M, Q and V shall be as specified in MIL-PRF-38535. End-point electrical parameters shall be as specified in table IIA herein.

4.4.4.1 Total dose irradiation testing. Total dose irradiation testing shall be performed in accordance with MIL-STD-883 method 1019 and as specified herein.

4.4.4.1.1 Accelerated aging test. Accelerated aging tests shall be performed on all devices requiring a RHA level greater than 5k rads(Si). The post-anneal end-point electrical parameter limits shall be as specified in table IA herein and shall be the pre-irradiation end-point electrical parameter limit at 25 C 5 C. Testing shall be performed at initial qualification and after any design or process changes which may affect the RHA response of the device.

4.4.4.2 Neutron testing. Neutron testing shall be performed in accordance with test method 1017 of MIL-STD-883 and herein (see 1.4). All device classes must meet the post irradiation end-point electrical parameter limits as defined in table IA, for the subgroups specified in table IIA herein at T_A = +25 C 5 C after an exposure of 2 x 10^{12} neutron/cm^2 (minimum).

4.4.4.3 Dose rate induced latchup testing. Dose rate induced latchup testing shall be performed in accordance with test method 1020 of MIL-STD-883 and as specified herein (see 1.4). Tests shall be performed on devices, SEC, or approved test structures at technology qualification and after any design or process changes which may effect the RHA capability of the process.

4.4.4.4 Dose rate upset testing. Dose rate upset testing shall be performed in accordance with test method 1021 of MIL-STD-883 and herein (see 1.4).

a. Transient dose rate upset testing shall be performed at initial qualification and after any design or process changes which may effect the RHA performance of the devices. Test 10 devices with 0 defects unless otherwise specified.

b. Transient dose rate upset testing for class Q and V devices shall be performed as specified by a TRB approved radiation hardness assurance plan and MIL-PRF-38535.

4.4.4.5 Single event phenomena (SEP). SEP testing shall be required on class V devices (see 1.4). SEP testing shall be performed on the Standard Evaluation Circuit (SEC) or alternate SEP test vehicle as approved by the qualifying activity at initial qualification and after any design or process changes which may affect the upset or latchup characteristics. The recommended test conditions for SEP are as follows:

a. The ion beam angle of incidence shall be between normal to the die surface and 60 to the normal, inclusive (i.e. 0 angle 60). No shadowing of the ion beam due to fixturing or package related effects is allowed.

b. The fluence shall be 100 errors or 10^6 ions/cm^2.

c. The flux shall be between 10^2 and 10^5 ions/cm^2/s. The cross-section shall be verified to be flux independent by measuring the cross-section at two flux rates which differ by at least an order of magnitude.

d. The particle range shall be 20 microns in silicon.

e. The test temperature shall be +25 C and the maximum rated operating temperature 10 C.

f. Bias conditions shall be defined by the manufacturer for latchup measurements.

g. Test four devices with zero failures.

h. For SEP test limits, see table IB herein.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535 for device classes Q and V or MIL-PRF-38535, appendix A for device class M.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.1.2 Substitutability. Device class Q devices will replace device class M devices.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished in accordance with MIL-STD-973 using DD Form 1692, Engineering Change Proposal.

6.3 Record of users. Military and industrial users should inform Defense Supply Center Columbus when a system application requires configuration control and which SMD's are applicable to that system. DSCC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DSCC-VA, telephone (614) 692-0525.

6.4 Comments. Comments on this drawing should be directed to DSCC-VA , Columbus, Ohio 43216-5000, or telephone (614) 692-0674.

6.5 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535, MIL-HDBK-1331, and table III herein.

6.6 Sources of supply.

6.6.1 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in QML-38535. The vendors listed in QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DSCC-VA and have agreed to this drawing.

6.6.2 Approved sources of supply for device class M. Approved sources of supply for class M are listed in MIL-HDBK-103. The vendors listed in MIL-HDBK-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DSCC-VA.

6.7 Additional information. A copy of the following additional data shall be maintained and available from the device manufacturer:

a. RHA upset levels.

b. Test conditions (SEP).

c. Number of upsets (SEP).

d. Number of transients (SEP).

e. Occurrence of latchup (SEP).

TABLE III. Pin descriptions.

Name	Type 1/	Active 2/	Description
Data bus			
D0	TTB	--	Bit 0 (LSB) of the bi-directional Data bus.
D1	TTB	--	Bit 1 of the bi-directional Data bus.
D2	TTB	--	Bit 2 of the bi-directional Data bus.
D3	TTB	--	Bit 3 of the bi-directional Data bus.
D4	TTB	--	Bit 4 of the bi-directional Data bus.
D5	TTB	--	Bit 5 of the bi-directional Data bus.
D6	TTB	--	Bit 6 of the bi-directional Data bus.
D7	TTB	--	Bit 7 of the bi-directional Data bus.
D8	TTB	--	Bit 8 of the bi-directional Data bus.
D9	TTB	--	Bit 9 of the bi-directional Data bus.
D10	TTB	--	Bit 10 of the bi-directional Data bus.
D11	TTB	--	Bit 11 of the bi-directional Data bus.
D12	TTB	--	Bit 12 of the bi-directional Data bus.
D13	TTB	--	Bit 13 of the bi-directional Data bus.
D14	TTB	--	Bit 14 of the bi-directional Data bus.
D15	TTB	--	Bit 15 (MSB) of the bi-directional Data bus.
Address bus			
A0	TTB	--	Bit 0 (LSB) of the bi-directional Address bus.
A1	TTB	--	Bit 1 of the bi-directional Address bus.
A2	TTB	--	Bit 2 of the bi-directional Address bus.
A3	TTB	--	Bit 3 of the bi-directional Address bus.
A4	TTB	--	Bit 4 of the bi-directional Address bus.
A5	TTO	--	Bit 5 of the Address bus.
A6	TTO	--	Bit 6 of the Address bus.
A7	TTO	--	Bit 7 of the Address bus.
A8	TTO	--	Bit 8 of the Address bus.
A9	TTO	--	Bit 9 of the Address bus.
A10	TTO	--	Bit 10 of the Address bus.
A11	TTO	--	Bit 11 of the Address bus.
A12	TTO	--	Bit 12 of the Address bus.
A13	TTO	--	Bit 13 of the Address bus.
A14	TTO	--	Bit 14 of the Address bus.
A15	TTO	--	Bit 15 (MSB) of the Address bus.

See footnotes at end of table.

TABLE III. Pin descriptions - Continued.

Name	Type 1/	Active 2/	Description
Remote terminal address inputs			
RTA0	TUI	--	Remote Terminal Address bit 0. This is bit 0 of the RT address. This is the least significant bit for the RT address.
RTA1	TUI	--	Remote Terminal Address bit 1. This is bit 1 of the RT address.
RTA2	TUI	--	Remote Terminal Address bit 2. This is bit 2 of the RT address.
RTA3	TUI	--	Remote Terminal Address bit 3. This is bit 3 of the RT address.
RTA4	TUI	--	Remote Terminal Address bit 4. This is the most significant bit of the RT address.
RTPTY	TUI	--	Remote Terminal Parity. This is an odd parity input for the RT address.
JTAG testability pins			
TDO	TTO	--	TDO. This output performs the operation of Test Data Output as defined in the IEEE Standard 1149.1. This cell provides the output signal for the Test Access Port (TAP). This non-inverting output buffer is optimized for driving TTL loads.
TCK	TI	--	TCK. This input performs the operation of Test Clock input as defined in the IEEE Standard 1149.1. This cell provides the input clock for non-inverting input buffer that is optimized for driving TTL input levels.
TMS	TUI	--	TMS. This input performs the operation of Test Mode Select as defined in the IEEE Standard 1149.1. This cell provides the input signal for the Test Access Port (TAP). This non-inverting input buffer is optimized for driving TTL input levels.
TDI	TUI	--	TDI. This input performs the operation of Test Data In as defined in the IEEE Standard 1149.1. This cell provides the input signal for the Test Access Port (TAP). This non-inverting input buffer is optimized for driving TTL input levels.
$\overline{\text{TRST}}$	TUI	AL	$\overline{\text{TRST}}$. This input provides the RESET to the TAP controller as defined in the IEEE Standard 1149.1. This non-inverting input buffer is optimized for driving TTL input levels. When not exercising JTAG, tie $\overline{\text{TRST}}$ to a logical 0.
Biphase inputs/outputs			
CHA	DIO	--	Channel A (true). This is the Manchester-encoded true signal for channel A.
$\overline{\text{CHA}}$	DIO	--	Channel A (complement). This is the Manchester-encoded complement signal for channel A.
CHB	DIO	--	Channel B (true). This is the Manchester-encoded true signal for channel B.
$\overline{\text{CHB}}$	DIO	--	Channel B (complement). This is the Manchester-encoded complement signal for channel B.
DMA signals			
$\overline{\text{DMAR}}$	TTO 3/	AL	DMA Request. This signal is asserted when access to RAM is required. It goes inactive upon request of the $\overline{\text{DMAG}}$ signal.
$\overline{\text{DMAG}}$	TI	AL	DMA Grant. Once this input is received, the device is allowed to access RAM.
$\overline{\text{DMACK}}$	TTO 3/	AL	DMA Acknowledge. This signal is asserted by the device to indicate the receipt of $\overline{\text{DMAG}}$. The signal remains active until all RAM bus activity is completed.
$\overline{\text{DTACK}}$	TI	AL	Data Transfer Acknowledge. This pin indicates that a data transfer is to occur and that the device may complete the memory cycle.

See footnotes at end of table.

TABLE III. Pin descriptions - Continued.

Name	Type 1/	Active 2/	Description
Control signals			
RD/$\overline{\text{WR}}$	TI	--	Read/Write. This indicates the direction of data flow with respect to the host. A logic high signal means the host is trying to read data from the device, and a logic low signal means the host is trying to write data to the device.
$\overline{\text{CS}}$	TI	AL	Chip Select. This pin selects the device when accessing the internal registers.
$\overline{\text{RRD}}$	TTO	AL	RAM Read. This signal is generated by the device to read data from RAM.
$\overline{\text{RWR}}$	TTO	AL	RAM Write. This signal is generated by the device to write data to RAM.
$\overline{\text{RCS}}$	TTO	AL	RAM Chip Select. This signal is used in conjunction with the $\overline{\text{RRD}}$ / $\overline{\text{RWR}}$ signal to access RAM.
$\overline{\text{AUTOEN}}$	TI	AL	Auto Enable. This pin, when active, enables automatic initialization.
$\overline{\text{ROMEN}}$	TTO 3/	AL	ROM Enable. This pin, when active enables the ROM for automatic initialization applications.
$\overline{\text{SSYSF}}$	TI	AL	Subsystem Fail. Upon receipt, this signal propagates directly to the RT 1553 status word.
24 MHz	CI	--	24 MHz Clock. This 24 MHz input clock requires a 50% 10% duty cycle with an accuracy of 0.01%.
$\overline{\text{MRST}}$	TUI	AL	Master Reset. This input pin resets the internal encoders, decoders, all register, and associated logic.
MSEL1	TI	--	Mode Select 1. This pin is the most significant bit for the mode select. For proper mode selection, see below: MSEL1 — MSEL0 — Mode of Operation 0 — 0 — Bus Controller = SBC 0 — 1 — Remote Terminal = SRT 1 — 0 — Monitor Terminal = SMT 1 — 1 — SMT/SRT
MSEL0	TI	--	Mode Select 0. This pin is the least significant bit for the mode select. (See MSEL1 for proper logic states.)
TCLK	TI	--	Timer Clock. This internal timer is a 16-bit counter with a 64 s resolution when using the 24 MHz input clock. For different applications, the user may input a clock (0-60 MHz) to establish the timer resolution. (Duty Cycle = 50% 10%).
A/$\overline{\text{B}}$ STD	TI	--	Military Standard A or B. This pin defines whether the device will be used a MIL-STD-1553A or 1553B mode of operation.
$\overline{\text{LOCK}}$	TI	AL	Lock. This pin, when set active, prevents software changes to both the RT address, A/$\overline{\text{B}}$ STD, and mode select.

See footnotes at end of table.

TABLE III. Pin descriptions - Continued.

Name	Type 1/	Active 2/	Description
Status signals			
$\overline{\text{TERACT}}$	TO	AL	Terminal Active. This output pin indicates that the terminal is actively processing a 1553 command.
$\overline{\text{MSG\_INT}}$	TTO 3/	AL	Message Interrupt. This pin is active for three clock cycles (i. e., 125 ns pulse) upon the occurrence of interrupt events which are enabled.
$\overline{\text{YF\_INT}}$	TTO 3/	AL	You Failed Interrupt. This pin is active for three clock cycles (i. e., 125 ns pulse) upon the occurrence of interrupt events which are enabled.
$\overline{\text{READY}}$	TO	AL	Ready. This signal indicates the device has completed initialization or BIT, and regular execution may begin.
Power/Ground			
V_{DD}	--	--	+5 volt logic power (10%)
V_{CC}	--	--	Device types 01, 03, 04, 06, 07, and 09: +5 volt transceiver power (+10%, -5%). Recommended de-coupling capacitors: 4.7 F and 0.1 F. Device type 02: +5 volt transceiver power (5%). Device types 05 and 08: +5 volt transceiver power (10%). Recommended de-coupling capacitors: 4.7 F and 0.1 F.
V_{EE}	--	--	Device types 01, 03, 04, 06, 07, and 09 only: -12 or -15 volt transceiver power (5%). Recommended de-coupling capacitors: 4.7 F and 0.1 F.
V_{SS}	--	--	Digital ground.
GND	--	--	Transceiver ground.

1/ TO = TTL output
TTB = Three-state TTL bi-directional
CI = CMOS input
TUI = TTL input (internally pulled high)
TI = TTL input
TTO = Three-state TTL output
DIO = Differential input/output
All pins specified as TTL are actually CMOS transistor pairs designed for TTL compatibility.

2/ AH = Active high
AL = Active low

3/ High impedance and active low.

STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 99-04-28

Approved sources of supply for SMD 5962-94663 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DSCC-VA. This bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962-9466301QXA	3/	
5962-9466301QYA	3/	
5962-9466301QXC	3/	
5962-9466301QYC	3/	
5962-9466302QXA	3/	
5962-9466302QYA	3/	
5962-9466302QXC	3/	
5962-9466302QYC	3/	
5962-9466303QXA	3/	
5962-9466303QYA	3/	
5962-9466303QXC	3/	
5962-9466303QYC	3/	
5962-9466304QXA	3/	
5962-9466304QYA	3/	
5962-9466304QXC	3/	
5962-9466304QYC	3/	
5962R9466304QXA	65342	UT69151LXE15/GQAR
5962R9466304QYA	65342	UT69151LXE15/WQAR
5962R9466304QXC	65342	UT69151LXE15/GQCR
5962R9466304QYC	65342	UT69151LXE15/WQCR
5962R9466304VXA	65342	UT69151LXE15/GVAR
5962R9466304VYA	65342	UT69151LXE15/WVAR
5962R9466304VXC	65342	UT69151LXE15/GVCR
5962R9466304VYC	65342	UT69151LXE15/WVCR
5962-9466305QXA	3/	
5962-9466305QYA	3/	
5962-9466305QXC	3/	
5962-9466305QYC	3/	
5962H9466305QXA	65342	UT69151DXE/GQAH
5962H9466305QYA	65342	UT69151DXE/WQAH
5962H9466305QXC	65342	UT69151DXE/GQCH
5962H9466305QYC	65342	UT69151DXE/WQCH

See footnotes at end of table.

STANDARD MICROCIRCUIT DRAWING BULLETIN - Continued.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962H9466305VXA	65342	UT69151DXE/GVAH
5962H9466305VYA	65342	UT69151DXE/WVAH
5962H9466305VXC	65342	UT69151DXE/GVCH
5962H9466305VYC	65342	UT69151DXE/WVCH
5962-9466306QXA	3/	
5962-9466306QYA	3/	
5962-9466306QXC	3/	
5962-9466306QYC	3/	
5962-9466307QXA	65342	UT69151LXE15/GQA
5962-9466307QYA	65342	UT69151LXE15/WQA
5962-9466307QXC	65342	UT69151LXE15/GQC
5962-9466307QYC	65342	UT69151LXE15/WQC
5962-9466308QXA	65342	UT69151DXE/GQA
5962-9466308QYA	65342	UT69151DXE/WQA
5962-9466308QXC	65342	UT69151DXE/GQC
5962-9466308QYC	65342	UT69151DXE/WQC
5962-9466309QXA	65342	UT69151LXE12/GQA
5962-9466309QYA	65342	UT69151LXE12/WQA
5962-9466309QXC	65342	UT69151LXE12/GQC
5962-9466309QYC	65342	UT69151LXE12/WQC

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed, contact the vendor to determine its availability.
2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.
3/ No longer available from an approved source of supply.

Vendor CAGE number	Vendor name and address
65342	UTMC Microelectronics System Inc. 4350 Centennial Boulevard Colorado Springs, Colorado 80907-3486

The information contained herein is disseminated for convenience only and the Government assumes no liability whatsoever for any inaccuracies in the information bulletin.