ACS8510 SETS

Synchronous Equipment Timing Source for SONET or SDH Network Elements

ADVANCED COMMUNCIATIONS — **FINAL**

Description

The ACS8510 is a highly integrated, single-chip solution for the Synchronous Equipment Timing Source (SETS) function in a SONET or SDH Network Element. The device generates SONET or SDH Equipment Clocks (SEC) and frame synchronization clocks. The ACS8510 is fully compliant with the required specifications and standards.

The device supports Free-Run, Locked and Holdover modes. It also supports all three types of reference clock source: recovered line clock, PDH network, and node synchronization. The ACS8510 generates independent SEC and BITS clocks, an 8 kHz Frame Synchronization clock and a 2 kHz Multi-Frame Synchronization clock.

Two ACS8510 devices can be used together in a Master/Slave configuration mode allowing system protection against a single ACS8510 failure.

A microprocessor port is incorporated, providing access to the configuration and status registers for device setup and monitoring. The ACS8510 supports IEEE 1149.1 JTAG boundary scan.

* Meets Holdover requirements, lowest bandwidth 0.1 Hz.

Features

• Suitable for Stratum 3E*, 3, 4E and 4 SONET or SDH Equipment Clock (SEC) applications
• Meets AT&T, ITU-T, ETSI and Telcordia specifications
• Accepts 14 individual input reference clocks
• Generates 11 output clocks
• Supports Free-Run, Locked and Holdover modes of operation
• Robust input clock source quality monitoring on all inputs
• Automatic "hit-less" source switchover on loss of input
• Phase build-out for output clock phase continuity during input switchover and mode transitions
• Microprocessor interface - Intel, Motorola, Serial, Multiplexed, EEPROM
• Programmable wander and jitter tracking/attenuation 0.1 Hz to 20 Hz
• Support for Master/Slave device configuration alignment and hot/standby redundancy
• IEEE 1149.1 JTAG Boundary Scan
• Single 3.3 v operation. 5 v I/O compatible
• Operating temperature (ambient) -40°C to +85°C
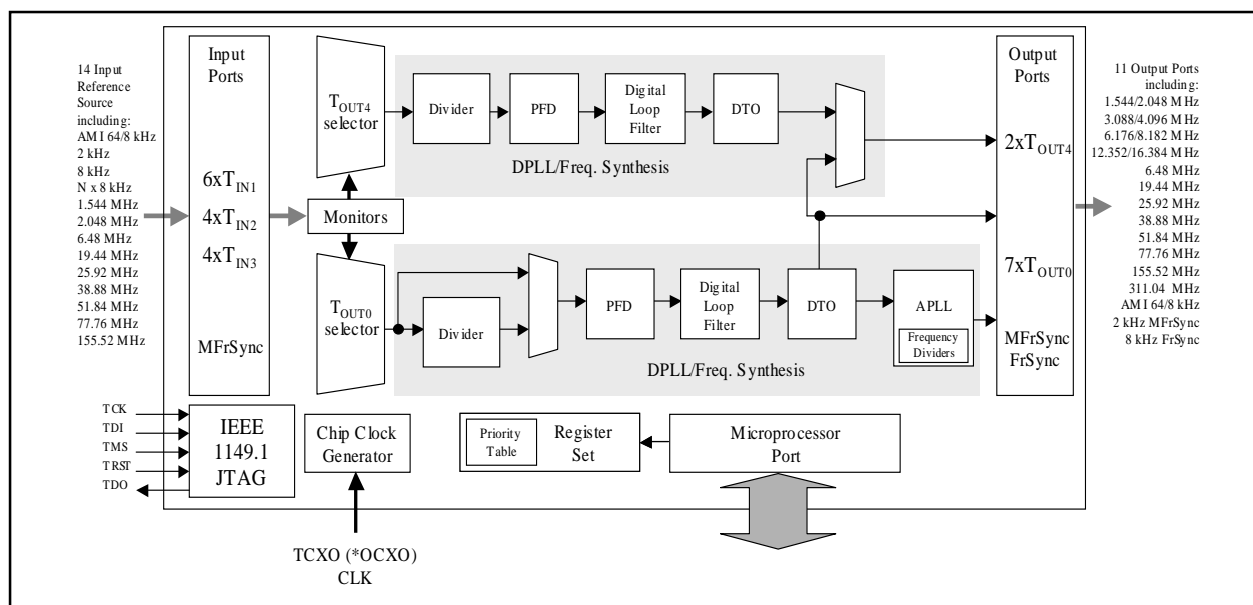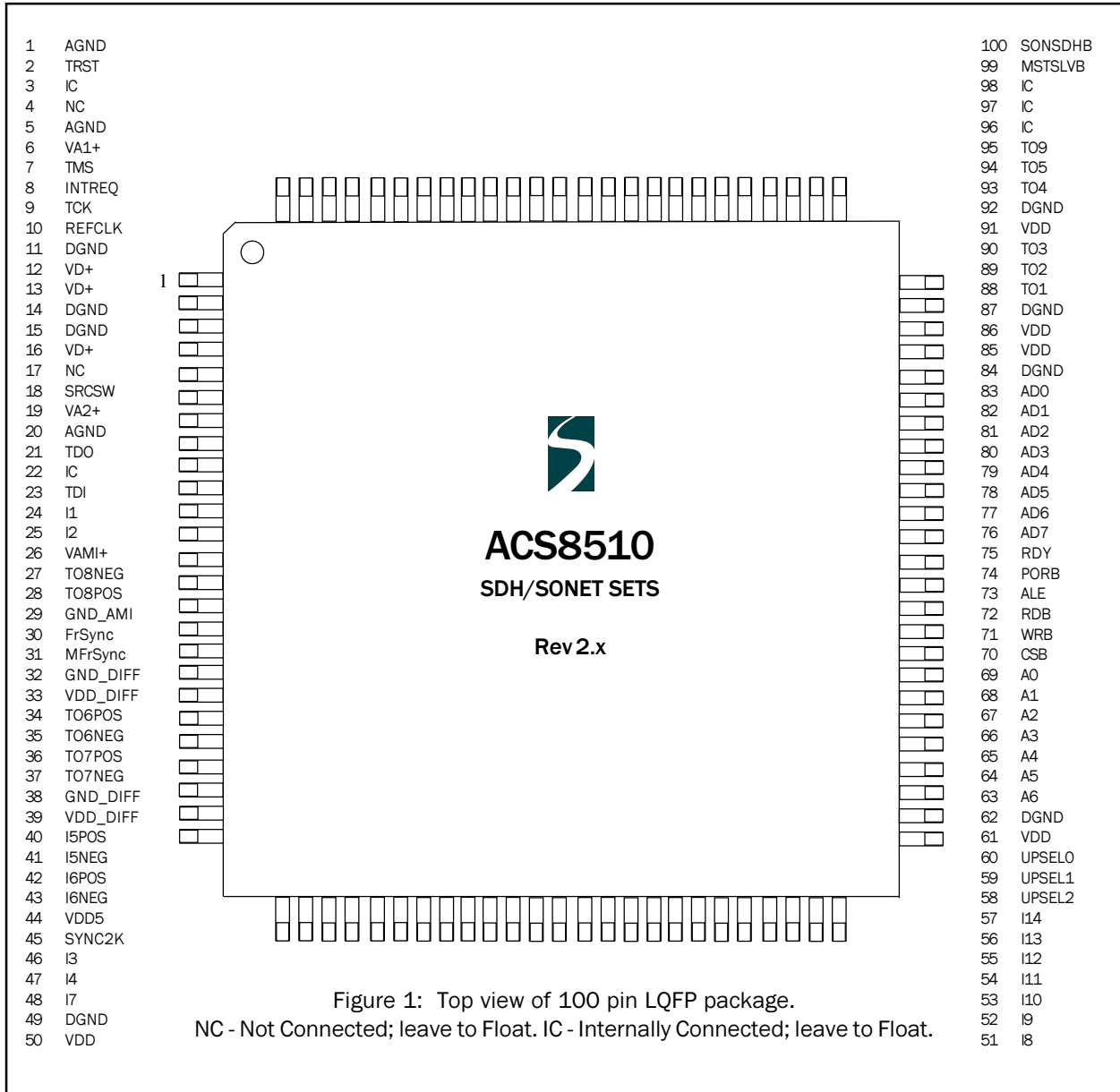• Available in 100 pin LQFP package

Block Diagram

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Pin Diagram

#	Pin		#	Pin
1	AGND		100	SONSDHB
2	TRST		99	MSTSLVB
3	IC		98	IC
4	NC		97	IC
5	AGND		96	IC
6	VA1+		95	TO9
7	TMS		94	TO5
8	INTREQ		93	TO4
9	TCK		92	DGND
10	REFCLK		91	VDD
11	DGND		90	TO3
12	VD+		89	TO2
13	VD+		88	TO1
14	DGND		87	DGND
15	DGND		86	VDD
16	VD+		85	VDD
17	NC		84	DGND
18	SRCSW		83	AD0
19	VA2+		82	AD1
20	AGND		81	AD2
21	TDO		80	AD3
22	IC		79	AD4
23	TDI		78	AD5
24	I1		77	AD6
25	I2		76	AD7
26	VAMI+		75	RDY
27	TO8NEG		74	PORB
28	TO8POS		73	ALE
29	GND_AMI		72	RDB
30	FrSync		71	WRB
31	MFrSync		70	CSB
32	GND_DIFF		69	A0
33	VDD_DIFF		68	A1
34	TO6POS		67	A2
35	TO6NEG		66	A3
36	TO7POS		65	A4
37	TO7NEG		64	A5
38	GND_DIFF		63	A6
39	VDD_DIFF		62	DGND
40	I5POS		61	VDD
41	I5NEG		60	UPSEL0
42	I6POS		59	UPSEL1
43	I6NEG		58	UPSEL2
44	VDD5		57	I14
45	SYNC2K		56	I13
46	I3		55	I12
47	I4		54	I11
48	I7		53	I10
49	DGND		52	I9
50	VDD		51	I8

ACS8510

SDH/SONET SETS

Rev 2.x

Figure 1: Top view of 100 pin LQFP package.
NC - Not Connected; leave to Float. IC - Internally Connected; leave to Float.

Pin Descriptions

Power

PIN	SYMBOL	IO	TYPE	NAME/DESCRIPTION
12, 13, 16	VD+	P	-	Supply voltage: Digital supply to gates in analog section, +3.3 Volts. +/- 10%
26	VAMI+	P	-	Supply voltage : Digital supply to AMI output, +3.3 Volts. +/- 10%
33, 39	VDD_DIFF	P	-	Supply voltage : Digital supply for differential ports, +3.3 Volts. +/- 10%
44	VDD5	P	-	VDD5: Digital supply for +5 Volts tolerance to input pins. Connect to +5 volts (+/- 10%) for clamping to +5 v. Connect to VDD for clamping to +3.3 v. Leave floating for no clamping, input pins tolerant up to +5.5 v.
50, 61, 85, 86, 91	VDD	P	-	Supply voltage : Digital supply to logic, +3.3 Volts. +/- 10%
6	VA1+	P	-	Supply voltage: Analog supply to clock multipying PLL, +3.3 Volts. +/- 10%
19	VA2+	P	-	Supply voltage : Analog supply to output PLL, +3.3 Volts. +/- 10%
11, 14, 15, 49, 62, 84, 87, 92	DGND	P	-	Supply Ground: Digital ground for logic
29	GND_AMI	P	-	Supply Ground: Digital ground for AMI output
32, 38	GND_DIFF	P	-	Supply Ground: Digital ground for differential ports
1, 5, 20	AGND	P	-	Supply Ground: Analog ground

No connections

PIN	SYMBOL	IO	TYPE	NAME/DESCRIPTION
4, 17	NC	-	-	Not Connected: Leave to Float
3, 22, 96, 97,98	IC	-	-	Internally Connected: Leave to Float

Note: I = input, O = output, P = power, TTL^U = TTL input with pull-up resistor, TTL$_D$ = TTL input with pull-down resistor

Others

PIN	SYMBOL	IO	TYPE	NAME/DESCRIPTION
2	TRST	I	TTL$_D$	JTAG Control Reset Input: TRST = 1 to enable JTAG Boundary Scan mode. TRST = 0 for normal device operation (JTAG logic transparent). If not used connect to GND or leave floating.
7	TMS	I	TTL$_U$	JTAG Test Mode Select: Boundary Scan enable. Sampled on rising edge of TCK. If not used connect to VDD or leave floating.
8	INTREQ	O	TTL CMOS	Interrupt Request: Active high software Interrupt output
9	TCK	I	TTL$_D$	JTAG Clock: Boundary Scan clock input. If not used connect to GND or leave floating. This pin may require a capacitor placed between the pin and the nearest GND, to reduce noise pickup. A value of 10 pF should be adequate, but the value is dependent on PCB layout.
10	REFCLK	I	TTL	Reference Clock: 12.8 MHz (refer to section headed Local Oscillator Clock)
18	SRCSW	I	TTL$_D$	Source Switching: Force Fast Source Switching
21	TDO	O	TTL CMOS	JTAG Output: Serial test data output. Updated on falling edge of TCK. If not used leave floating.
23	TDI	I	TTL$_U$	JTAG Input: Serial test data Input. Sampled on rising edge of TCK. If not used connect to VDD or leave floating.
24	I1	I	AMI	Input reference 1: composite clock 64 kHz + 8 kHz
25	I2	I	AMI	Input reference 2: composite clock 64 kHz + 8 kHz
27	TO8NEG	O	AMI	Output reference 8: composite clock, 64 kHz + 8 kHz negative pulse
28	TO8POS	O	AMI	Output reference 8: composite clock, 64 kHz + 8 kHz positive pulse
30	FrSync	O	TTL CMOS	Output reference 10: 8 kHz Frame Sync clock output (square wave)
31	MFrSync	O	TTL CMOS	Output reference 11: 2 kHz Multi-Frame Sync clock output (square wave)
34 35	TO6POS TO6NEG	O	PECL/ LVDS	Output reference 6: default 38.88 MHz. Also Dig1 (1.544 MHz/2.048 MHz and 2, 4, 8 x), 19.44 MHz, 155.52 MHz, 311.04 MHz. Default type LVDS.
36 37	TO7POS TO7NEG	O	LVDS/ PECL	Output reference 7: default 19.44 MHz. Also 51.84 MHz, 77.76 MHz, 155.52 MHz. Default type PECL.
40 41	I5POS I5NEG	I	LVDS PECL	Input reference 5: default 19.44 MHz, default type LVDS
42 43	I6POS I6NEG	I	PECL LVDS	Input reference 6: default 19.44 MHz, default type PECL

PIN	SYMBOL	IO	TYPE	NAME/DESCRIPTION
45	SYNC2K	I	TTL$_D$	Synchronise 2 kHz: Connect to 2 kHz Multi-Frame Sync output of partner ACS8510 in redundancy system
46	I3	I	TTL$_D$	Input reference 3: programmable, default 8 kHz
47	I4	I	TTL$_D$	Input reference 4: programmable, default 8 kHz
48	I7	I	TTL$_D$	Input reference 7: programmable, default 19.44 MHz
51	I8	I	TTL$_D$	Input reference 8: programmable, default 19.44 MHz
52	I9	I	TTL$_D$	Input reference 9: programmable, default 19.44 MHz
53	I10	I	TTL$_D$	Input reference 10: programmable, default 19.44 MHz.
54	I11	I	TTL$_D$	Input reference 11: programmable, default (master mode)1.544/2.048 MHz, default (slave mode) 6.48 MHz
55	I12	I	TTL$_D$	Input reference 12: programmable, default 1.544/2.048 MHz.
56	I13	I	TTL$_D$	Input reference 13: programmable, default 1.544/2.048 MHz.
57	I14	I	TTL$_D$	Input reference 14: programmable, default 1.544/2.048 MHz.
58 - 60	UPSEL(2:0)	I	TTL$_D$	Microprocessor select: Configures the interface for a particular microprocessor type.
63 - 69	A(6:0)	I	TTL$_D$	Microprocessor Interface Address: Address bus for the microprocessor interface registers. A(0) is SDI in Serial mode.
70	CSB	I	TTL^U	Chip Select (Active Low): This pin is asserted Low by the microprocessor to enable the microprocessor interface.
71	WRB	I	TTL^U	Write (Active Low): This pin is asserted Low by the microprocessor to initiate a write cycle. In Motorola mode, WRB = 1 for Read.
72	RDB	I	TTL^U	Read (Active Low): This pin is asserted Low by the microprocessor to initiate a read cycle.
73	ALE	I	TTL$_D$	Address Latch Enable: This pin becomes the address latch enable from the microprocessor. When this pin transitions from High to Low, the address bus inputs are latched into the internal registers. ALE = SCLK in Serial mode.
74	PORB	I	TTL^U	Power On Reset: Master reset. If PORB is forced Low, all internal states are reset. back to default values.
75	RDY	O	TTL CMOS	Ready/Data acknowledge: This pin is asserted High to indicate the device has completed a read or write operation.
76 - 83	AD(7:0)	IO	TTL$_D$	Address/Data: Multiplexed data/address bus depending on the microprocessor mode selection. AD(0) is SDO in Serial mode

PIN	SYMBOL	IO	TYPE	NAME/DESCRIPTION
88	TO1	O	TTL CMOS	Output reference 1: default 6.48 MHz. Also Dig1 (1.544 MHz/2.048 MHz and 2, 4, 8 x), 19.44 MHz, 25.92 MHz
89	TO2	O	TTL CMOS	Output reference 2: default 38.88 MHz. Also Dig2 (1.544 MHz/2.048 MHz and 2, 4, 8 x), 25.92 MHz, 51.84 MHz
90	TO3	O	TTL CMOS	Output reference 3: 19.44 MHz - fixed.
93	TO4	O	TTL CMOS	Output reference 4: 38.88 MHz - fixed.
94	TO5	O	TTL CMOS	Output reference 5: 77.76 MHz - fixed.
95	TO9	O	TTL CMOS	Output reference 9: 1.544/2.048 MHz. (T4 BITS)
99	MSTSLVB	I	TTL^U	MASTERSLAVEB: Master slave select: sets the initial power up state (or state after a PORB) of the Master/Slave selection register, addr 34, bit 1. The register state can be changed after power up by software.
100	SONSDHB	I	TTL$_D$	SONETSDHB: SONET or SDH frequency select: sets the initial power up state (or state after a PORB) of the SONET/SDH frequency selection registers, addr 34h, bit 2 and addr 38, bit 5. The register states can be changed after power up by software.

Functional description

The ACS8510 is a highly integrated, single-chip solution for the SETS function in a SONET/SDH Network Element, for the generation of SEC and frame synchronisation pulses. In Free-Run mode, the ACS8510 generates a stable, low-noise clock signal from an internal oscillator. In Locked mode, the ACS8510 selects the most appropriate input reference source and generates a stable, low-noise clock signal locked to the selected reference. In Holdover mode, the ACS8510 generates a stable, low-noise clock signal from the internal oscillator, adjusted to match the last-known-good frequency of the last-selected reference source. In all modes, the frequency accuracy, jitter and drift performance of the clock meet the requirements of ITU G.812, G.813, G.823, GR 1244-CORE.

The ACS8510 supports all three types of reference clock source: recovered line clock (T_{IN1}), PDH network synchronisation timing (T_{IN2}) and node synchronisation (T_{IN3}). The ACS8510 generates independent T_{OUT0} and T_{OUT4} clocks, an 8 kHz Frame Synchronisation clock and a 2 kHz Multi-Frame Synchronisation clock.

The ACS8510 has a high tolerance to input jitter and wander. The output jitter and wander are low, where the wander transfer is programmable (0.1 Hz up to 20 Hz cut-off points).

The ACS8510 supports protection. Two ACS8510 devices can be configured to provide protection against a single ACS8510 failure. The protection maintains alignment of the two ACS8510 devices (Master and Slave) and ensures that both ACS8510 devices maintain the same priority table, choose the same

reference input and generate the T_{OUT0} clock, the 8 kHz Frame Synchronisation clock and the 2 kHz Multi-Frame Synchronisation clock with the same phase. The ACS8510 includes a microprocessor port, providing access to the configuration and status registers for device setup and monitoring.

Local Oscillator Clock

The Master system clock on the ACS8510 should be provided by an external clock oscillator of frequency 12.80 MHz. The clock specification is important for meeting the ITU/ETSI and Telcordia performance requirements in Holdover mode. ITU and ETSI specifications permit a combined drift characteristic, at constant temperature, of all non-temperature-related parameters, of up to 10 ppb per day. The same specifications allow a drift of 1 ppm over a temperature range of 0 to 70 Celsius. Telcordia specifications are somewhat tighter, requiring a non-temperature-related drift of less than 40 ppb per day and a drift of 280 ppb over the temperature range 0 to 50 Celsius.

ITU and ETSI specification

Tolerance: +/- 4.6 ppm over 20 year life time.

Drift*: +/- 0.05 ppm/15 seconds @ constant temp.

+/- 0.01 ppm/day @ constant temp.

+/- 1 ppm over temp. range 0-70 Celsius

*Frequency drift over supply voltage range of 2.7 V to 3.3 V.

Telcordia GR-1244 CORE specification

Tolerance: +/- 4.6 ppm over 20 year life time.

Drift*: +/- 0.05 ppm/15 seconds @ constant temp.

+/- 0.04 ppm/day @ constant temp.

+/- 0.28 ppm over temp. range 0-50 Celsius

*Frequency drift over supply voltage range of 2.7 V to 3.3 V.

Please contact Semtech for information on crystal oscillator suppliers.

Crystal Frequency Calibration

The absolute crystal frequency accuracy is less important than the stability since any frequency offset can be compensated by adjustment of register values in the IC. This allows for calibration and compensation of any crystal frequency variation away from its nominal value. +/- 50 ppm adjustment would be sufficient to cope with most crystals, in fact the range is an order of magnitude larger due to the use of two 8 bit register locations. The setting of the *conf_nominal_frequency* register allows for this adjustment. An increase in the register value increases the output frequencies by 0.02 ppm for each LSB step. The default value (in decimal) is 39321. The minimum being 0 and the maximum 65535, gives a +500 ppm to -700 ppm adjustment range of the output frequencies.

For example, if the crystal was oscillating at 12.8 MHz + 5 ppm, then the calibration value in the register to give a -5 ppm adjustment in output frequencies to compensate for the crystal inaccuracy, would be : 39321 - (5 / 0.02) = 39071 (decimal).

Input Interfaces

The ACS8510 supports up to fourteen input reference clock sources from input types T_{IN1}, T_{IN2} and T_{IN3} using TTL, CMOS, PECL, LVDS and AMI buffer I/O technologies. These interface technologies support 3.3 V and 5 V operation.

Over-Voltage Protection

The ACS8510 may require Over-Voltage Protection on input reference clock ports according to the ITU Recommendation K.41. Semtech recommends the use of their protection devices for this purpose (see separate Semtech data book).

Input Reference Clock Ports

Table 1 gives details of the input reference ports, showing the input technologies and the range of frequencies supported on each port; the default spot frequencies and default priorities assigned to each port on power-up or by reset are also shown. Note that SDH and SONET networks use different default frequencies; the network type is pin-selectable (using the SONSDHB pin). Specific frequencies and priorities are set by configuration.

Although each input port is shown as belonging to one of the types, T_{IN1}, T_{IN2} or T_{IN3}, they are fully interchangeable as long as the selected speed is within the maximum operating speed of the input port technology.

SDH and SONET networks use different default frequencies; the network type is selectable using the *config_mode* register 34 Hex, bit 2. For SONET, *config_mode* register 34 Hex, bit 2 = 1, for SDH *config_mode* register 34 Hex, bit 2 = 0. On power-up or by reset, the default will be set by the state of the SONSDHB pin (pin 100). Specific frequencies and priorities are set by configuration.

TTL ports (compatible also with CMOS signals) support clock speeds up to 100 MHz, with the highest spot frequency being 77.76 MHz. The actual spot frequencies supported are; 8 kHz (and N x 8 kHz), 1.544 MHz/2.048 MHz, 6.48 MHz, 19.44 MHz, 25.92 MHz, 38.88 MHz, 51.84 MHz, 77.76 MHz. The frequency selection is programmed via the *cnfg_ref_source_frequency* register. The internal DPLL will normally lock to the selected input at the frequency of the input, eg. 19.44 MHz will lock the DPLL phase comparisons at 19.44 MHz. It is, however, possible to utilise an internal pre-divider to the DPLL to divide the input frequency before it is used for phase comparisons in the DPLL. This pre-divider can be used in one of 2 ways:

(i) any of the supported spot frequencies can be divided to 8 kHz by setting the "lock8K" bit (bit 6) in the appropriate cnfg_ref_source_frequency register location

(ii) any multiple of 8 kHz between 1544 kHz to 100 MHz can be supported by using the "DivN" feature (bit 7 of the cnfg_ref_source_frequency register). Any reference input can be set to use DivN independently of the frequencies and configurations of the other inputs.

Any reference input with the "DivN" bit set in the cnfg_ref_source_frequency register will employ the internal pre-divider prior to the DPLL locking. The cnfg_freq_divn register contains the divider ratio N where the reference input will get divided by (N+1) where $0<N<2^{14}-1$. The cnfg_ref_source_frequency register must be set to the closest supported spot frequency to the input frequency, but must be lower than the input frequency. When using the "DivN" feature the post-divider frequency must be 8 kHz, which is indicated by setting the 'lock8k' bit high (bit 6 in 'cnfg_ref_source_ frequency' register). Any input set to DivN must have the frequency monitors disabled (If the frequency monitors are disabled, they are disabled for all inputs regardless of the input configurations, in this case only activity monitoring will take place). Whilst any number of inputs can be set to use the "DivN" feature, only one N can be programmed, hence all inputs using the "DivN" feature must require the same division to get to 8 kHz.

PECL and LVDS ports support the spot clock frequencies listed above plus 155.52 MHz and 311.04 MHz. The choice of PECL or LVDS compatibility is programmed via the *cnfg_differential_inputs* register. Unused PECL/ LVDS differential inputs should be fixed with one input high (VDD) and the other input low (GND), or set in LVDS mode and left floating, in which case one input is internally pulled high and the other low.

Port Number	Channel Number	Port Type	Input Port Technology	Frequencies Supported	Default Priority
I_1	0001	T_{IN3}	AMI	64/8kHz (composite clock, 64kHz + 8kHz) Default (SONET): 64/8kHz Default (SDH): 64/8kHz	2
I_2	0010	T_{IN3}	AMI	64/8kHz (composite clock, 64kHz + 8kHz) Default (SONET): 64/8kHz Default (SDH): 64/8kHz	3
I_3	0011	T_{IN3}	TTL/CMOS	Up to 100MHz (see Note 1) Default (SONET): 8kHz Default (SDH): 8kHz	4
I_4	0100	T_{IN3}	TTL/CMOS	Up to 100MHz (see Note 1) Default (SONET): 8kHz Default (SDH): 8kHz	5
I_5	0101	T_{IN1}	LVDS/PECL LVDS default	Up to 155.52MHz (see Note 2) Default (SONET): 19.44MHz Default (SDH): 19.44MHz	6
I_6	0110	T_{IN1}	PECL/LVDS PECL default	Up to 155.52MHz (see Note 2) Default (SONET): 19.44MHz Default (SDH): 19.44MHz	7
I_7	0111	T_{IN1}	TTL/CMOS	Up to 100MHz (see Note 1) Default (SONET): 19.44MHz Default (SDH): 19.44MHz	8
I_8	1000	T_{IN1}	TTL/CMOS	Up to 100MHz (see Note 1) Default (SONET): 19.44MHz Default (SDH): 19.44MHz	9
I_9	1001	T_{IN1}	TTL/CMOS	Up to 100MHz (see Note 1) Default (SONET): 19.44MHz Default (SDH): 19.44MHz	10
I_10	1010	T_{IN1}	TTL/CMOS	Up to 100MHz (see Note 1) Default (SONET): 19.44MHz Default (SDH): 19.44MHz	11
I_11	1011	T_{IN2}	TTL/CMOS	Up to 100MHz (see Note 1) Default (Master) (SONET): 1.544MHz Default (Master) (SDH): 2.048MHz Default (Slave) 6.48MHz	12/1 (Note 3)
I_12	1100	T_{IN2}	TTL/CMOS	Up to 100MHz (see Note 1) Default (SONET): 1.544MHz Default (SDH): 2.048MHz	13
I_13	1101	T_{IN2}	TTL/CMOS	Up to 100MHz (see Note 1) Default (SONET): 1.544MHz Default (SDH): 2.048MHz	14
I_14	1110	T_{IN2}	TTL/CMOS	Up to 100MHz (see Note 1) Default (SONET): 1.544MHz Default (SDH): 2.048MHz	15

Table 1: Input Reference Source Selection and Priority Table

Notes for Table 1.

Note 1: TTL ports (compatible also with CMOS signals) support clock speeds up to 100 MHz, with the highest spot frequency being 77.76 MHz. The actual spot frequencies are: 2 kHz, 4 kHz, 8 kHz, 1.544 MHz/2.048 MHz, 6.48 MHz, 19.44 MHz, 25.92 MHz, 38.88 MHz, 51.84 MHz, 77.76 MHz. There are different output clock frequencies available for SONET and SDH applications. SONSDHB controls the default frequency output. F_1/F_2 means that the output frequency is F_1 when the SONSDHB pin is High and F_2 when SONSDHB pin is Low.

Note 2: PECL and LVDS ports support the spot clock frequencies listed above plus 155.52 MHz and 311.04 MHz.

Note 3: Input port <I_11> is set at 12 on the Master SETS IC and 1 on the Slave SETS IC, as default on power up (or PORB). The default setup of Master or Slave <I_11> priority is determined by the MSTSLVB pin.

DivN examples

To lock to 2.000 MHz.

(1) The cnfg_ref_source_frequency register is set to 11XX0001 (binary) to set the DivN, lock8k bits, and the frequency to E1/T1. (XX = "leaky bucket" ID for this input).

(2) The cnfg_mode register (34Hex) bit 2 needs to be set to 1 to select SONET frequencies (T1).

(3) The frequency monitors are disabled in cnfg_monitors register (48Hex) by writing 00 to bits 0 and 1.

(4) the DivN register is set to F9 Hex (249 decimal).

To lock to 10.000 MHz.

(1) The cnfg_ref_source_frequency register is set to 11XX0010 (binary) to set the DivN, lock8k bits, and the frequency to 6.48 MHz. (XX = "leaky bucket" ID for this input).

(2) The frequency monitors are disabled in cnfg_monitors register (48Hex) by writing 00 to bits 0 and 1.

(3) the DivN register is set to 4E1 Hex (1249 decimal).

An AMI port supports a composite clock, consisting of a 64 kHz AMI clock with 8 kHz boundaries marked by deliberate violations of the AMI coding rules, as specified in ITU recommendation G.703. Departures from the nominal pattern are detected within the ACS8510, and may cause reference-switching if too frequent. See Figure 9 for more details.

Input Wander and Jitter Tolerance

The ACS8510 is compliant to the requirements of all relevant standards, principally ITU Recommendation G.825, ANSI T1.101-1994 and ETS 300 462-5 (1997).

All reference clock inputs have a tight frequency tolerance but a generous jitter tolerance. Pull-

in, hold-in and pull-out ranges are specified for each input port in Table 2. Minimum jitter tolerance masks are specified in Figures 1 and 2, and Tables 3 and 4, respectively. The ACS8510 will tolerate wander and jitter components greater than those shown in Figure 1 and Figure 2, up to a limit determined by a combination of the apparent long-term frequency offset caused by wander and the eye-closure caused by jitter (the input source will be rejected if the offset pushes the frequency outside the hold-in range for long enough to be detected, whilst the signal will also be rejected if the eye closes sufficiently to affect the signal purity). The '8klocking' mode should be engaged for high jitter tolerance according to these masks. All reference clock

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ports are monitored for quality, including frequency offset and general activity. Single short-term interruptions in selected reference clocks may not cause rearrangements, whilst longer interruptions, or multiple, short-term interruptions, will cause rearrangements, as will frequency offsets which are sufficiently large or sufficiently long to cause loss-of-lock in the phase-locked loop. The failed reference source will be removed from the priority table and declared as unserviceable, until its perceived quality has been restored to an acceptable level.

The registers reg sts_curr_inc_offset (address 0C, 0D, 07) report the frequency of the DPLL with respect to the external TCXO frequency. This is a 19 bit signed number with one LSB representing 0.0003 ppm (range of +/- 80 ppm). Reading this regularly can show how the currently locked source is varying in value e.g. due to wander on its input.

The ACS8510 performs automatic frequency monitoring with an acceptable input frequency offset range of +/- 16.6 ppm. The ACS8510 DPLL has a programmable frequency limit of +/- 80 ppm. If the range is programmed to be > 16.6 ppm, the frequency monitors should be disabled so the input reference source is not automatically rejected as out of frequency range.

Jitter Tolerance	Frequency Monitor Acceptance Range	Frequency Acceptance Range (Pull-in)	Frequency Acceptance Range (Hold-in)	Frequency Acceptance Range (Pull-out)
G.703	+/- 16.6 ppm	+/- 4.6 ppm (see Note 1) +/- 9.2 ppm (see Note 2)	+/- 4.6 ppm (see Note 1) +/- 9.2 ppm (see Note 2)	+/- 4.6 ppm (see Note 1) +/- 9.2 ppm (see Note 2)
G.783				
G.823				
GR-1244-CORE				

Table 2: Input Reference Source Jitter Tolerance.

Notes for Table 2.

Note 1. The frequency acceptance and generation range will be +/-4.6 ppm around the required frequency when the external crystal frequency accuracy is within a tolerance of +/- 4.6 ppm.

Note 2. The fundamental acceptance range and generation range is +/- 9.2 ppm with an exact external crystal frequency of 12.8 MHz.

Note 3. The power up default PDLL range is as stated in note 2, but the range is also programmable from 0 to 80 ppm in 0.08 ppm steps.
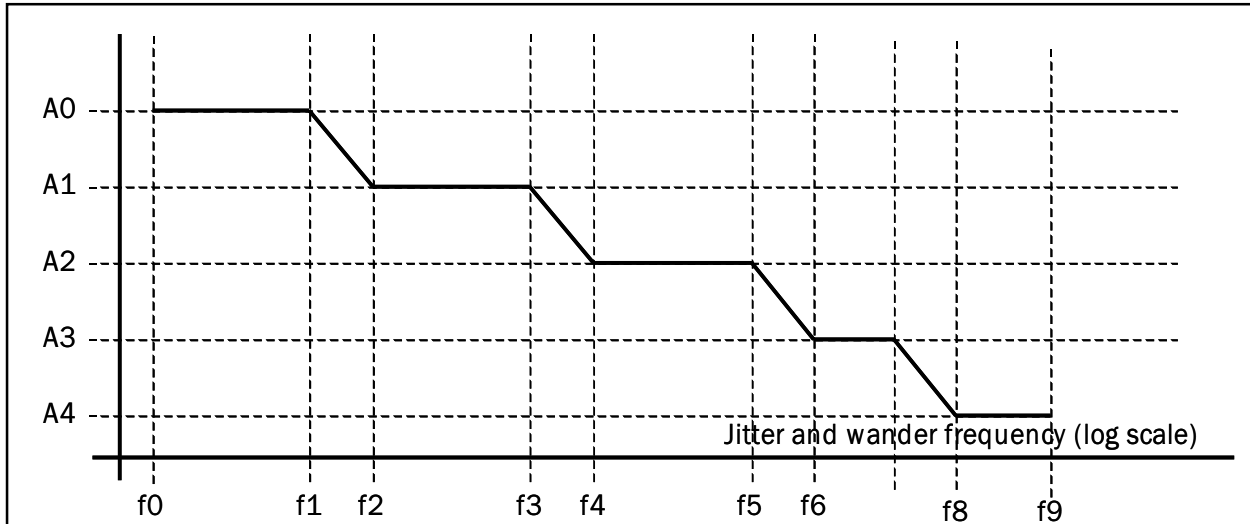
Figure 1: Minimum Input Jitter Tolerance for inputs supporting G.783 compliant sources

STM level	Peak to peak amplitude (unit Interval)					Frequency (Hz)									
	A0	A1	A2	A3	A4	F0	F1	F2	F3	F4	F5	F6	F7	F8	F9
STM-1	2800	311	39	1.5	0.15	12u	178u	1.6m	15.6m	0.125	19.3	500	6.5k	65k	1.3m

Table 3: Amplitude and Frequency values for Jitter Tolerance for inputs supporting G.783 compliant sources

Output Clock Ports

The device supports a set of main output clocks, T_{OUT0} and T_{OUT4}, and a pair of secondary output clocks, 'Frame-Sync' and 'Multi-Frame-Sync'. The two main output clocks, T_{OUT0} and T_{OUT4}, are independent of each other and are individually-selectable. The two secondary output clocks, 'Frame-Sync' and 'Multi-Frame-Sync', are derived from T_{OUT0}. The frequencies of the output clocks are selectable from a range of pre-defined spot frequencies and a variety of output technologies are supported, as defined in Table 5.

Performance-wise, the output ports are specified in Figures 3, 4 and 5, in terms of jitter, MTIE (and TDEV) and Phase Error, respectively.

Low-speed Output Clock (T_{OUT4})

The T_{OUT4} clock is supplied on two output ports, T_{08} and T_{09}. The former port will provide an AMI signal carrying a composite clock of 64 kHz and 8 kHz, according to ITU Recommendation G.703. The latter port will provide a TTL/CMOS signal at either 1.544 MHz or 2.048 MHz, depending on the setting of the SONSDHB pin.

High-speed Output Clock (Part of T_{OUT0})

The T_{OUT0} port has multiple outputs. Outputs T_{01} and T_{02} are TTL/CMOS output with a choice of 11 different frequencies up to 51.84 MHz. Outputs T_{03} to T_{05} are all TTL/CMOS outputs with fixed frequencies of 19.44 MHz, 38.88 MHz and 77.76 MHz, respectively. Output T_{06} is differential and can support clocks up to 155.52 MHz. Output T_{07} is also differential

Peak-to-peak jitter and wander amplitude (log scale)
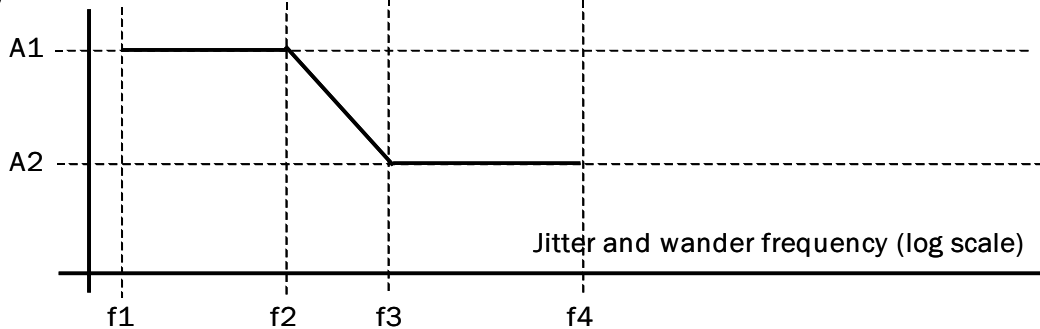
Figure 2: Minimum Input Jitter Tolerance for inputs supporting G.703 compliant sources

Type	Spec.	Amplitude (UI pk-pk)		Frequency (Hz)			
		A1	A2	F1	F2	F3	F4
DS1	GR-1244-CORE	5	0.1	10	500	8k	40k
E1	ITU G.823	1.5	0.2	20	2.4k	18k	100k

Table 4: Amplitude and Frequency values for Jitter Tolerance for inputs supporting G.703 compliant sources

and can support clocks up to 155.52 MHz. Each output is individually configured to operate at the frequencies shown in Table 5 (configuration must be consistent between ACS8510 devices for protection-switching to be effective - output clocks will be phase-aligned between devices). Using the *cnfg_differential_outputs* register, outputs T_{06} and T_{07} can be made to be LVDS or PECL compatible.

Frame Sync and Multi-Frame Sync Clocks (Part of T_{OUT0})

Frame Sync (8 kHz) and Multi-Frame Sync (2 kHz) clocks will be provided on outputs T_{010} (FrSync) and T_{011} (MFrSync). The FrSync and MFrSync clocks have a 50:50 mark space ratio.

These will be driven from the T_{OUT0} clock. They will be synchronised with their counterparts in a second ACS8510 device (if used), using the technique described later.

Output Wander and Jitter

Wander and jitter present on the output clocks are dependent on:

The magnitude of wander and jitter on the selected input reference clock (in Locked mode);

The internal wander and jitter transfer characteristic (in Locked mode);

The jitter on the local oscillator clock;

The wander on the local oscillator clock (in

Holdover mode).

Wander and jitter are treated in different ways to reflect their differing impacts on network design. Jitter is always strongly attenuated, whilst wander attenuation can be varied to suit the application and operating state. Wander and jitter attenuation is performed using a digital phase locked loop (DPLL) with a programmable bandwidth. This gives a transfer characteristic of a low pass filter, with a programmable pole.

It is sometimes necessary to change the filter dynamics to suit particular circumstances - one example being when locking to a new source, the filter can be opened up to reduce locking time and can then be gradually tightened again to remove wander. Since wander represents a relatively long-term deviation from the nominal operating frequency, it affects the rate of supply of data to the network element. Strong wander attenuation limits the rate of consumption of data to within a smaller range, so a larger buffer

Port Name	Output Port Technology	Frequencies Supported
T_{01}	TTL/CMOS	1.544 MHz/2.048 MHz, 3.088 MHz/4.096 MHz, 6.176 MHz/8.192 MHz, 6.48 MHz (default), 12.352 MHz/16.384 MHz, 19.44 MHz, 25.92 MHz
T_{02}	TTL/CMOS	1.544 MHz/2.048 MHz, 3.088 MHz/4.096 MHz, 6.176 MHz/8.192 MHz, 12.352 MHz/16.384 MHz, 25.92 MHz, 38.88 MHz (default), 51.84 MHz
T_{03}	TTL/CMOS	19.44 MHz - fixed
T_{04}	TTL/CMOS	38.88 MHz - fixed
T_{05}	TTL/CMOS	77.76 MHz - fixed
T_{06}	PECL/LVDS (LVDS default)	1.544 MHz/2.048 MHz, 3.088 MHz/4.096 MHz, 6.176 MHz/8.192 MHz, 12.352 MHz/16.384 MHz, 19.44 MHz, 38.88 MHz (default), 155.52 MHz, 311.04 MHz
T_{07}	LVDS/PECL (PECL default)	19.44 MHz (default), 51.84 MHz, 77.76 MHz, 155.52 MHz
T_{08}	AMI	64/8 kHz (composite clock, 64 kHz + 8 kHz)
T_{09}	TTL/CMOS	1.544 MHz/2.048 MHz
T_{010}	TTL/CMOS	FrSync, 8 kHz - with a 50:50 MSR
T_{011}	TTL/CMOS	MFrSync, 2 kHz - with a 50:50 MSR

Table 5: Output Reference Source Selection Table

Note for Table 5.

Frequencies supported: There are different output clock frequencies available for SONET and SDH applications. SONSDHB controls the default frequency output. F_1/F_2 means that the output frequency is F_1 when the SONSDHB pin is High and F_2 when SONSDHB pin is Low.

store is required to prevent data loss. But, since any buffer store potentially increases latency, wander may often only need to be removed at specific points within a network where buffer stores are acceptable, such as at digital cross connects. Otherwise, wander is sometimes not required to be attenuated and can be passed through transparently. The ACS8510 has programmable wander transfer characteristics in a range from 0.1 Hz to 20 Hz. The wander and jitter transfer characteristic is shown in Figure 3.

Wander on the local oscillator clock will not have significant effect on the output clock whilst in Locked mode, so long as the DPLL bandwidth is set high enough so that the DPLL can compensate quickly enough for any frequency changes in the crystal. In Free-Running or Holdover mode wander on the crystal is more significant. Variation in crystal temperature or supply voltage both cause drifts in operating frequency, as does ageing. These effects must

be limited by careful selection of a suitable component for the local oscillator, as specified in the section 'Local Oscillator Clock'.

Phase Variation

There will be a phase shift across the ACS8510 between the selected input reference source and the output clock. This phase shift may vary over time but will be constrained to lie within specified limits. The phase shift is characterised using two parameters, MTIE (Maximum Time Interval Error), and TDEV (Time Deviation), which, although being specified in all relevent specifications, differ in acceptable limits in each one. Typical measurements for the ACS8510 are shown in Figures 4 and 5, for Locked mode operation. Figure 6 shows a typical measurement of Phase Error accumulation in Holdover mode operation.

The required performance for phase variation during Holdover is specified in several ways depending upon the particular circumstances
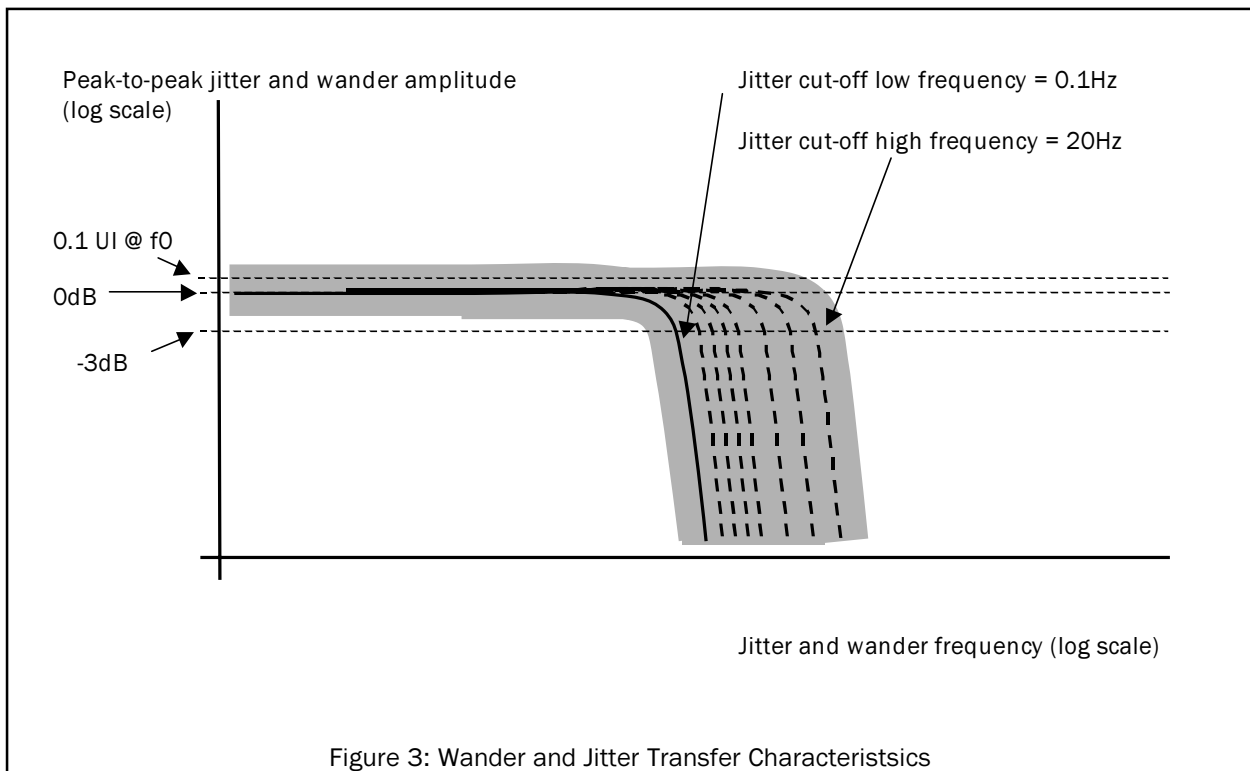
Figure 3: Wander and Jitter Transfer Characteristsics

pertaining:

1. ETSI 300 462-5, Section 9.1, requires that the short-term phase error during switchover (i.e., Locked to Holdover to Locked) be limited to an accumulation rate no greater than 0.05 ppm during a 15 second interval.

2. ETSI 300 462-5, Section 9.2, requires that the long-term phase error in the Holdover mode should not exceed $\{(a1+a2)S+0.5bS^2+c\}$, where

a1 = 50 ns/s (allowance for initial frequency offset)

a2 = 2000 ns/s   (allowance for temperature variation)

b = 1.16×10^{-4} ns/s^2 (allowance for ageing)

c = 120 ns (allowance for entry into Holdover mode).

3. ANSI Tin1.101-1994, Section 8.2.2, requires that the phase variation be limited so that no more than 255 slips (of 125 µs each) occur during the first day of Holdover. This requires a frequency accuracy better than:

$((24 \times 60 \times 60) + (255 \times 125 \mu s))/(24 \times 60 \times 60) = 0.37$ ppm.

Temperature variation is not restricted, except to within the normal bounds of 0 to 50 Celsius.

4. Telcordia GR.1244.CORE, Section 5.2. Table 4. shows that an initial frequency offset of 50 ppb is permitted on entering Holdover, whilst a drift over temperature of 280 ppb is allowed; an allowance of 40 ppb is permitted for all other effects.

5. ITU G.822, Section 2.6, requires that the slip rate during category(b) operation (interpreted as being applicable to Holdover mode operation) be limited to less than 30 slips (of 125 µs each) per hour

$((((60 \times 60)/30)+125 \mu s)/(60 \times 60)) = 1.042$ ppm.

Phase Build Out

Phase Transient Response and Holdover

Phase Build Out (PBO) is the function to minimise phase transients on the output SEC clock during input reference switching. If the currently selected input reference clock source is lost (due to a short interruption, out of frequency detection, or complete loss of reference), the second, next highest priority reference source will be selected. During this transition, the Lost_Phase mode is entered.

The typical phase disturbance on clock reference source switching will be less than 12 ns on the ACS8510. For clock reference switching caused by the main input failing or being disconnected, then the phase disturbance on the output will still be less than the 120 ns allowed for in the G.813 spec. The actual value is dependant on the frequency being locked to.

The PBO requirement, as specified in Telcordia GR1244-CORE, Section 5.7, is that a phase transient of greater than 3.5 µs occuring in less than 0.1 seconds should be absorbed. This will be implemented on a future version.

ITU-T G.813 states that the max allowable short term phase transient response, resulting from a switch from one clock source to another, with Holdover mode entered in between, should be a maximum of 1 µs over a 15 second interval. The maximum phase transient or jump should be less than 120 ns at a rate of change of less than 7.5 ppm and the Holdover performance should be better than 0.05 ppm.

On the ACS8510, PBO can be enabled, disabled or frozen using the µP interface. By default, it is enabled. When PBO is enabled, it can also be frozen, which will disable the PBO operation on the next input reference switch, but will remain with the current offset. If PBO is disabled while the device is in the Locked mode, there will be a phase jump on the output SEC clocks as the DPLL locks back to 0 degree phase error.

Micro-Processor Interface

The ACS8510 incorporates a microprocessor interface, which can be configured for the following modes via the bus interface mode control pins UPSEL(2:0) as defined in Table 6.

Figure 4: Maximum Time Interval Error of T_{OUT0} output port

Figure 5: Time Deviation of T_{OUT0} output port

Figure 6: Phase error accumulation of T_{OUT0} output port in hold-over mode
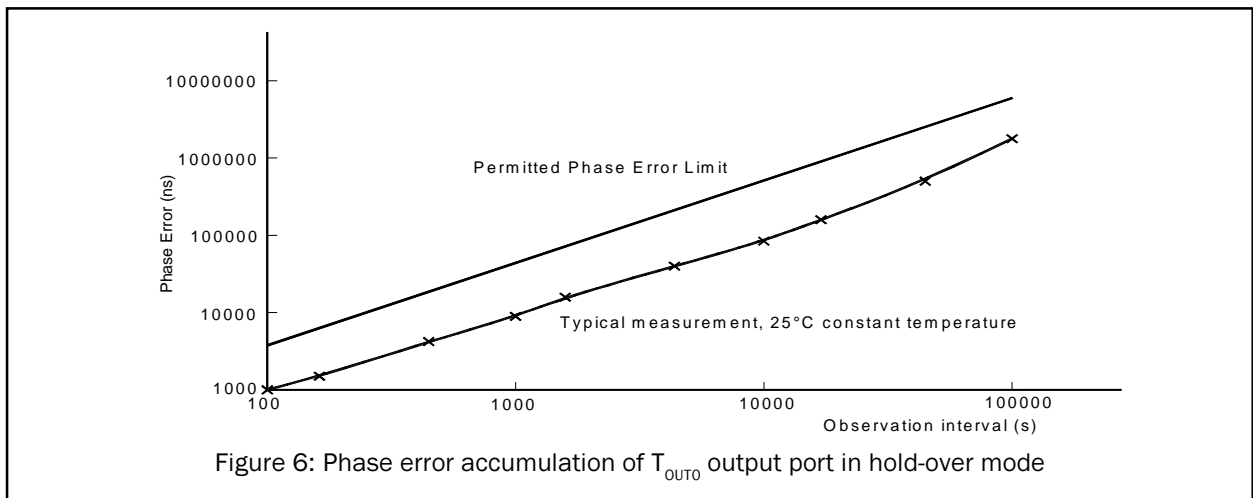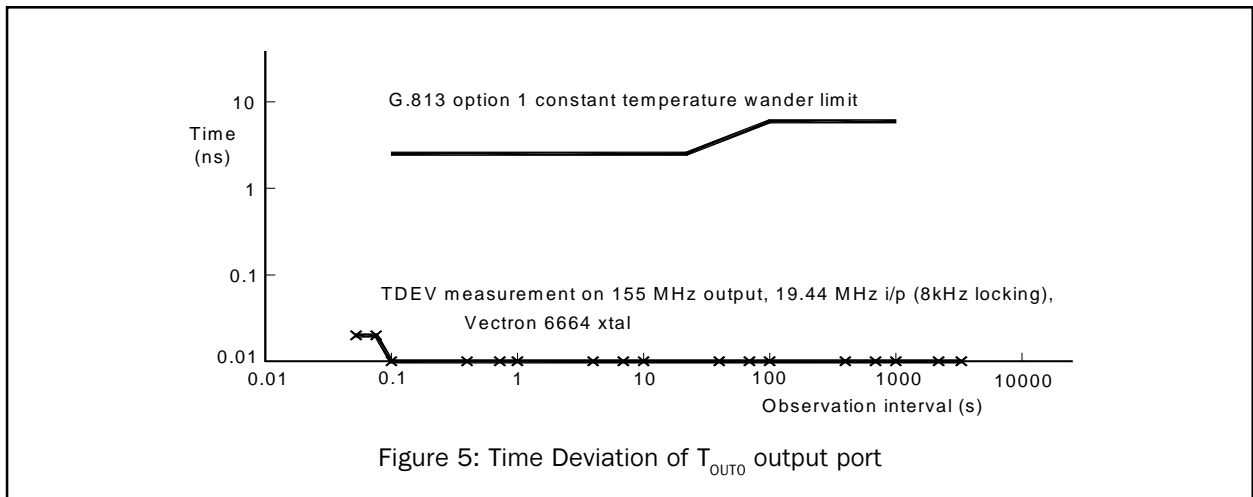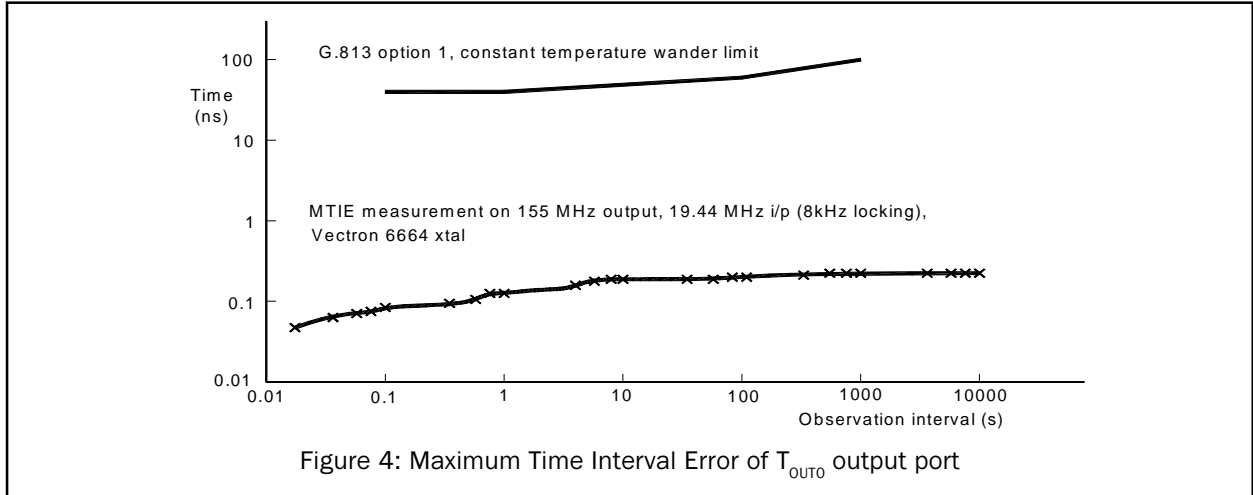
UPSEL(2:0)	Mode	Description
111 (7)	OFF	Interface disabled
110 (6)	OFF	Interface disabled
101 (5)	SERIAL	Serial uP bus interface
100 (4)	MOTOROLA	Motorola interface
011 (3)	INTEL	Intel compatible bus interface
010 (2)	MULTIPLEXED	Multiplexed bus interface
001 (1)	EPROM	EPROM read mode
000 (0)	OFF	Interface disabled

Table 6: Microprocessor Interface Mode Selection

Motorola Mode

Parallel data + address: this mode is suitable for use with Motorola's 68x0 type bus.

Intel Mode

Parallel data + address: this mode is suitable for use with Intel's 80x86 type bus.

Multiplexed Mode

Data/address: this mode is suitable for use with microprocessors which share bus signals between address and data (e.g., Intel's 80x86 family).

Serial Mode

This mode is suitable for use with microprocessor which use a serial interface.

EPROM Mode

This mode is suitable for use with an EPROM, in which configuration data is stored (one-way communication - status information will not be accessible). A state machine internal to the ACS8510 device will perform numerous EPROM read operations to pull the data out of the EPROM.

Register Set

All registers are 8-bits wide, organised with the most-significant bit positioned in the left-most bit, with bit-significance decreasing towards the right most bit. Some registers carry several individual data fields of various sizes, from single-bit values (e.g. flags) upwards. Several data fields are spread across multiple registers; their organisation is shown in the register map, Table 7.

Configuration Registers

Each configuration register reverts to a default value on power-up or following a reset. Most default values are fixed, but some will be pin-settable. All configuration registers can be read out over the microprocessor port.

Status Registers

The Status Registers contain readable registers. They may all be read from outside the chip but are not writeable from outside the chip (except for a clearing operation). All status registers are read via shadow registers to avoid data hits due to dynamic operation. Each individual status register has a unique location.

Register Access

Most registers are of one of two types, configuration registers or status registers, the exceptions being the Chip_ID and Chip_revision registers. Configuration registers may be written to or read from at any time (the complete 8-bit register must be written, even if only one bit is being modified). All status registers may be read at any time and, in some status registers (such as the 'sts_interrupts' register), any individual data field may be cleared by writing a "1" into each bit of the field (writing a "0" value into a bit will not affect the value of the bit). A description of each register follows.

Interrupt Enable and Clear

Interrupt requests are flagged on pin INTREQ (active High).

Bits in the interrupt status register are set (high)

by the following conditions;

(i) any reference source becoming valid or going invalid

(ii) a change in the operating state (eg. locked, holdover etc.)

(iii) brief loss of the currently selected reference source

(iv) AMI input error

All interrupt sources are maskable via the mask register, each one being enabled by writing a '1' to the appropriate bit.

Any unmasked bit set in the interrupt status register will cause the interrupt request pin to be asserted (high).

All interrupts are cleared by writing a '1' to the bit(s) to be cleared in the status register.

When all pending unmasked interrupts are cleared the interrupt pin will go inactive (low).

The loss of the currently selected reference source will eventually cause the input to be considered invalid, triggering an interrupt. The time taken to raise this interrupt is dependant on the leaky bucket configuration of the activity monitors. The very fastest leaky bucket setting will still take up to 128 ms to trigger the interrupt. The interrupt caused by the brief loss of the currently selected reference source is provided to facilitate very fast source failure detection if desired. It is triggered after missing just a couple of cycles of the reference source. Some applications require the facility to switch downstream devices based on the status of the reference sources. In order to provide extra flexibility, it is possible to flag the "main reference failed" interrupt (addr 06, bit 6) on the pin TDO. This is simply a copy of the status bit in the interrupt register and is independent of the mask register settings. The bit is reset by writing to the interrupt status register in the normal way. This feature can be enabled and disabled by writing to bit 6 of register 48Hex.

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Register map

Shaded areas in the map are 'don't care' and writing either 0 or 1 will not affect any function of the device.

Bits labelled 'Set to 0' or 'Set to 1' must be set as stated during initialisation of the device, either following power up, or after a power on reset (POR). Failure to correctly set these bits may result in the device operating in an unexpected way.

Some registers do not appear in this list. These are either not used, or have test functionality. Do not write to any undefined registers as this may cause the device to operate in a test mode. If an undefined register has been inadvertently addressed, the device should be reset to ensure the undefined registers are at default values.

Addr. (Hex)	Parameter Name	Data Bit							
		7 (msb)	6	5	4	3	2	1	0 (lsb)
00	chip_id (read only)	Device part number (7:0)							
01		Device part number (15:8)							
02	chip_revision (read only)	Chip revision number (7:0)							
03	cnfg_control1 (read/write)			Set to '0'	Analog div sync	Set to '0'	Set to '0'	Set to '0'	Set to '0'
04	cnfg_control2 (read/write)			Phase loss flag limit			Set to '0'	Set to '1'	Set to '0'
05	sts_interrupts (read/write)	<I_8> valid change	<I_7> valid change	<I_6> valid change	<I_5> valid change	<I_4> valid change	<I_3> valid change	<I_2> valid change	<I_1> valid change
06		Operating mode	Main ref. failed	<I_14> valid change	<I_13> valid change	<I_12> valid change	<I_11> valid change	<I_10> valid change	<I_9> valid change
08	sts_T4_inputs (read/write)				T4 ref failed	Ami2 Violation	Ami2 L.O.S.	Ami1 Violation	Ami1 L.O.S.
09	sts_operating_mode (read only)						Operating mode (2:0)		
0A	sts_priority_table (read only)	Highest priority valid source				Currently selected reference source			
0B		3rd highest priority valid source				2nd highest priority valid source			
0C	sts_curr_inc_offset (read only)	Current increment offset (7:0)							
0D		Current increment offset (15:8)							
07							Current increment offset (18:16)		
0E	sts_sources_valid (read only)	<I_8>	<I_7>	<I_6>	<I_5>	<I_4>	<I_3>	<I_2>	<I_1>
0F				<I_14>	<I_13>	<I_12>	<I_11>	<I_10>	<I_9>

Addr. (Hex)	Parameter Name	Data Bit							
		7 (msb)	6	5	4	3	2	1	0 (lsb)
10	sts_reference_sources (read/write)	status <l_2>				status <l_1>			
11		status <l_4>				status <l_3>			
12		status <l_6>				status <l_5>			
13		status <l_8>				status <l_7>			
14		status <l_10>				status <l_9>			
15		status <l_12>				status <l_11>			
16		status <l_14>				status <l_13>			
18	cnfg_ref_selection_priority (read/write)	programmed_priority <l_2>				programmed_priority <l_1>			
19		programmed_priority <l_4>				programmed_priority <l_3>			
1A		programmed_priority <l_6>				programmed_priority <l_5>			
1B		programmed_priority <l_8>				programmed_priority <l_7>			
1C		programmed_priority <l_10>				programmed_priority <l_9>			
1D		programmed_priority <l_12>				programmed_priority <l_11>			
1E		programmed_priority <l_14>				programmed_priority <l_13>			
20	cnfg_ref_source_frequency (read/write)	divn	lock8k	bucket_id <l_1>(1:0)		reference_source_frequency <l_1>(3:0)			
21		divn	lock8k	bucket_id <l_2>(1:0)		reference_source_frequency <l_2>(3:0)			
22		divn	lock8k	bucket_id <l_3>(1:0)		reference_source_frequency <l_3>(3:0)			
23		divn	lock8k	bucket_id <l_4>(1:0)		reference_source_frequency <l_4>(3:0)			
24		divn	lock8k	bucket_id <l_5>(1:0)		reference_source_frequency <l_5>(3:0)			
25		divn	lock8k	bucket_id <l_6>(1:0)		reference_source_frequency <l_6>(3:0)			
26		divn	lock8k	bucket_id <l_7>(1:0)		reference_source_frequency <l_7>(3:0)			
27		divn	lock8k	bucket_id <l_8>(1:0)		reference_source_frequency <l_8>(3:0)			
28		divn	lock8k	bucket_id <l_9>(1:0)		reference_source_frequency <l_9>(3:0)			
29		divn	lock8k	bucket_id <l_10>(1:0)		reference_source_frequency <l_10>(3:0)			
2A		divn	lock8k	bucket_id <l_11>(1:0)		reference_source_frequency <l_11>(3:0)			
2B		divn	lock8k	bucket_id <l_12>(1:0)		reference_source_frequency <l_12>(3:0)			
2C		divn	lock8k	bucket_id <l_13>(1:0)		reference_source_frequency <l_13>(3:0)			
2D		divn	lock8k	bucket_id <l_14>(1:0)		reference_source_frequency <l_14>(3:0)			

Addr. (Hex)	Parameter Name	Data Bit							
		7 (msb)	6	5	4	3	2	1	0 (lsb)
30	cnfg_sts_remote_sources_valid	Remote status, channels <8:1>							
31	(read/write)			Remote status, channels <14:9>					
32	cnfg_operating_mode (read/write)						Forced operating mode		
33	cnfg_ref_selection (read/write)						force_select_reference_source		
34	cnfg_mode (read/write)	Auto external 2K enable	Phase alarm timeout enable	Clock edge	Holdover Offset enable	External 2K Sync enable	SONET/ SDH I/P	Master/ Slave	Reversion mode
35	cnfg_T4 (read/write)			Squelch	Select T0/T1	Force T1 input source selection (only valid for inputs I_5 to I_10)			
36	cnfg_differential_inputs (read/write)							<I_6> PECL	<I_5> PECL
37	cnfg_uPsel_pins (read only)						Micro-processor type		
38	cnfg_T0_output_enable (read/write)	311.04MHz on T06	1=SONET 0=SDH for Dig2	1=SONET 0=SDH for Dig1	T01	T02	T03 19.44MHz	T04 38.88MHz	T05 77.76MHz
39	cnfg_T0_output_frequencies (read/write)	Digital2		Digital1		T02		T01	
3A	cnfg_differential_outputs (read/write)	T07 Frequency selection		T06 Frequency selection		T07 LVDS enable	T07 PECL enable	T06 LVDS enable	T06 PECL enable
3B	cnfg_bandwidth (read/write)	Auto b/w switch Acq/lock	Acquisition bandwidth			Set to '0'	Normal/locked bandwidth		
3C	cnfg_nominal_frequency (read/write)	Nominal frequency (7:0)							
3D		Nominal frequency (15:8)							
3E	cnfg_holdover_offset (read/write)	Holdover offset (7:0)							
3F		Holdover offset (15:8)							
40		Auto Holdover Averaging					Holdover offset (18:16)		
41	cnfg_freq_limit (read/write)	DPLL Frequency offset limit (7:0)							
42								DPLL Frequency offset limit (9:8)	
43	cnfg_interrupt_mask (read/write)	<I_8> valid change	<I_7> valid change	<I_6> valid change	<I_5> valid change	<I_4> valid change	<I_3> valid change	<I_2> valid change	<I_1> valid change
44		Operating mode	Main ref. failed	<I_14> valid change	<I_13> valid change	<I_12> valid change	<I_11> valid change	<I_10> valid change	<I_9> valid change
45					T4 ref	Ami2 Violation	Ami2 L.O.S	Ami1 Violation	Ami1 L.O.S
46	cnfg_freq_divn (read/write)	Divide-input-by-n ratio (7:0)							
47				Divide-input-by-n ratio (13:8)					

Addr. (Hex)	Parameter Name	Data Bit							
		7 (msb)	6	5	4	3	2	1	0 (lsb)
48	cnfg_monitors (read/write)		Flag ref lost on TDO	Ultra-fast switching	External source switch enable	Freeze phase buildout	Phase buildout enable	Frequency monitors configuration (1:0)	
50	cnfg_activ_upper_threshold0 (read/write)	Configuration 0: Activity alarm set threshold (7:0)							
51	cnfg_activ_lower_threshold0 (read/write)	Configuration 0: Activity alarm reset threshold (7:0)							
52	cnfg_bucket_size0 (read/write)	Configuration 0: Activity alarm bucket size (7:0)							
53	cnfg_decay_rate0 (read/write)							Cfg 0:decay_rate (1:0)	
54	cnfg_activ_upper_threshold1 (read/write)	Configuration 1: Activity alarm set threshold (7:0)							
55	cnfg_activ_lower_threshold1 (read/write)	Configuration 1: Activity alarm reset threshold (7:0)							
56	cnfg_bucket_size1 (read/write)	Configuration 1: Activity alarm bucket size (7:0)							
57	cnfg_decay_rate1 (read/write)							Cfg 1:decay_rate (1:0)	
58	cnfg_activ_upper_threshold2 (read/write)	Configuration 2: Activity alarm set threshold (7:0)							
59	cnfg_activ_lower_threshold2 (read/write)	Configuration 2: Activity alarm reset threshold (7:0)							
5A	cnfg_bucket_size2 (read/write)	Configuration 2: Activity alarm bucket size (7:0)							
5B	cnfg_decay_rate2 (read/write)							Cfg 2:decay_rate (1:0)	
5C	cnfg_activ_upper_threshold3 (read/write)	Configuration 3: Activity alarm set threshold (7:0)							
5D	cnfg_activ_lower_threshold3 (read/write)	Configuration 3: Activity alarm reset threshold (7:0)							
5E	cnfg_bucket_size3 (read/write)	Configuration 3: Activity alarm bucket size (7:0)							
5F	cnfg_decay_rate3 (read/write)							Cfg 3:decay_rate (1:0)	
7F	cnfg_uPsel (read/write)						Micro-processor type		

Register map description

Addr. (Hex)	Parameter Name	Description	Default Value (bin)
00	chip_id	This read-only register contains the device ID. Address 00 Least-significant byte: 3E(hex)	00111110
01		Address 01 Most-significant byte: 21(hex) 213E(hex) = 8510(dec)	00100001
02	chip_revision	This read only register contains the chip revision number	00000001
03	cnfg_control1	Bits (3:0) & 5 are test controls and should be either set at '0' during initialisation or left unchanged. Bit 4, when set high, synchronises the dividers in the output APLL section to the dividers in the DPLL section such that their phases align. This is necessary to have the phase alignment between the inputs and output clocks at OC3 derived rates (6.48 MHz to 77.76 MHz). By default, synchronisation occurs for 2 seconds after power up and is then turned off. Setting this bit high keeps synchronisation on, which may be necessary to avoid the dividers getting out of sync when quick changes in frequency occur such as a force into freerun mode.	XX000000
04	cnfg_control2	Bits (2:0) are test controls and should be set at '010' during initialisation or left unchanged. Bits (5:3) define the phase loss flag limit. By default set to 4 (100) which corresponds to approximately 140°. A lower value sets a corresponding lower phase limit. The flag limit determines the value at which the DPLL indicates phase lost as a result of input jitter, a phase jump, or a frequency jump on the input	XX100010
	sts_interrupts	This 16 bit register contains one bit for each bit of sts_sources_valid, one for loss of reference the device was locked to, and another for the operating mode. All bits are active high. All bits except the main_ref_failed bit (bit14) are set on a "change" in the state of the relevent status bit, i.e. if a source becomes valid, or goes invalid it will trigger an interrupt. If the FSM changes state at all the interrupt will be generated. Bit 14 (main_ref_failed) of the interrupt status register is used to flag inactivity on the reference that the device is locked to much more quickly than the activity monitors can support. If bit 6 of the cnfg_monitors register (flag ref loss on TDO) is set, then the state of this bit is driven onto the TDO pin of the device. All bits are maskable by the bits in the cnfg_interrupt_mask register. Each bit may be cleared individually by writing a '1' to that bit, thus resetting the interrupt. Any number of bits can be cleared with a single write operation. Writing '0's will have no effect.	
05		Least-significant byte (7:0)	00000000
06		Most-significant byte (15:8)	00000000
08	sts_T4_inputs	This register holds the status flags of the AMI inputs and the TOUT4 reference. The alarms once set will hold their state until reset. Each bit may be cleared individually by writing a '1' to that bit, thus resetting the interrupt. Writing '0's will have no effect. These bits can also generate interrupts. Bit Content 0: '1' = Ami1 Loss of signal; '0' = Ami1 clear 1: '1' = Ami1 Violation detected; '0' = Ami1 clear 2: '1' = Ami2 Loss of signal; '0' = Ami2 clear 3: '1' = Ami2 Violation detected; '0' = Ami2 clear 4: '1' = T4 reference failed - no valid T_{IN1} input (<I_10>:<I_5>), T4 DPLL cannot lock to source; '0' = T4 reference good - valid T_{IN1} input available (5:7) unused (value: x)	XXX10000
09	sts_operating_mode	This read-only register holds the current operating state of the main state machine. Figure 7 show how the values of the 'operating state' variable match with the individual states. Bit Content 2:0 Operating state (2:0) Bits (2:0) State 001 freerun 010 holdover 100 locked 110 pre-locked 101 pre-locked2 111 phase lost (3:7) unused	XXXXX001

Addr. (Hex)	Parameter Name	Description	Default Value (bin)
	sts_priority_table	This is a 16-bit read-only register, taking two addresses. Currently-selected reference source: this is the channel number of the input reference source which is currently connected to the SETG function. Highest-priority valid source: this is the channel number of the input reference source which is valid and has the highest priority; it may not be the same as the currently-selected reference source (due to failure history or changes in programmed priority). Second-highest priority valid source: this is the channel number of the input reference source which is valid and has the next-highest priority to the highest-priority valid source. Third-highest priority valid source: this is the channel number of the input reference source which is valid and has the next-highest priority to the second-highest-priority valid source. Note that these registers are updated by the state machine in response to the contents of the cnfg_ref_selection_priority register and the ongoing status of individual channels; channel number '0000', appearing in any of these registers, indicates that no channel is available for that priority. Bit　　　　Content	
0A		(7:4)　　　Highest-priority valid source (3:0)　　　Currently selected reference source	00000000
0B		(7:4)　　　3rd-highest-priority valid source (3:0)　　　2nd-highest-priority valid source	00000000
	sts_curr_inc_offset	This read-only register contains a signed-integer value representing the 19 bits of the current increment offset of the digital PLL. The register may be read periodically to build up a historical database for later use during holdover periods (this would only be necessary if an external oscillator which did not meet the stability criteria described in Local Oscillator Clock section is used). The register will read 00000000 immediately after reset.	
0C		Least significant byte of offset value	00000000
0D		Next significant byte of offset value	00000000
07		Bits (7:4) unused Bits (2:0) 3 most significant bits of offset value	XXXXX000
0E	sts_sources_valid	This 14 bit register contains copies of bit 3 from all the status_reference_sources bytes. This allows the user to get the 'validity' of all sources in just 2 reads.	00000000
0F		This register only indicates whether or not a source has passed all criteria.	XX000000
	sts_reference_sources	This is a 7-byte register which holds the status of each of the 14 input reference sources. The status of each reference source is shown in a 4-bit field. Each bit is active high.To aid status checking, a copy of each status bit 3 is provided in the sts_sources_valid register. The status is reported as follows: (Each bit may be cleared individually) Status bit 0 = phase lock alarm Status bit 1 = no activity alarm Status bit 2 = out-of-band alarm Status bit 3 = Source valid (no alarms) (bit 3 is combination of bits (2:0)) The organisation of the register is shown below and in the register map. Bit　　　　Content	
10		(3:0)　　　Status of input reference source <I-1> (7:4)　　　Status of input reference source <I_2>	01000100
11		(3:0)　　　Status of input reference source <I_3> (7:4)　　　Status of input reference source <I_4>	01100110
12		(3:0)　　　Status of input reference source <I_5> (7:4)　　　Status of input reference source <I_6>	01100110
13		(3:0)　　　Status of input reference source <I_7> (7:4)　　　Status of input reference source <I_8>	01000100
14		(3:0)　　　Status of input reference source <I_9> (7:4)　　　Status of input reference source <I_10>	01000100
15		(3:0)　　　Status of input reference source <I_11> (7:4)　　　Status of input reference source <I_12>	01000100
16		(3:0)　　　Status of input reference source <I_13> (7:4)　　　Status of input reference source <I_14>	01000100

Addr. (Hex)	Parameter Name	Description	Default Value (bin)
	cnfg_ref_selection_priority	This is a 7-byte register which holds the priority of each of the 14 input reference sources. The priority values are all relative to each other, with lower-valued numbers taking higher priorities. Only the values 1 to 15 (dec) are valid - 0 disables the reference source. Each reference source should be given a unique number, however two sources given the same priority number will be assigned on a first in first out basis.

It is sensible to reserve the value '1' in case it is necessary to re-order the priorities on the fly - therefore, the range 2 to 15 would normally be used (in a slave device, the value 1 is automatically used for the protection source, input #11). All values should be in hexadecimal.

The organisation of the register is shown below and in the register map.

* The default value given is valid when MSTSLVB pin is left unconnected or tied high. If MSTSLVB is tied low, the default value is DC (hex).

Bit   Content | |
18		(3:0) Programmed priority of input reference source <I_1> (7:0) Programmed priority of input reference source <I_2>	00110010
19		(3:0) Programmed priority of input reference source <I_3> (7:4) Programmed priority of input reference source <I_4>	01010100
1A		(3:0) Programmed priority of input reference source <I_5> (7:4) Programmed priority of input reference source <I_6>	01110110
1B		(3:0) Programmed priority of input reference source <I_7> (7:4) Programmed priority of input reference source <I_8>	10011000
1C		(3:0) Programmed priority of input reference source <I_9> (7:4) Programmed priority of input reference source <I_10>	10111010
1D		(3:0) Programmed priority of input reference source <I_11> (7:4) Programmed priority of input reference source <I_12>	11010001*
1E		(3:0) Programmed priority of input reference source <I_13> (7:4) Programmed priority of input reference source <I_14>	11111110
	cnfg_ref_source_frequency	This is a 14-byte register which holds the keys to the frequencies of each of the 14 input reference sources, as listed below.

Bits (3:0) of each byte define the frequency of the reference source in accordance with the following key:
0000   8 kHz
0001   1544 kHz (SONET) / 2048 kHz (SDH) (As defined by Register 34, bit 2)
0010   6.48 MHz
0011   19.44 MHz
0100   25.92 MHz
0101   38.88 MHz
0110   51.84 MHz
0111   77.76 MHz
1000   155.52 MHz
1001   2 kHz
1010   4 kHz

Bits (5:4) of each byte together define which leaky bucket settings (0-3) are used, as defined in registers 50 (hex) to 5F (hex).

Bits (7:6) of each byte define the operation undertaken on the input frequency, in accordance with the following key:
00   The input frequency is fed directly into the DPLL.
01   The input frequency is internally divided down to 8 kHz, before being fed into the DPLL. This gives excellent jitter tolerance.
10   Unsupported configuration - do not use.
11   Uses the division coefficient stored in register cnfg_freq_divn to divide the input by this value prior to going to the DPLL. The frequency monitors must be disabled. The divided down frequency should equal 8kHz. The frequency (3:0) should be set to the nearest spot frequency just below the actual input frequency. The DivN feature works for input frequencies between 1.544 MHz and 100 MHz.

* The default value given is valid when MSTSLVB pin is left unconnected or tied high. If MSTSLVB is tied low, the default value is 03 (hex). | |
20		Frequency of reference source <I_1> - fixed at 00000000 for 8kHz only	00000000
21		Frequency of reference source <I_2> - fixed at 00000000 for 8kHz only	00000000
22		Frequency of reference source <I_3>	00000000
23		Frequency of reference source <I_4>	00000000

Addr. (Hex)	Parameter Name	Description	Default Value (bin)
24		Frequency of reference source <l_5>	00000011
25		Frequency of reference source <l_6>	00000011
26		Frequency of reference source <l_7>	00000011
27		Frequency of reference source <l_8>	00000011
28		Frequency of reference source <l_9>	00000011
29		Frequency of reference source <l_10>	00000011
2A		Frequency of reference source <l_11>	00000010*
2B		Frequency of reference source <l_12>	00000001
2C		Frequency of reference source <l_13>	00000001
2D		Frequency of reference source <l_14>	00000001
	cnfg_sts_remote_sources_valid	This 14-bit register holds the status of the reference sources supplied to another device.It is a copy of the other device's sts_sources_valid register. The register is part of the protection mechanism. The register is organised as follows:	
30		Bit Reference source (7:0) <l_8>:<l_1>	11111111
31		Bit Reference source (5:0) <l_14>:<l_9> (7:6) unused	XX111111
32	cnfg_operating_mode	This 3-bit register occupies the entire 8-bit space at address 32(hex). It is used to force the device into a desired operating state, represented by the binary values shown in Figure 8. Value 0 (hex) allows the control state machine to operate automatically. Bit Reference source (2:0) Desired operating state (as per Figure 8) (7:3) Unused	XXXXX000
33	cnfg_ref_selection	This 4-bit register occupies the entire 8-bit space at address 33(hex). It is used to force the device to select a particular input reference source, irrespective of its priority. Writing to this register temporarily raises the selected input to priority '1'. Provided no other input is already programmed with priority '1', and revertive mode is on, this source will be selected, if it has been validated by the frequency and activity monitors. Writing X0(hex) or XF(hex) will disable all input reference sources. * The default is XF. Bit Information (3:0) Desired reference source (7:4) Unused	XXXX1111*
34	cnfg_mode	This 7-bit register occupies the entire 8-bit space at address 34(hex). It contains several individual configuration fields, as detailed below: Bit 0 = 0 Non-revertive Mode: The device will retain the presently selected source. This is the default state. = 1 Revertive Mode: The device will switch to the highest priority source available shown in the sts_priority_table register(7:4) (at address 0A(hex)). Bit 1 = 0 Slave Mode:The device will adopt the slave mode and will follow the master device. = 1 Master Mode:The device will adopt the master mode and make the active decisions of which source to select, etc. This bit is writeable, but its default value is determined by the pin, MSTSLVB.	11001000

Addr. (Hex)	Parameter Name	Description	Default Value (bin)
34 cont	cnfg_mode	**Bit 2** = 0 SDH Mode:The device expects the input frequency of any input channel given the value '0001' in the cnfg_ref_source_frequency register to be 2048 kHz. This bit is writeable, but its default value is determined by the pin, SONSDHB. = 1 SONET Mode:The device expects the input frequency of any input channel given the value '0001' in the cnfg_ref_source_frequency register to be 1544 kHz. This bit is writeable, but its default value is determined by the pin, SONSDHB. **Bit 3** = 0 External 2 kHz Sync Disable: The device will ignore the Sync2k pin. = 1 External 2 kHz Sync Enable: The device will align the phase of its internally-generated Frame Sync signal (8 kHz) and Multi-Frame Sync signal (2 kHz) with that of the signal supplied to the Sync2K pin. The device should be locked to a 6.48 MHz output from another ACS8510. This is the default state. **Bit 4** = 0 Holdover Offset Disable: The device will ignore the value and holdover will use the current PLL integral path value. This is the default state. = 1 Holdover Offset Enable: The device will adopt the Holdover Offset value stored in the cnfg_holdover_offset register. This value is then used to set the frequency in Holdover mode. **Bit 5** = 0 Falling Clock Edge Selected: The device will reference to the falling edge of the external oscillator signal. This is the default state. = 1 Rising Clock Edge Selected: The device will reference to the rising edge of the external oscillator signal. **Bit 6** = 0 Phase Alarm Timeout Disable: The phase alarm will not timeout and must be reset externally. = 1 Phase Alarm Timeout Enable: The phase alarm will time out after 100 seconds. This is the default state. **Bit 7** = 0 Auto 2 kHz Sync Disable:The user controls this function using bit 3 of this register, as described above. = 1 Auto 2 kHz Sync Enable: External 2 kHz Sync will be enabled only when the source is locked to 6.48 MHz. Otherwise it will be disabled. This is the default state.	11001000

35	cnfg_T4	This 6-bit register occupies the entire 8-bit space at address 35(hex). It contains several individual configuration fields, as detailed below:
		
		Bit Configuration field
		(3:0) T_{IN1} input source selection
		4 '1' = Select T_{OUT0}
		    '0' = Select T_{IN1}
		5 '1' = Squelch
		    '0' = Non-Squelch (Default)
		6 Unused
		7 Unused
		
		T_{IN1} input source selection: The device will switch to the source shown in this field for the generation of the T_{OUT4} signal. If '0' it will select the highest priority active T_{IN1}.
		
		Select T_{OUT0}/T_{IN1}: The device will generate the T_{OUT4} signal from the T_{OUT0} path or the T_{IN1} path, according to the status of this bit.
		
		Squelch/Non-Squelch: If this bit is set high the device will squelch the T_{OUT4} signal, causing it to stop toggling and remain at either '1' or '0', If set low it will not squelch the T_{OUT4} signal.
			XX000000

36	cnfg_differential_inputs	This 2-bit register occupies the entire 8-bit space at address 36(hex). It contains two individual configuration fields, as detailed below:
		
		Bit Configuration field
		0 '1' = Input <I_5> is PECL-compatible
		    '0' = Input <I_5> is LVDS-compatible (Default)
		1 '1' = Input <I_6> is PECL-compatible (Default)
		    '0' = Input <I_6> is LVDS-compatible
		(7:2) Unused
			XXXXXX10

Addr. (Hex)	Parameter Name	Description	Default Value (bin)
37	cnfg_uPsel_pins	This 3-bit register occupies the entire 8-bit space at address 37(hex). It holds the key for the selection of the microprocessor type. It is read-only, the value being applied on the uPSel pins and adopted on power-up or reset. After power-up the pins are ignored but can still be read via this register. Bit (2:0) Microprocessor type 000 OFF (interface disabled) 001 EPROM 010 MULTIPLEXED 011 INTEL 100 MOTOROLA 101 SERIAL 110 OFF (interface disabled) 111 OFF (interface disabled)	Bits(7:3)= XXXXX Bits(2:0)= Pin dependent

38	cnfg_T0_output_enable	This 8-bit register occupies the entire 8-bit space at address 38(hex). It contains several individual configuration fields, as detailed below:
		
		Bit Configuration field
		0 '1' = Output port T05 enabled (77.76 MHz)
		         '0' = Output port T05 disabled
		
		1 '1' = Output port T04 enabled (38.88 MHz)
		         '0' = Output port T04 disabled
		
		2 '1' = Output port T03 enabled (19.44 MHz)
		         '0' = Output port T03 disabled
		
		3 '1' = Output port T02 enabled
		         '0' = Output port T02 disabled
		         - see register cnfg_T0_output_frequencies
		
		4 '1' = Output port T01 enabled
		         '0' = Output port T01 disabled
		         - see register cnfg_T0_output_frequencies
		
		5 '1' = Sonet mode selected for Dig1
		         '0' = SDH mode selected for Dig1
		         - see register cnfg_T0_output_frequencies
		
		6 '1' = Sonet mode selected for Dig2
		         '0' = SDH mode selected for Dig2
		         - see register cnfg_T0_output_frequencies
		
		7 '1' = T06 output frequency set to 311.04 MHz
		         '0' = T06 output frequency set by Address 3A (5:4)
		
		Note: "Disabled" means that the output port holds a static logic value (the port is not Tri-stated).
			00011111

39	cnfg_T0_output_frequencies	This register holds the frequency selections for each output port, as detailed below. Bit Configuration field Bit Configuration field (1:0) T01 (3:2) T02 00 6.48 MHz* 00 25.92 MHz 01 25.92 MHz 01 51.84 MHz 10 19.44 MHz 10 38.88 MHz* 11 Dig1 11 Dig2 (5:4) Dig1 (7:6) Dig2 00 1544 kHz/2048 kHz* 00 1544 kHz/2048 kHz* 01 3088 kHz/4096 kHz 01 3088 kHz/4096 kHz 10 6176 kHz/8192 kHz 10 6176 kHz/8192 kHz 11 12352 kHz/16384 kHz 11 12352 kHz/16384 kHz * = default - For both Dig1 and Dig2, the left most frequency values are for Sonet mode and the others are for SDH mode. They are selected via the SONET/SDH bits in register cnfg_T0_output_enable.	00001000

Addr. (Hex)	Parameter Name	Description	Default Value (bin)
3A	cnfg_differential_outputs	This register holds the frequency selections and the port-technology type for the differential outputs, T06 and T07, as detailed below. Bit Configuration field Bit Configuration field (1:0) T06 (3:2) T07 00 Port disabled 00 Port disabled 01 PECL-compatible 01 PECL-compatible* 10 LVDS-compatible* 10 LVDS-compatible 11 unused 11 unused (5:4) T06 (7:6) T07 00 38.88 MHz* 00 155.52 MHz 01 19.44 MHz 01 51.84 MHz 10 155.52 MHz 10 77.76 MHz 11 Dig1. 11 19.44 MHz* * = default	11000110

3B	cnfg_bandwidth	This register contains information used to control the operation of the digital PLL. When bandwidth selection is set to automatic, the DPLL will use the acquisition bandwidth setting when out of lock, and the normal/locked bandwidth setting when in lock. When set to manual, the DPLL will alway use the normal/locked bandwidth setting.
		
		Bit (2:0) Loop bandwidth (6:4) Acquisition bandwidth
		000 0.1 Hz 000 0.1 Hz
		001 0.3 Hz 001 0.3 Hz
		010 0.6 Hz 010 0.6 Hz
		011 1.2 Hz 011 1.2 Hz
		100 2.5 Hz 100 2.5 Hz
		101 5.0 Hz 101 5.0 Hz
		110 10 Hz 110 10 Hz
		111 20 Hz 111 20 Hz
		
		3 unused 7 Bandwidth selection
		      '0'= Manual operation
		      '1'= Automatic operation
			0111X101

	cnfg_nominal_frequency	This register holds a 16 bit unsigned integer representing the desired nominal frequency. This is available to optionally calibrate the nominal output frequency to compensate against variation in the external crystal frequencies.	
3C		Least-significant byte.	10011001
3D		Most-significant byte.	10011001
	cnfg_holdover_offset	This 16-bit register uses addresses 3E(hex) to 40(hex). It holds a 16 bit signed integer, representing the holdover offset value, which can be used to set the holdover mode frequency when enabled via the holdover offset enabled bit in the cnfg_mode register.	
3E		Bit (7:0) Holdover offset (7:0)	00000000
3F		Bit (7:0) Holdover offset (15:8)	00000000
40		Bit (2:0) Holdover offset (18:16) Bit 7 is Auto Holdover Averaging enable - default 1. This enables the frequency average to be taken from 32 samples. One sample taken every 32 seconds, after the frequency has been confirmed to be in-band by the frequency monitors, giving a 17 minute history of the currently locked to reference source for use in Holdover. Bit (6:3) Unused	1XXXX000

	cnfg_freq_limit	This register holds a 10 bit unsigned integer representing the pull-in range of the DPLL. It should be set according to the accuracy of crystal implemented in the application, using the following formula:
		      Frequency range +/- (ppm) = (cnfg_freq_limit x 0.0785)+0.01647 or
		      cnfg_freq_limit = (Frequency range - 0.01647) / 0.0785
		
		Default value when SRCSW is left unconnected or tied low is ±9.2 ppm. Default value when SRCSW is high isthe full range of around ±80 ppm.	

41		Least significant byte	01110110 (SRCSW low) 11111111 (SRCSW high)
42		(7:2) Unused (1:0) Most significant byte	XXXXXX00 (SRCSW low) XXXXXX11 (SRCSW high)

Addr. (Hex)	Parameter Name	Description	Default Value (bin)
43	cnfg_interrupt_mask	Each bit of this 21 bit register, if set to zero, will disable the appropriate interrupt source in either the interrupt status register or the sts_T4_inputs register.	11111111
44			11111111
45			XXX11111
	cnfg_freq_divn	This 14 bit integer is used as the divisor for any input applied to <I_14>:<I_1> to get the phase locking frequency desired. Only active for inputs with the DivN bit set to '1'. This will cause the input frequency to be divided by (N+1) prior to phase comparison, e.g. program N to: ((input freq)/ 8 kHz) -1 The reference_source_frequency bits should be set to reflect the closest spot frequency to the input frequency, but must be lower than the input frequency.	
46		Least-significant byte.	00000000
47		Most-significant 6 bits.	XX000000
48	cnfg_monitors	This 7 bit register allows global configuration of monitors and control of phase build out. Bits (1:0) are for configuring frequency monitors- 00 = off, 01 = 15 ppm, others are reserved for future use. Bit 2 Phase buildout en enables phasebuildout. If disabled, the DPLL will always lock to 0 degrees. Bit 3 Freeze phase buildout (when phase buildout is enabled) will effectively disable any future phase buildout events but remain with the current phase offset. Bit 4 External protection switching enables the SrcSwit pin to force the locking to either input 4 or 3. Bit 5 Ultra-fast switching enables the dpll to raise an inactivity alarm on the currently selected source after missing only a few cycles. This will enable very fast switching away from the selected source in a protection type application. This is triggered by the main_ref_failed interrupt mechanism. Bit 6 Flag reference loss on TDO will enable the value of the main_ref_failed interrupt to be driven out of the TDO pin of the device. * The default value given is valid when SRCSWT pin is left unconnected or tied low. If SRCSWT is tied high, the default value is 15 (hex).	X0000101*
50	cnfg_activ_upper_threshold0	This 8 bit register sets the value in the leaky bucket that causes the activity alarm to be raised.	00000110
51	cnfg_activ_lower_threshold0	This 8 bit register sets the value in the leaky bucket that causes the activity alarm to be cleared.	00000100
52	cnfg_bucket_size0	This 8 bit register sets the maximum value that the leaky bucket can reach given an inactive input.	00001000
53	cnfg_decay_rate0	This 2 bit register controls the leak rate of the leaky bucket. The fill-rate of the bucket is +1 for every 128 ms interval that has experienced some level of inactivity. The decay rate is programmable in ratios of the fill rate. The ratio can be set to 1:1, 2:1, 4:1, 8:1 by using values of 00, 01, 10, 11 respectively. However, these buckets are not 'true' leaky buckets in nature. The bucket stops 'leaking' when it is being filled. This means that the fill and decay rates can be the same (00 = 1:1) with the net effect that an active input can be recognised at the same rate as an inactive one.	XXXXXX01
54	cnfg_activ_upper_threshold1	This 8 bit register sets the value in the leaky bucket that causes the activity alarm to be raised.	00000110
55	cnfg_activ_lower_threshold1	This 8 bit register sets the value in the leaky bucket that causes the activity alarm to be cleared.	00000100
56	cnfg_bucket_size1	This 8 bit register sets the maximum value that the leaky bucket can reach given an inactive input.	00001000
57	cnfg_decay_rate1	As for register 53(hex) but for bucket 1.	XXXXXX01

Addr. (Hex)	Parameter Name	Description	Default Value (bin)
58	cnfg_activ_upper_threshold2	This 8 bit register sets the value in the leaky bucket that causes the activity alarm to be raised.	00000110
59	cnfg_activ_lower_threshold2	This 8 bit register sets the value in the leaky bucket that causes the activity alarm to be cleared.	00000100
5A	cnfg_bucket_size2	This 8 bit register sets the maximum value that the leaky bucket can reach given an inactive input.	00001000
5B	cnfg_decay_rate2	As for register 53(hex) but for bucket 2.	XXXXXX01
5C	cnfg_activ_upper_threshold3	This 8 bit register sets the value in the leaky bucket that causes the activity alarm to be raised.	00000110
5D	cnfg_activ_lower_threshold3	This 8 bit register sets the value in the leaky bucket that causes the activity alarm to be cleared.	00000100
5E	cnfg_bucket_size3	This 8 bit register sets the maximum value that the leaky bucket can reach given an inactive input.	00001000
5F	cnfg_decay_rate3	As for register 53(hex) but for bucket 3.	XXXXXX01
7F	cnfg_uPsel	This 3 bit register is used to control the mode of the microprocessor interface. This will power-up with the value on the µPsel pins. Subsequently, the register can be written to put the micro-processor interface into another mode. This will support booting from EPROM and subsequently communicating via another mode. The value on the pins can always be read via the cnfg_uPsel_pins register. These 3 pins can be used as general purpose inputs for the µP if necessary after booting.	Bits(7:3)= XXXXX Bits(2:0)= Pin dependent

Selection of Input Reference Clock Source

Under normal operation, the input reference sources are selected automatically by an order of priority. But, for special circumstances, such as chip or board testing, the selection may be forced by configuration.

Automatic operation selects a reference source based on its pre-defined priority and its current availability. A table is maintained which lists all reference sources in the order of priority. This is initially downloaded into the ACS8510 via the micro-processor interface by the Network Manager, and is subsequently modified by the results of the ongoing quality monitoring. In this way, when all the defined sources are active and valid, the source with the highest programmed priority is selected but, if this source fails, the next-highest source is selected, and so on.

Restoration of repaired reference sources is handled carefully to avoid inadvertent disturbance of the output clock. The ACS8510 has two modes of operation; Revertive and Non-Revertive. In Revertive mode, if a re-validated (or newly validated) source has a higher priority than the reference source which is currently selected, a switch over will take place. Many applications prefer to minimise the clock switching events and choose Non-Revertive mode. In Non-Revertive mode , when a re-validated (or newly validated) source has a higher priority then the selected source will be maintained. The re-validation of the reference source will be flagged in the sts_sources_valid register and, if not masked, will generate an interrupt. Selection of the re-validated source can only take place under software control - the software should briefly enable Revertive mode to affect a switch-over to the higher priority source. If the selected source fails under these conditions the device will still not select the higher priority source until instructed to do so by the software, by briefly setting the Revertive mode bit. When there is a reference available with higher priority than the selected reference, there will be NO change of reference source as long as the Non-Revertive mode remains on. This is the case even of there are lower priority references available or the currently selected reference fails. When the ONLY valid reference sources that are available

have a lower priority than the selected reference, a failure of the selected reference will always trigger a switch-over regardless of whether Revertive or Non-revertive mode has been chosen.

Also, in a Master/Slave redundancy-protection scheme, the Slave device(s) must follow the Master device. The alignment of the Master and Slave devices is part of the protection mechanism. The availability of each source is determined by a combination of local and remote monitoring of each source. Each input reference source supplied to each ACS8510 device is monitored locally and the results are made available to other devices.

Forced Control Selection

A configuration register, 'cnfg_ref_selection', controls both the choice of automatic or forced selection and the selection itself (when forced selection is required). The forced selection of an input reference source occurs when the 'cnfg_ref_selection' variable contains a non-zero value, the value then representing the input port required to be selected. This is not the normal mode of operation, and the 'cnfg_ref_selection' variable is defaulted to the all-zero value on reset, thereby adopting the automatic selection of the reference source.

Automatic Control Selection

When an automatic selection is required, the 'cnfg_ref_selection' register must be set to all-zero. The configuration registers, 'cnfg_ref_selection_priority', held in the µP port block, consists of seven, 8 bit registers organised as one 4 bit register per input reference port. Each register holds a 4-bit value which represents the desired priority of that particular port. Unused ports should be given the value, '0000' or '1111', in the relevant register to indicate they are not to be included in the priority table. On power-up, or following a reset, the whole of the configuration file will be defaulted to the values defined by Table 1. The

selection priority values are all relative to each other, with lower-valued numbers taking higher priorities. Each reference source should be given a unique number, the valid values are 1 to 15 (dec). A value of 0 disables the reference source. However if two or more inputs are given the same priority number those inputs will be selected on a first in, first out basis. If the first of two same priority number sources goes invalid the second will be switched in. If the first then becomes valid again, it becomes the second source on the first in, first out basis, and there will not be a switch. If a third source with the same priority number as the other two becomes valid, it joins the priority list on the same first in, first out basis. There is no implied priority based on the channel numbers.

The input port <I_11> is for the connection of the synchronous clock of the T_{OUT0} output of the Master device (or the active-Slave device), to be used to align the T_{OUT0} output with the Master (or active-Slave) device if this device is acting in a subordinate-Slave or subordinate-Master role.

Clock Quality Monitoring

Clock quality is monitored and used to modify the priority tables of the local and remote ACS8510 devices. The following parameters are monitored:

- Activity (toggling)

- Frequency (This monitoring is only performed when there is no irregular operation of the clock or loss of clock condition)

In addition, input ports <I_1> and <I_2> carry AMI-encoded composite clocks which are monitored by the AMI-decoder blocks. Loss of signal is declared by the decoders when either the signal amplitude falls below 0.3 v or there is no activity for 1 ms.

Any reference source which suffers a loss-of-

signal, loss-of-activity, loss-of-regularity or clock-out-of-band condition will be declared as unavailable.

Clock quality monitoring is a continuous process which is used to identify clock problems. There is a difference in dynamics between the selected clock and the other reference clocks. Anomalies occurring on non-selected reference sources affect only that source's suitability for selection, whereas anomalies occurring on the selected clock could have a detrimental impact on the accuracy of the output clock.

Anomalies, whether affecting signal-purity or signal frequency, could induce jitter or frequency offsets in the output clock, leading to anomalous behaviour. Anomalies on the selected clock, therefore, have to be detected as they occur and the phase locked loop must be temporarily isolated until the clock is once again pure. The clock monitoring process cannot be used for this because the high degree of accuracy required dictates that the process be slow. To achieve the immediacy required by the phase locked loop requires an alternative mechanism. The phase locked loop itself contains appropriate circuitry, based around the

phase detector, and isolates itself from the selected reference source as soon as a signal impurity is detected. It can likewise respond to frequency offsets outside the permitted range since these result in saturation of the phase detector. When the phase locked loop is isolated from the reference source, it is essentially operating in a Hold-Over state; this is preferable to feeding the loop with a standby source, either temporarily or permanently, since excessive phase excursions on the output clock are avoided.

Anomalies detected by the phase detector are integrated in a leaky bucket accumulator. Occasional anomalies do not cause the accumulator to cross the alarm-setting threshold, so the selected reference source is retained. Persistent anomalies cause the alarm-setting threshold to be crossed and result in the selected reference source being rejected.

Activity Monitoring

The ACS8510 has a combined inactivity and irregularity monitor. The ACS8510 uses a "leaky bucket" accumulator, which is a digital circuit which mimics the operation of an analog integrator, in which input pulses increase the

Figure 7: Inactivity and irregularity monitoring
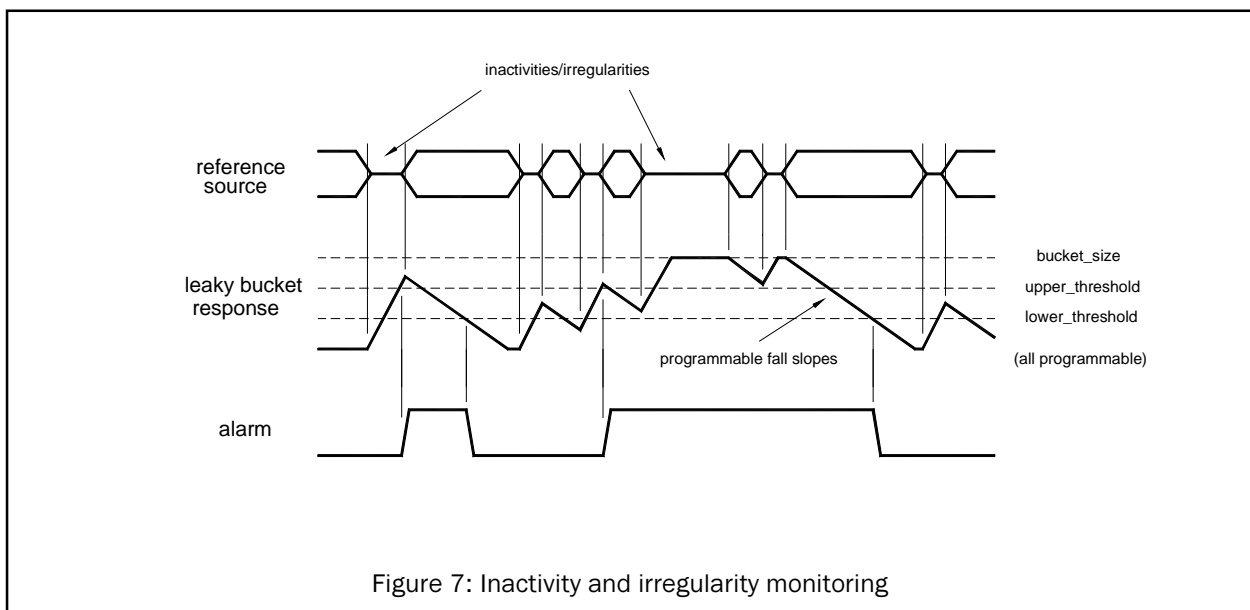
output amplitude but die away over time. Such integrators are used when alarms have to be triggered either by fairly regular defect events, which occur sufficiently close together, or by defect events which occur in bursts. Events which are sufficiently spread out should not trigger the alarm. By adjusting the alarm-setting threshold, the point at which the alarm is triggered can be controlled. The point at which the alarm is cleared depends upon the decay rate and the alarm-clearing threshold. On the alarm-setting side, if several events occur close together, each event adds to the amplitude and the alarm will be triggered quickly; if events occur a little more spread out, but still sufficiently close together to overcome the decay, the alarm will be triggered eventually. If events occur at a rate which is not sufficient to overcome the decay, the alarm will not be triggered. On the alarm-clearing side, if no defect events occur for a sufficient time, the amplitude will decay gradually and the alarm will be cleared when the amplitude falls below the alarm-

clearing threshold. The ability to decay the amplitude over time allows the importance of defect events to be reduced as time passes by. This means that, in the case of isolated events, the alarm will not be set, whereas, once the alarm becomes set, it will be held on until normal operation has persisted for a suitable time (but if the operation is still erratic, the alarm will remain set). See Figure 7.

The "leaky bucket" accumulators are programmable for size, alarm set & reset thresholds and decay rate. Each source is monitored over a 128 ms period. If, within a 128 ms period, an irregularity occurs that is not deemed to be due to allowable jitter/wander, then the accumulator is incremented. The accumulator will continue to increment up to the point that it reaches the programmed bucket size. The "fill rate" of the leaky bucket is, therefore, 8 units/second. The "leak rate" of the leaky bucket is programmable to be in multiples of the fill rate (x1, x0.5, x0.25 and x0.125) to give a programmable leak rate from

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Leaky bucket timing

The time taken to raise an inactivity alarm on a reference source that has previously been fully active (leaky bucket empty) will be:

$$\frac{(\text{cnfg\_activ\_upper\_threshold N})}{8} \text{ secs}$$

where N is the number of the relevent leaky bucket configuration. If an input is intermittently inactive then this time can be longer. The default setting of cnfg_activ_upper_threshold is 6, therefore the default time is 0.75 s.

The time taken to cancel the activity alarm on a previously completely inactive reference source is calculated as:

$$\frac{2^{(\text{cnfg\_decay\_rate N})} \times ((\text{cnfg\_bucket\_size N}) - (\text{cnfg\_activ\_lower\_thrshold N}))}{8} \text{ secs}$$

where N is the number of the relevent leaky bucket configuration in each case. The default setting are shown in the following:

$$\frac{2^{1} \times (8\text{-}4)}{8} = 1.0 \text{ s}$$

8 units/sec down to 1 unit/sec. A conflict between trying to 'leak' at the same time as a 'fill' is avoided by preventing a 'leak' when a 'fill' event occurs.

Disqualification of a non-selected reference source is based on inactivity, or on an out of band result from the frequency monitors. The currently selected reference source can be disqualified for phase, frequency, inactivity or if the source is outside the DPLL lock range. If the currently selected reference source is disqualified, the next highest priority, active reference source is selected.

Ultra Fast Switching

A reference source is normally disqualified after the leaky bucket monitor thresholds have been crossed. An option for a faster disqualification has been implemented, whereby if register 48H, bit 5 (Ultra Fast Switching), is set then a loss of activity of just a few reference clock cycles will set the 'no activity alarm' and cause a reference switch. This can be chosen to cause an interrupt to occur instead of or as well as causing the reference switch.

The sts_interrupts register 05 Hex Bit 15 (main_ref_failed) of the interrupt status register is used to flag inactivity on the reference that the device is locked to much faster than the activity monitors can support. If bit 6 of the cnfg_monitors register (flag ref loss on TDO) is set, then the state of this bit is driven onto the TDO pin of the device.

The flagging of the loss of the main reference failure on TDO is simply allowing the status of the sts_interrupt bit 15 to be reflected in the state of the TDO output pin. The pin will, therefore remain High until the interrupt is cleared. This functionality is not enabled by default so the usual JTAG functions can be used. When JTAG is normally used straight out of power-up, then this feature will have no bearing on the functionality. The TDO flagging feature will need to be disabled if JTAG is not

enabled on power-up and the feature has since been enabled.

When the TDO output from the ACS8510 is connected to the TDI pin of the next device in the JTAG scan chain, the implementation should be such that a logic change caused by the action of the interrupt on the TDI input should not effect the operation when JTAG is not active.

External Protection Switching

Fast external switching between inputs <I_3> and <I_4> can also be triggered directly from a dedicated pin (SRCSW). This mode can be activated either by holding this pin high during reset, or by writing to bit 4 of register address 48Hex. Once external protection switching is enabled, then the value of this pin directly selects either <I_3> (SRCSW high) or <I_4> (SRCSW low). If this mode is activated at reset by pulling the SRCSW pin high, then it configures the default frequency tolerance of <I_3> and <I_4> to +/- 80 ppm (register address 41Hex and 42Hex). Any of these registers can be subsequently set by external software if required.

When external protection switching is enabled, the device will operate as a simple switch. All clock monitoring is disabled and the DPLL will simply be forced to try to lock on to the indicated reference source.

Frequency Monitoring

The ACS8510 performs frequency monitoring to identify reference sources which have drifted outside the acceptable frequency range of +/- 16.6 ppm (measured with respect to the output clock). The *sts_reference sources* out-of-band alarm for a particular reference source is raised when the reference source is outside the acceptable frequency range. The ACS8510 DPLL has a programmable frequency limit of +/- 80 ppm. If the range is programmed to be > 16.6 ppm, the activity monitors should be

disabled so the input reference source is not automatically rejected as out of frequency range.

Modes of Operation

The ACS8510 has three primary modes of operation (Free-Run, Locked and Holdover) supported by three secondary, temporary modes (Pre-Locked, Lost_Phase and Pre-Locked2). These are shown in the State Transition Diagram, Figure 8.

The ACS8510 can operate in Forced or Automatic control. On reset, the ACS8510 reverts to Automatic Control, where transitions between states are controlled completely automatically. Forced Control can be invoked by configuration, allowing transitions to be performed under external control. This is not the normal mode of operation, but is provided for special occasions such as testing, or where a high degree of hands-on control is required.

Free-Run mode

The Free-Run mode is typically used following a power-on-reset or a device reset before network synchronisation has been achieved. In the Free-Run mode, the timing and synchronisation signals generated from the ACS8510 are based on the Master clock frequency provided from the external oscillator and are not synchronised to an input reference source. The frequency of the output clock is a fixed multiple of the frequency of the external oscillator, and the accuracy of the output clock is equal to the accuracy of the Master clock.

The transition from Free-Run to Pre-locked(1) occurs when the ACS8510 selects a reference source.

Pre-Locked(1) mode

The ACS8510 will enter the Locked state in a maximum of 100 seconds, as defined by GR-1244-CORE specification, if the selected reference source is of good quality. If the

device cannot achieve lock within 100 seconds, it reverts to Free-Run mode and another reference source is selected.

Locked mode

The Locked mode is used when an input reference source has been selected and the PLL has had time to lock. When the Locked mode is achieved, the output signal is in phase and locked to the selected input reference source. The selected input reference source is determined by the priority table. When the ACS8510 is in Locked mode, the output frequency and phase follows that of the selected input reference source. Variations of the external crystal frequency have a minimal effect on the output frequency. Only the minimum to maximum frequency range is affected. Note that the term, 'in phase', is not applied in the conventional sense when the ACS8510 is used as a frequency translator (e.g., when the input frequency is 2.048 MHz and the output frequency is 19.44 MHz) as the input and output cycles will be constantly moving past each other; however, this variation will itself be cyclical over time unless the input and output are not locked.

Lost_Phase mode

Lost_Phase mode is used whenever the selected reference source suffers most kinds of anomalous behaviour. Clock generation is performed in the same way as in the Holdover mode. If the leaky bucket accumulator calculates that the anomaly is serious, the device rejects the reference source and one of the following transitions takes place:

Go to Pre-Locked(2);

   - If a known-good standby source is available.

Go to Hold-Over;

   - If no standby sources are available.

Holdover mode

The Holdover mode is used when the ACS8510 was in Locked mode for long enough to acquire stable frequency data, but the final selected reference source has become unavailable and a replacement has not yet been qualified for selection.

In Holdover mode, the ACS8510 provides the timing and synchronisation signals to maintain the Network Element (NE), but they are not phase locked to any input reference source. The timing is based on a stored value of the frequency ratio obtained during the last Locked mode period.

The Holdover performance is mainly limited by what is happening to the TCXO. The ACS8510 has 3 ways of determining Holdover, either;

1. By external frequency setting (cnfg_holdover_offset register)

2. By an internal frequency measuring and averaging system which averages the last 20 minutes

3. By just using the last frequency (as reported by the sts_curr_inc_offset register). This value can be read out of the device and used to build up a longer term average using an external averaging circuit. This value can then to readback into the device and used as the Holdover offset (via cnfg_holdover_offset register).

By default it uses the internal averager. This means that if the TCXO frequency is varying due to temperature fluctuations in the room, then the instantaneous value can be different from the average value, and then it may be possible to exceed the 0.05 ppm limit (depending on how extreme the temperature flucuations are). It is advantageous to shield the TCXO to slow down frequency changes due to drift and external temperature fluctuations.

The frequency accuracy of Holdover mode has to meet the ITU-T, ETSI and Telcordia performance requirements. The performance of the external oscillator clock is critical in this mode, although only the frequency stability is important - the stability of the output clock in Hold-Over is directly related to the stability of the external oscillator.

Pre-Locked(2) mode

This state is very similar to the Pre-Locked(1) state. It is entered from the Holdover state when a reference source has been selected and applied to the phase locked loop. It is also entered if the device is operating in revertive mode and a higher-priority reference source is restored.

Upon applying a reference source to the phase locked loop, the ACS8510 will enter the Locked state in a maximum of 100 seconds, as defined by GR-1244-CORE specification, if the selected reference source is of good quality.

If the device cannot achieve lock within 100 seconds, it reverts to Holdover mode and another reference source is selected.

Protection Facility

The ACS8510 supports redundancy protection. The primary functions of this include:

- Alignment of the priority tables of both Master and Slave ACS8510 devices so as to align the selection of reference sources of both Master and Slave ACS8510 devices.

- Alignment of the phases of the 8 kHz and 2 kHz clocks in both Master and Slave ACS8510 devices to within one cycle of the 77.76 MHz internal clock.

When two ACS8510 devices are to be used in a redundancy-protection scheme within an NE, one will be designated as the Master and the other as the Slave. It is expected that an NE will use the T_{OUT0} output for its internal operations because the T_{OUT4} output is intended to feed an SSU/BITS system. An SSU/BITS will not be bothered by phase differences between

signals arriving from different sources because it typically incorporates line build-out functions to absorb phase differences on reference inputs. This means that the phasing of the composite clocks between two ACS8510 devices do not have to be mutually-aligned. The same is not true, however, of the T_{OUT0} output signals (T_{01} - T_{07}, Frame clock and Multi-Frame clock). It is usually important to align the phases of all equivalent T_{OUT0} signals generated by different sources so that switch-over from one device to another does not affect the internal operations of the NE. Both ACS8510 devices will produce the same signals, which will be routed around the NE to the various consumers (clock sinks). With the possible exception of a through-timing mode, the signals from the Master device will be used by all consumers, unless the Master device fails, when each consumer will switch over to the signals generated by the Slave device.

Switchover to a new T_{OUT0} clock should be as hitless as possible. This requires the signals of both ACS8510 devices to be phase aligned at each consumer. Phase alignment requires frequency alignment. To ensure that both devices can generate output clocks locked to the same source, both devices are supplied with the same reference sources on the same input ports and will have identical priority tables. Failures of selected reference sources will result in both ACS8510 devices making the same updates to their priority tables as availability information will be updated in both devices. Although, in principle, the priority tables will be the same if the same reference sources are used on the same input port on each device, in practice, this is only true if the reference sources actually arrive at each device - failures of a source seen only by one device and not by the other, such as could be caused, for example, by a backplane connector failure, would result in the priority tables becoming misaligned. It is thus necessary to force the priority tables to

be aligned under normal operating conditions so that the devices can make the same decisions - this can be achieved by loading the availability seen by one device (via the *sts_reference_sources* register) into the *cnfg_sts_remote_sources_valid* register of the other device. Another factor which could affect hit-less switching is the frequency of the local oscillator clock used by each ACS8510 device: these clocks are not mutually aligned and, whilst this has no impact on the frequency of the output clocks during locked mode, it could cause the output frequencies to diverge during Holdover mode if no action were taken to avoid it. In order to maintain alignment of the output frequencies of each ACS8510 device even during Holdover, the Master device's 6.48 MHz output is fed into the Slave device on its <I_11> pin, whilst the Multi-Frame Sync (2 kHz) output is fed to the Sync2k input of the Slave. In this way, the Slave locks to the master's output and remains locked whilst the Master moves between operating states. Only when the Master fails does the Slave use its own reference inputs - should the Master have been in the Holdover state, the Slave device will see the same lack of reference sources and also enter the Holdover state. This scheme also provides a convenient way to phase-align all T_{OUT0} output clocks in Master and Slave devices, and also to detect the failure of the Master device.

If a Master device fails, the Slave has to take over responsibility for the generation of the output clocks, including the 8 kHz and 2 kHz Frame and Multi-Frame clocks. The Slave device is also given responsibility for building the priority table and performing the reference switching operations. The Slave device, therefore, adopts a more active role when the Master has failed. The *cnfg_mode* register 34 (Hex) Bit 1 contains the "Master/Slave" control bit to determine the designation of the device.

To restore redundancy protection, the Master

has to be repaired and replaced. When this occurs, the new Master cannot immediately adopt its normal role because it must not cause phase hits on the output clocks. It has, therefore, to adopt a subordinate role to the active Slave device, at least until such time as it has acquired alignment to the 8 kHz and 2 kHz frame and Multi-Frame clocks and the priority table of the Slave device; then, when a switch-back (restoration) is ordered, the Master can take over responsibility. These activities, in Master or Slave operation, are detailed in Table 8.

Alignment of priority tables in Master and Slave ACS8510

Correct protection will only be achieved by connecting individual reference sources to the same input ports on each device and priority tables in each device must be aligned to each other.

The Master device must take account of the availability of each reference source seen by another device and a Slave device must adopt the same order of priority as the Master device (except that the slave's highest-priority input is <I_11>). Both devices monitor the reference sources and decide the availability of each source; if the failure of a reference source is seen by both devices, they will both update their priority tables - however, if the reference source failure is only seen by one device and not by both, the priority tables could get out of step: this could be catastrophic if it resulted in two devices choosing different reference sources since any slight differences in frequency variation over time (e.g. wander) would mis-align the phase of the 8 kHz Frame and 2 kHz Multi-Frame clocks produced by the individual devices, resulting in phase hits on switch-over. It is therefore important that the same priority table be built by each device, using the reference source availability seen by each device.

The monitoring of the reference sources performed by a Master ACS8510 results in a list of available sources being placed in a *sts_valid_sources* register. This information is used within the device as one of the masks used to build the device's priority table. The information is passed to the Slave device and used to configure the *cnfg_sts_remote_sources_valid* register so that it can use it as a mask in building its own priority tables. The information is passed between devices using the microprocessor port.

Alignment of the selection of reference sources for T_{OUT4} generation in the Master and Slave ACS8510

As stated previously, there is no need to align the phases of the T_{OUT4} outputs in Master and Slave devices. There is a need, however, to ensure that all devices select the same reference source. But, since there is no Holdover mode required for the generation of the T_{OUT4} clock, and every reference source is continuously monitored within each device, it is permissible to rely on external intelligence to command a switch-over to an alternative source should the selected one fail. The time delay involved in detecting the failure, indicating it to the outside and selecting a new source, will result only in the SSU/BITS entering its Hold-Over mode for a short time.

Alignment of the phases of the 8kHz and 2kHz clocks in both Master and Slave ACS8510

In addition to aligning the edges of the T_{OUT0} outputs of Master and Slave devices, it is necessary to align the edges of the Frame and Multi-Frame clocks. If this is not performed, frame alignment may be lost in distant equipment on switch-over to an alternative device, resulting in anomalous network operation of a very serious nature.

In accordance with the alignment mechanism used with the main T_{OUT0} clock (described in the

opening paragraphs of this section), whereby the 6.48 MHz output of the Master device is supplied to the Slave device, the alignment of both the 8 kHz and 2 kHz clocks is accomplished (they are already synchronous to the T_{OUTO} clocks) by feeding the 2 kHz clock of the Master device into the Slave device. The Multi-Frame Sync clock output of the Slave device is also fed to the Sync2K input of the Master device. Alignment of the Multi-Frame Sync input occurs only when *cnfg_mode* register, bit 3, address 34Hex External 2 kHz Sync Enable is set to 1.

JTAG

The JTAG connections on the ACS8510 allow a full boundary scan to be made. The JTAG implementation is fully compliant to IEEE 1149.1, with the following minor exceptions, and the user should refer to the standard for further information.

1. The output boundary scan cells do not capture data from the core, and so do not support EXTEST. However this does not affect board testing.

2. In common with some other manufacturers, pin TRST is internally pulled low to disable JTAG by default. The standard is to pull high. The polarity of TRST is as the standard: TRST high to enable JTAG boundary scan mode, TRST low for normal operation.

3. The device does not support the optional tri-state capability (HIGHZ). This will be supported on the next revision of the device.

The JTAG timing diagram is shown on page 53.

PORB

The Power On Reset (PORB) pin resets the device if forced Low for a power-on-reset to be initiated. The reset is asynchronous, the minimum Low pulse width is 5 ns. Reset is needed to initialize all of the register values to their defaults. Asserting Reset (POR) is required at power on, and may be re-asserted at any time to restore defaults. This is implemented most simplistically by an external capacitor to GND along with the internal pull-up resistor. The ACS8510 is held in a reset state for 250 ms after the PORB pin has been pulled High. In normal operation PORB should be held High.

Notes to Table 8

Note 1: Both ACS8510 must build a common priority table so that the Slave ACS8510 can select the same input reference source as the Master ACS8510 if the Master fails (when the Master is OK, the Slave locks to the Master's output).

Note 2: Slave ACS8510 uses common priority table, built before Master ACS8510 failed - priority table can be modified as status of the input reference sources changes

Note 3: Slave ACS8510 outputs must remain in phase with those of Master ACS8510

TCXO

V_{DD}

MASTER

MSTSLVB — T_{01} — 6.48 MHz

SEC1 → I_1 — T_{02}

SEC2 → I_2 — T_{03}

SEC3 → I_3 — T_{04}

I_11 — T_{07}

SEC14 → I_14 — T_{011}

SYNC2K — MF_rS_{ync}

TCXO

6.48 MHz

SLAVE

MSTSLVB — T_{01}

GND — SEC1 → I_1 — T_{02}

SEC2 → I_2 — T_{03}

SEC3 → I_3 — T_{04}

I_11 — T_{07}

SEC13 → I_14 — T_{011}

SYNC2K — MF_rS_{ync}

SYNC2K_EN=1

34Bit3
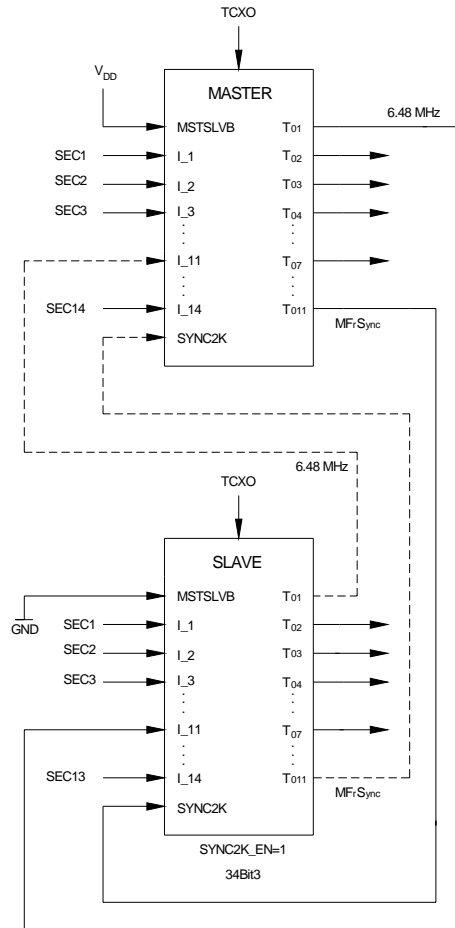
Ref_sources to Master ACS8510	Ref_sources to Slave ACS8510	Master ACS8510 status	Slave ACS8510 status	Master ACS8510	Slave ACS8510 output	Comments
All good	All good	Good	Good	Locked (ref_x)	Locked to master	Note 1
Some failed	Some others failed	Good	Good	Locked (ref_y)	Locked to master	Note 1
Good	Good	Good	Failed	Locked (ref_x)	Dead	
Good	Good	Failed	Good	Dead	Locked (ref_x)	Note 2
Good	Good	Failed	Failed	Dead	Dead	
Failed	Failed	Failed	Good	Holdover	Locked to master	Note 3
Failed	Failed	Good	Failed	Holdover	Dead	
Failed	Failed	Failed	Good	Dead	Holdover	Note 4
Failed	Failed	Failed	Failed	Dead	Dead	

Table 8: Master-Slave ACS8510 Relationship

Reference sources are flagged as 'valid' when active, 'in-band' and have no phase alarm set.

All sources are continuously checked for activity and frequency.

Only the main source is checked for phase. A phase lock alarm is only raised on a reference when that reference has lost phase whilst being used as the main reference. The micro-processor can reset the phase lock alarm.

A source is considered to have phase locked when it has been continuously in phase lock for between 1 and 2 seconds

Figure 8: Automatic Mode Control State Diagram.

Electrical Specification

Important Note: The "Absolute Maximum Ratings" are stress ratings only, and functional operation of the device at conditions other than those indicated in the "Operating Conditions" sections of this specification are not implied. Exposure to the absolute maximum ratings for an extended period may reduce the reliability or useful lifetime of the product.

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	MIN	MAX	UNITS
Supply Voltage V_{DD}, V_D+, V_A1+,V_A2+	V_{DD}	-0.5	3.6	V
Input Voltage (non-supply pins)	Vin	-	5.5	V
Output Voltage (non-supply pins)	Vout	-	5.5	V
Ambient Operating Temperature Range	T_A	-40	85	°C
Storage Temperature	T_{stor}	-50	150	°C

OPERATING CONDITIONS

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
Power Supply (dc voltage) VDD, VD+,VA1+, VA2+, VAMI+, VDD_DIFF	VDD	3.0	3.3	3.6	V
Power Supply (dc voltage) VDD5	VDD5	3.0	3.3/5.0	5.5	V
Ambient temperature Range	T_A	-40	-	85	°C
Supply current (Typical - one 19 MHz output)	IDD	-	110	200	mA
Total power dissipation	P_{TOT}	-	360	720	mW

DC CHARACTERISTICS: TTL Input pad.

Across operating conditions, unless otherwise stated

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
V_{in} High	V_{ih}	2.0	-	-	V
V_{in} Low	V_{il}	-	-	0.8	V
Input current	I_{in}	-	-	10	µA

DC CHARACTERISTICS: TTL Input pad with internal pull-up.

Across operating conditions, unless otherwise stated

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
V_{in} High	V_{ih}	2.0	-	-	V
V_{in} Low	V_{il}	-	-	0.8	V
Pull-up resistor	PU	30	-	80	kW
Input current	I_{in}	-	-	120	µA

DC CHARACTERISTICS: TTL Input pad with internal pull-down.

Across operating conditions, unless otherwise stated

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
V_{in} High	V_{ih}	2.0	-	-	V
V_{in} Low	V_{il}	-	-	0.8	V
Pull-udown resistor	PD	30	-	80	kW
Input current	I_{in}	-	-	120	µA

DC CHARACTERISTICS: TTL Output pad.

Across operating conditions, unless otherwise stated

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
Vout Low Iol = 4mA	Vol	0	-	0.4	V
Vout High Ioh = 4mA	Voh	2.4	-		V
Drive current	ID	-	-	4	mA

DC CHARACTERISTICS: PECL Input/Output pad.

Across operating conditions, unless otherwise stated

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
PECL Input Low voltage Differential inputs (Note 1)	V_{ILPECL}	VDD-2.5	-	VDD-0.5	V
PECL Input High voltage Differential inputs (Note 1)	V_{IHPECL}	VDD-2.4	-	VDD-0.4	V
Input Differential voltage	V_{IDPECL}	0.1	-	1.4	V
PECL Input Low voltage Single ended input (Note 2)	V_{ILPECL_S}	VDD-2.4	-	VDD-1.5	V
PECL Input High voltage Single ended input (Note 2)	V_{IHPECL_S}	VDD-1.3	-	VDD-0.5	V
Input High current Input differential voltage V_{ID} = 1.4v	I_{IHPECL}	-10	-	+10	µA
Input Low current Input differential voltage V_{ID} = 1.4v	I_{ILPECL}	-10	-	+10	µA
PECL Output Low voltage (Note 3)	V_{OLPECL}	VDD-2.10	-	VDD-1.62	V
PECL Output High voltage (Note 3)	V_{OHPECL}	VDD-1.25	-	VDD-0.88	V
PECL Output Differential voltage (Note 1)	V_{ODPECL}	580	-	900	mV

Notes:

Unused differential input ports should be left floating and set in LVDS mode, or the positive and negative inputs tied to VDD and GND respectively.

Note 1. Assuming a differential input voltage of at least 100 mV.

Note 2. Unused differential input terminated to VDD-1.4v.

Note 3. With 50Ω load on each pin to VDD-2v. i.e. 82Ω to GND and 130Ω to VDD.
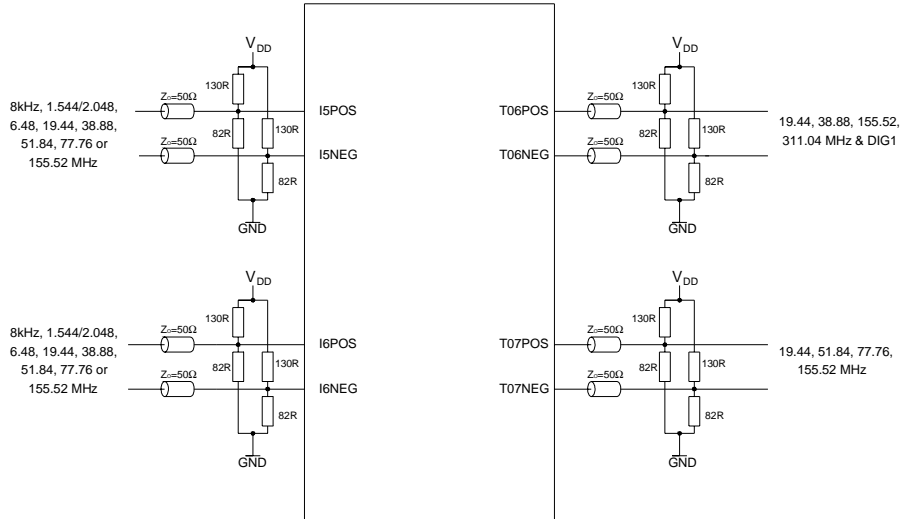
Recommended line termination for PECL Input/Output ports for VDD = 3.3V

DC CHARACTERISTICS: LVDS Input/Output pad.

Across operating conditions, unless otherwise stated

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
LVDS Input voltage range Differential input voltage = 100 mV	V_{VRLVDS}	0	-	2.40	V
LVDS Differential input threshold	V_{DITH}	-100	-	+100	mV
LVDS Input Differential voltage	V_{IDLVDS}	0.1	-	1.4	V
LVDS Input termination resistance Must be placed externally across the LVDS+/- input pins of ACS8510. Resistor should be 100W with 5% tolerance	R_{TERM}	95	100	105	W
LVDS Output high voltage (Note 1)	V_{OHLVDS}	-	-	1.585	V
LVDS Output low voltage (Note 1)	V_{OLLVDS}	0.885	-	-	V
LVDS Differential output voltage (Note 1)	V_{ODLVDS}	250	-	450	mV
LVDS Charge in magnitude of differential output voltage for complimentary states (Note 1)	$V_{DOSLVDS}$	-	-	25	mV
LVDS output offset voltage Temperature = 25°C (Note 1)	V_{OSLVDS}	1.125	-	1.275	V

Note 1. With 100Ω load between the differential outputs.
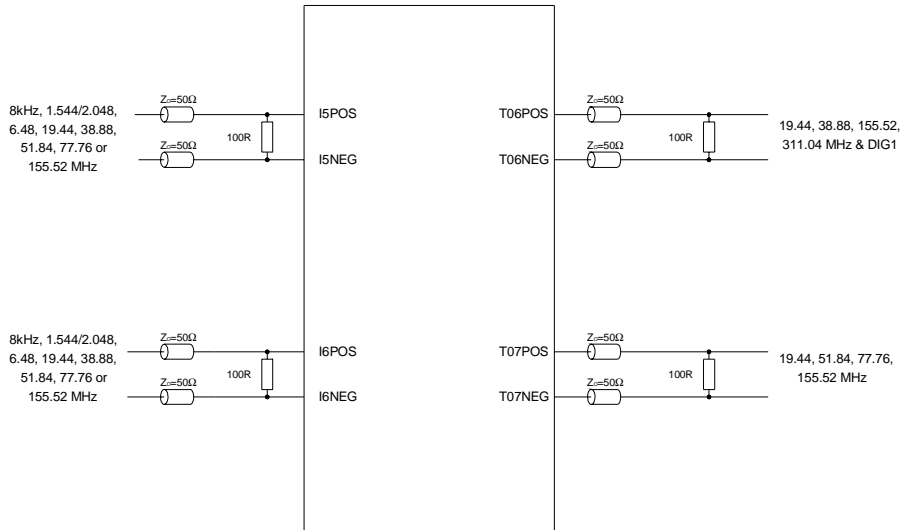
Recommended line termination for LVDS Input/Output ports

DC CHARACTERISTICS: AMI Input/Output pad.

Across operating conditions, unless otherwise stated

The Alternate Mark Inversion (AMI) signal is DC balanced and consists of positive and negative pulses with a peak to peak voltage of 2.0 +/- 0.2V.

The electrical specifications are taken from option a) of Table 2/G.703 - Digital 64kbit/s centralized clock interface, from ITU G.703.

PARAMETER	TIMING
Pulse shape	Nominally rectangular, with rise and fall times < 1µs
Nominal test load impedence	110 Ohms
Peak voltage of a "mark" (pulse)	1.0 +/- 0.1V
Peak value of a "space"	0.0 +/- 0.1V
Nominal pulse width	7.8µs

The electrical characteristics of 64kbits/s interface are as follows;

Nominal bit rate: 64kbit/s. The tolerance is determined by the network clock stability.

There should be a symmetrical pair carrying the composite timing signal (64kHz and 8kHz). The use of transformers is recommended.

Over-voltage protection requirement; refer to Recommendation K.41.

Code conversion rules;

The data signals are coded in AMI code with 100% duty cycle. The composite clock timing signals convey the 64kHz bit-timing information using AMI coding with a 50% to 70% duty ratio and the 8kHz octet phase information by introducing violations in the code rule. The structure of the signals and voltage levels are shown in Figure 9 and Figure 10.
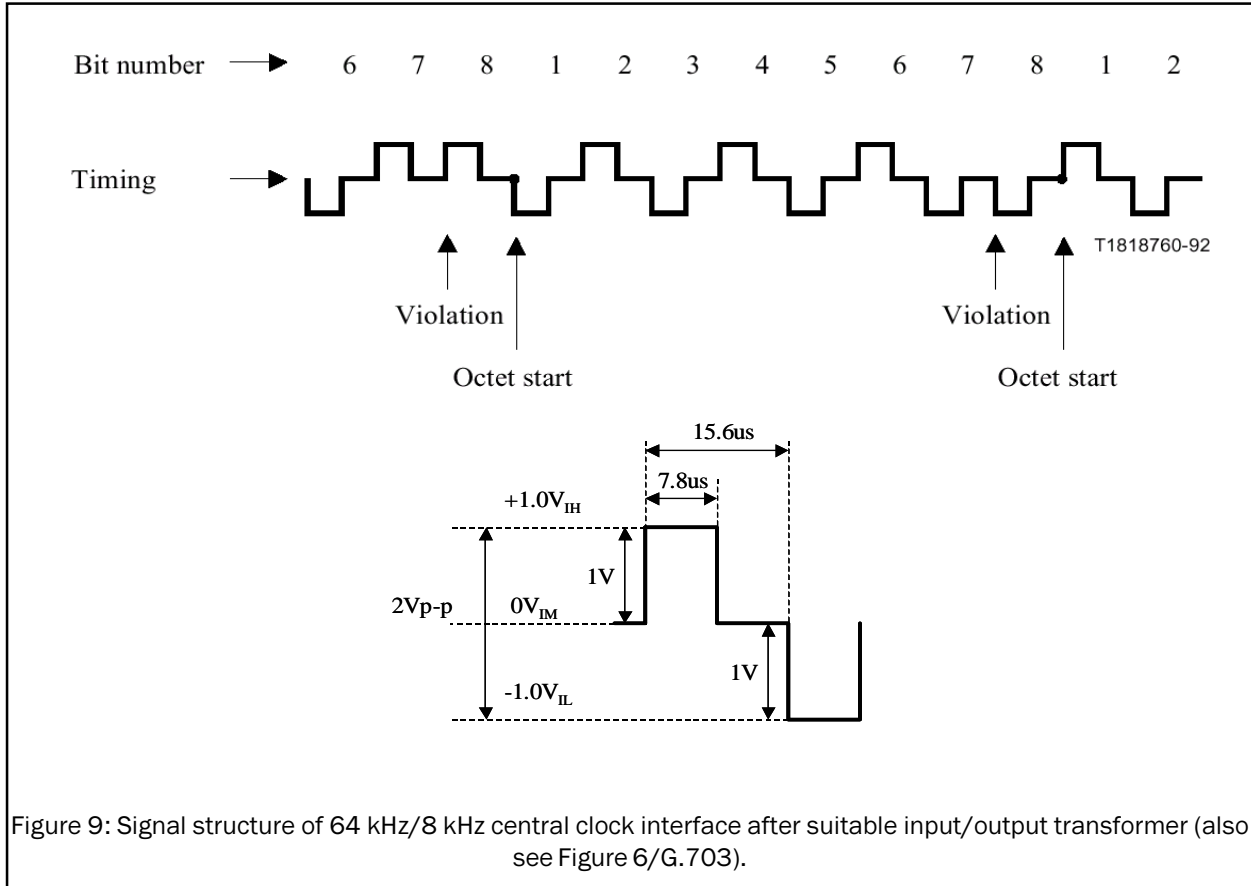
Figure 9: Signal structure of 64 kHz/8 kHz central clock interface after suitable input/output transformer (also see Figure 6/G.703).
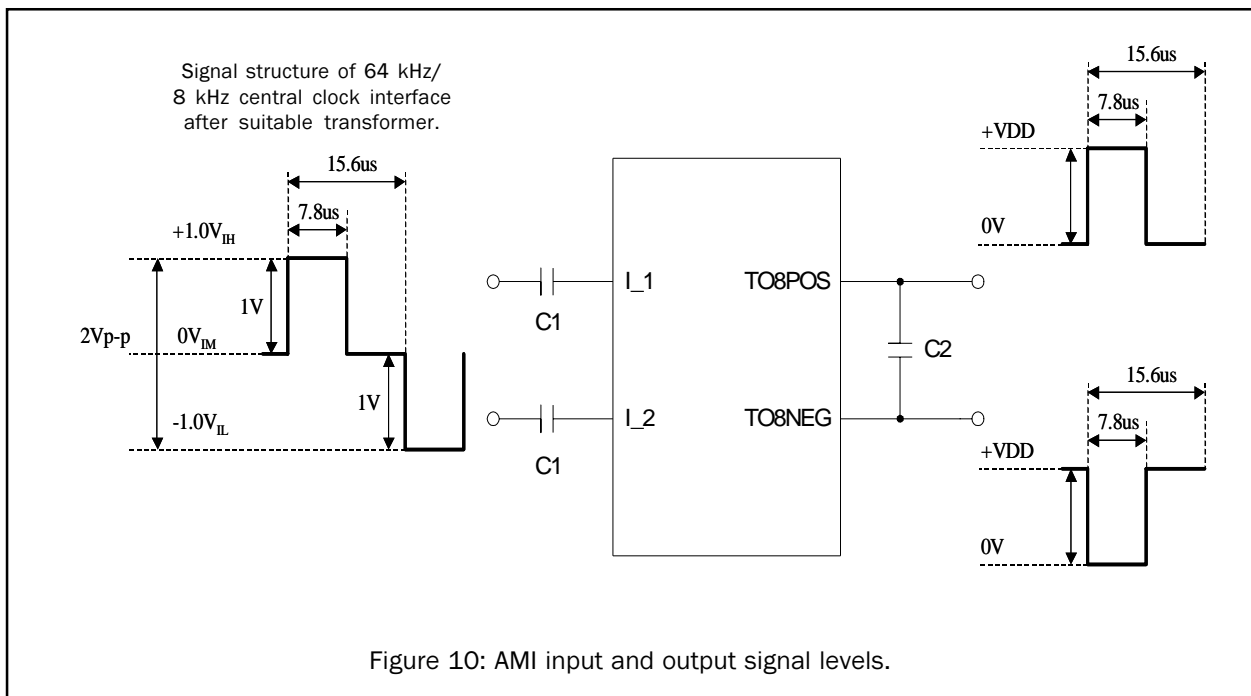
Figure 10: AMI input and output signal levels.

Recommended line termination for AMI Input/Output ports
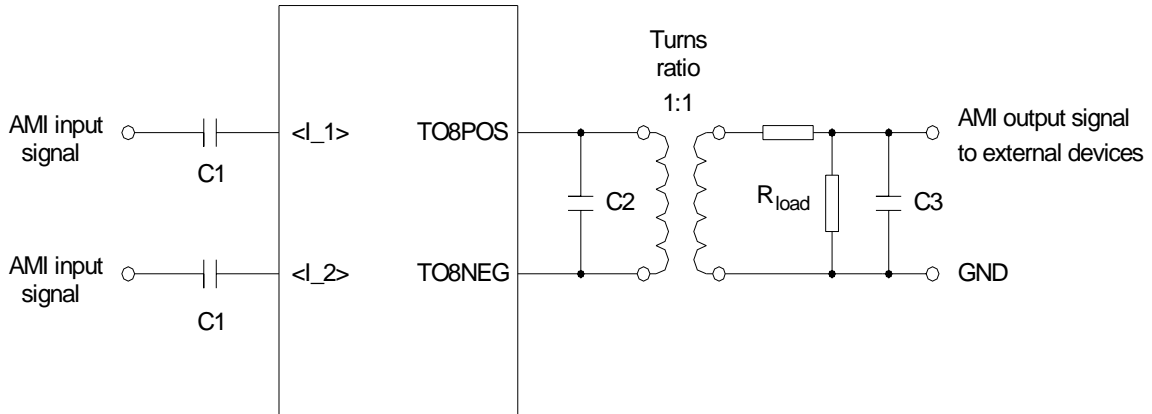
NOTE: For 1:1 turn ratio, a 3:1 potential divider R_{load} is required to give AMI output with 1 V pp for positive and negative pulses.

The AMI inputs <I_1> and <I_2> should be connected to the external AMI clock source by 470 nF coupling capacitor C1.

The AMI differential output O8POS/O8NEG should be coupled to a line transformer with a turns ration of 3:1. Components C2 = 470 pF and C3 = 2 nF. If a transformer with a turns ratio of 1:1 is used, a 3:1 ratio potential divider R_{load} must be used to achieve the required 1 V pp voltage level for the positive and negative pulses.

SEMTECH

DC CHARACTERISTICS: Output Jitter Generation

Across operating conditions, unless otherwise stated

Output jitter generation measured over 60 seconds interval, UI pp max measured using Vectron 6664 12.8MHz TCXO on ICT Flexacom + 10MHz reference from Wavetek 905.

Test definition	Filter used	UI spec	UI measurement on ACS8510 Rev 2
G813 for 155.52 MHz option 1	500 Hz to 1.3 MHz	$UI_{pp} = 0.5$	0.058 (Note 2)
G813 for 155.52 MHz option 1	65 kHz to 1.3 MHz	$UI_{pp} = 0.1$	0.048 (Note 3) 0.048 (Note 2)
G813 for 155.52 MHz option 2	12 kHz to 1.3 MHz	$UI_{pp} = 0.1$	0.053 (Note 4) 0.053 (Note 5)
			0.058 (Note 6) 0.053 (Note 7)
			0.053 (Note 2) 0.058 (Note 3)
			0.057 (Note 8) 0.055 (Note 9)
			0.057 (Note 10) 0.057 (Note 11)
			0.057 (Note 12) 0.053 (Note 13)
G813 & G812 for 2.048 MHz option 1	20 Hz to 100 kHz	$UI_{pp} = 0.05$	0.046 (Note 14)

Test definition	Filter used	UI spec	UI measurement on ACS8510 Rev 2
G812 for 1.544 MHz	10 Hz to 40 kHz	$UI_{pp} = 0.05$	0.036 (Note 14)
G812 for 155.52 MHz electrical	500 Hz to 1.3 MHz	$UI_{pp} = 0.5$	0.058 (Note 15)
G812 for 2.048 MHz electrical	65 kHz to 1.3 MHz	$UI_{pp} = 0.075$	0.048 (Note 15)

Test definition	Filter used	UI spec	UI measurement on ACS8510 Rev 2
ETS-300-462-3 for 2.048 MHz SEC	20 Hz to 100 kHz	UI_{pp} = 0.5	0.046 (Note 14)
ETS-300-462-3 for 2.048 MHz SEC (Filter spec 49 Hz to 100 kHz)	20 Hz to 100 kHz	UI_{pp} = 0.2	0.046 (Note 14)
ETS-300-462-3 for 2.048 MHz SSU	20 Hz to 100 kHz	UI_{pp} = 0.05	0.046 (Note 14)
ETS-300-462-3 for 155.52 MHz	500 Hz to 1.3 MHz	UI_{pp} = 0.5	0.058 (Note 15)
ETS-300-462-3 for 155.52 MHz	65 kHz to 1.3 MHz	UI_{pp} = 0.1	0.048 (Note 15)

Test definition	Filter used	UI spec	UI measurement on ACS8510 Rev 2
GR-253-CORE net i/f, 51.84 MHz	100 Hz to 400 kHz	UI_{pp} = 1.5	0.022 (Note 15)
GR-253-CORE net i/f, 51.84 MHz (Filter spec 20 kHz to 400 kHz)	18 kHz to 400 kHz	UI_{pp} = 0.15	0.019 (Note 15)
GR-253-CORE net i/f, 155.52 MHz	500 Hz to 1.3 MHz	UI_{pp} = 1.5	0.058 (Note 15)
GR-253-CORE net i/f, 155.52 MHz	65 kHz to 1.3 MHz	UI_{pp} = 0.15	0.048 (Note 15)
GR-253-CORE cat II elect i/f, 155.52 MHz	12 kHz to 400 kHz	UI_{pp} = 0.1	0.057 (Note 15)
		UI_{rms} = 0.01	0.006 (Note 15)
GR-253-CORE cat II elect i/f, 51.84 MHz	12 kHz to 1.3 MHz	UI_{pp} = 0.1	0.017 (Note 15)
		UI_{rms} = 0.01	0.003 (Note 15)
GR-253-CORE DS1 i/f, 1.544 MHz	10 Hz to 40 kHz	UI_{pp} = 0.1	0.036 (Note 14)
		UI_{rms} = 0.01	0.0055 (Note 14)

SEMTECH

Test definition	Filter used	UI spec	UI measurement on ACS8510 Rev 2
AT&T 62411 for 1.544 MHz (Filter spec 10 Hz to 8 kHz)	10 Hz to 40 kHz	$UI_{rms} = 0.02$	0.0055 (Note 14)
AT&T 62411 for 1.544 MHz	10 Hz to 40 kHz	$UI_{rms} = 0.025$	0.0055 (Note 14)
AT&T 62411 for 1.544 MHz	10 Hz to 40 kHz	$UI_{rms} = 0.025$	0.0055 (Note 14)
AT&T 62411 for 1.544 MHz	Broadband	$UI_{rms} = 0.05$	0.0055 (Note 14)

Test definition	Filter used	UI spec	UI measurement on ACS8510 Rev 2
G-742 for 2.048 MHz	DC to 100 kHz	$UI_{pp} = 0.25$	0.047 (Note 14)
G-742 for 2.048 MHz (Filter spec 18 kHz to 100 kHz)	20 Hz to 100 kHz	$UI_{pp} = 0.05$	0.046 (Note 14)
G-742 for 2.048 MHz	20 Hz to 100 kHz	$UI_{pp} = 0.05$	0.046 (Note 14)

Test definition	Filter used	UI spec	UI measurement on ACS8510 Rev 2
TR-NWT-000499 & G824 for 1.544 MHz	10 Hz to 40 kHz	$UI_{pp} = 5.0$	0.036 (Note 14)
TR-NWT-000499 & G824 for 1.544 MHz (Filter spec 8 kHz to 40 kHz)	10 Hz to 40 kHz	$UI_{pp} = 0.1$	0.036 (Note 14)

Test definition	Filter used	UI spec	UI measurement on ACS8510 Rev 2
GR-1244-CORE for 1.544 MHz	>10 Hz	$UI_{pp} = 0.05$	0.036 (Note 14)

Notes for the output jitter generation tables

Note 1.	Filter used is that defined by test definition unless otherwise stated
Note 2.	5 Hz bandwidth, 19.44 MHz direct lock
Note 3.	5 Hz bandwidth, 8 kHz lock
Note 4.	20 Hz bandwidth, 19.44 MHz direct lock
Note 5.	20 Hz bandwidth, 8 kHz lock
Note 6.	10 Hz bandwidth, 19.44 MHz direct lock
Note 7.	10 Hz bandwidth, 8 kHz lock
Note 8.	2.5 Hz bandwidth, 19.44 MHz direct lock
Note 9.	2.5 Hz bandwidth, 8 kHz lock
Note 10.	1.2 Hz bandwidth, 19.44 MHz direct lock
Note 11.	1.2 Hz bandwidth, 8 kHz lock
Note 12.	0.6 Hz bandwidth, 19.44 MHz direct lock
Note 13.	0.6 Hz bandwidth, 8 kHz lock
Note 14.	5 Hz bandwidth, 8 kHz lock, 2.048 MHz input
Note 15.	5 Hz bandwidth, 8 kHz lock, 19.44 MHz input

JTAG Timing
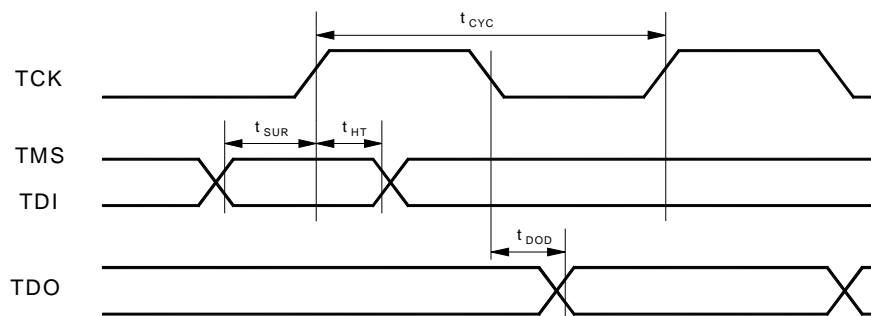
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
Cycle time	t_{CYC}	50	-	-	ns
TMS/TDI to TCK rising edge time	t_{SUR}	3	-	-	ns
TCK rising to TMS/TDI hold time	t_{HT}	23	-	-	ns
TCK falling to TDO valid	t_{DOD}	-	-	5	ns

Microprocessor interface timing

MOTOROLA Mode

In MOTOROLA mode, the device is configured to interface with a microprocessor using a 680x0 type bus. The following figures show the timing diagrams of write and read accesses for this mode.
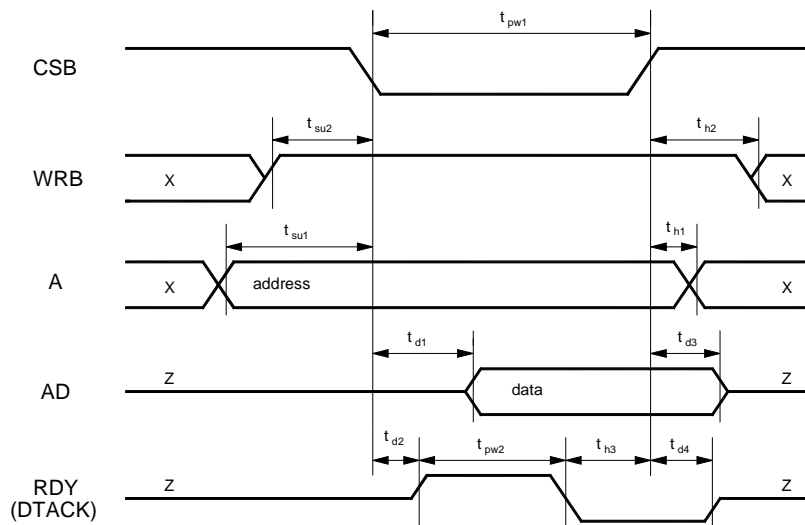
Symbol	Parameter	MIN	TYP	MAX
t_{su1}	Setup A valid to CSB$_{falling\ edge}$	0 ns	-	-
t_{su2}	Setup WRB valid to CSB$_{falling\ edge}$	0 ns	-	-
t_{d1}	Delay CSB$_{falling\ edge}$ to AD valid	-	-	177 ns
t_{d2}	Delay CSB$_{falling\ edge}$ to DTACK$_{rising\ edge}$	-	-	13 ns
t_{d3}	Delay CSB$_{rising\ edge}$ to AD high-Z	-	-	0 ns
t_{d4}	Delay CSB$_{rising\ edge}$ to RDY high-Z	-	-	7 ns
t_{pw1}	CSB low time	485 ns[1]	-	-
t_{pw2}	DTACK high time	310 ns	-	472 ns
t_{h1}	Hold A valid after CSB$_{rising\ edge}$	3 ns	-	-
t_{h2}	Hold WRB high after CSB$_{rising\ edge}$	0 ns	-	-
t_{h3}	Hold CSB low after DTACK$_{falling\ edge}$	0 ns	-	-
t_{p}	Time between consecutive accesses (CSB$_{rising\ edge}$ to CSB$_{falling\ edge}$)	320 ns	-	-

Read access timing in MOTOROLA Mode.

Note 1: Timing with RDY. If RDY not used, t_{pw1} becomes 178 ns.
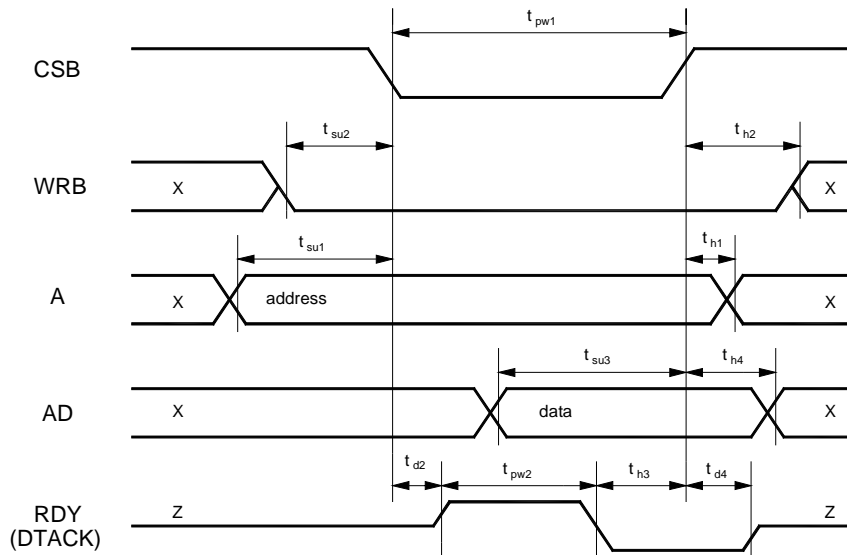
Symbol	Parameter	MIN	TYP	MAX
t_{su1}	Setup A valid to CSB$_{falling\ edge}$	0 ns	-	-
t_{su2}	Setup WRB valid to CSB$_{falling\ edge}$	0 ns	-	-
t_{su3}	Setup AD valid before CSB$_{rising\ edge}$	3 ns	-	-
t_{d2}	Delay CSB$_{falling\ edge}$ to DTACK$_{rising\ edge}$	-	-	13 ns
t_{d4}	Delay CSB$_{rising\ edge}$ to RDY high-Z	-	-	7 ns
t_{pw1}	CSB low time	485 ns[1]	-	-
t_{pw2}	DTACK high time	310 ns	-	472 ns
t_{h1}	Hold A valid after CSB$_{rising\ edge}$	3 ns	-	-
t_{h2}	Hold WRB low after CSB$_{rising\ edge}$	0 ns	-	-
t_{h3}	Hold CSB low after DTACK$_{falling\ edge}$	0 ns	-	-
t_{h4}	Hold AD valid after CSB$_{rising\ edge}$	4 ns		
t_{p}	Time between consecutive accesses (CSB$_{rising\ edge}$ to CSB$_{falling\ edge}$)	320 ns	-	-

Write access timing in MOTOROLA Mode.

Note 1: Timing with RDY. If RDY not used, t_{pw1} becomes 178 ns.

INTEL Mode

In INTEL mode, the device is configured to interface with a microprocessor using a 80x86 type bus. The following figures show the timing diagrams of write and read accesses for this mode.

Symbol	Parameter	MIN	TYP	MAX
t_{su1}	Setup A valid to CSB$_{falling\ edge}$	0 ns	-	-
t_{su2}	Setup CSB$_{falling\ edge}$ to RDB$_{falling\ edge}$	0 ns	-	-
t_{d1}	Delay RDB$_{falling\ edge}$ to AD valid	-	-	177 ns
t_{d2}	Delay CSB$_{falling\ edge}$ to RDY active	-	-	13 ns
t_{d3}	Delay RDB$_{rising\ edge}$ to RDY$_{falling\ edge}$	-	-	14 ns
t_{d4}	Delay RDB$_{rising\ edge}$ to AD high-Z	-	-	10 ns
t_{d5}	Delay CSB$_{rising\ edge}$ to RDY high-Z			9 ns
t_{pw1}	RDB low time	486 ns[1]	-	-
t_{pw2}	RDY low time	310 ns	-	472 ns
t_{h1}	Hold A valid after RDB$_{rising\ edge}$	0 ns	-	-
t_{h2}	Hold CSB low after RDB$_{rising\ edge}$	0 ns	-	-
t_{h3}	Hold RDB low after RDY$_{rising\ edge}$	0 ns	-	-
t_{p}	Time between consecutive accesses (RDB$_{rising\ edge}$ to RDB$_{falling\ edge}$, or RDB$_{rising\ edge}$ to WRB$_{falling\ edge}$)	320 ns	-	-

Read access timing in INTEL Mode.

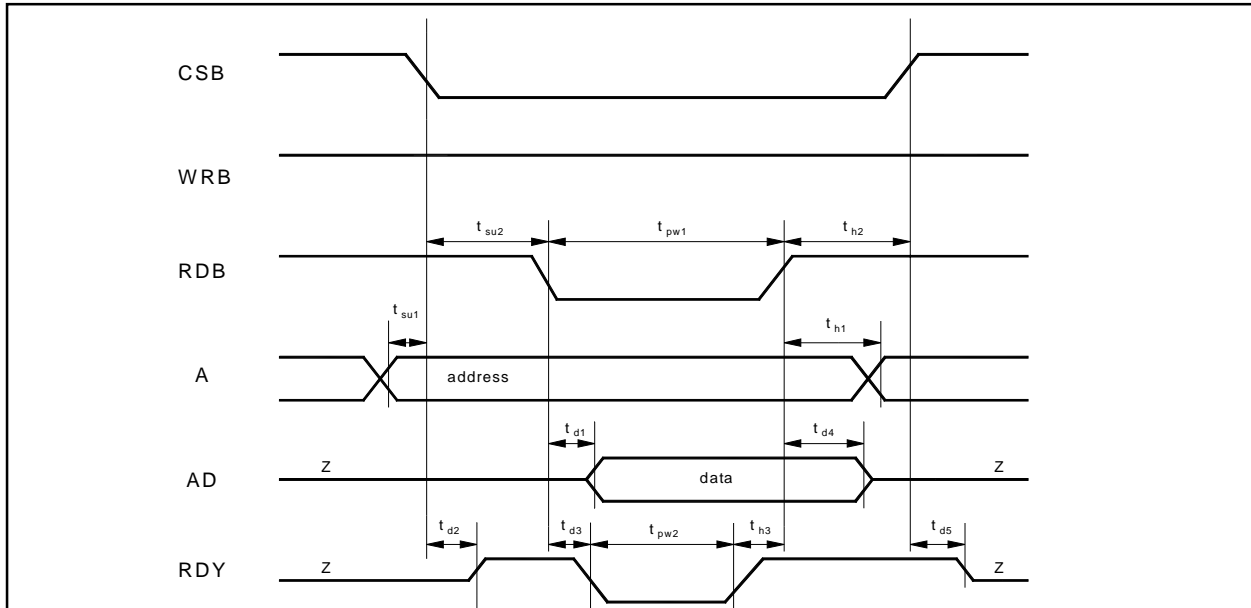Note 1: Timing with RDY. If RDY not used, t_{pw1} becomes 180 ns.

Symbol	Parameter	MIN	TYP	MAX
t_{su1}	Setup A valid to CSB$_{falling\ edge}$	0 ns	-	-
t_{su2}	Setup CSB$_{falling\ edge}$ to WRB$_{falling\ edge}$	0 ns	-	-
t_{su3}	Setup AD valid to WRB$_{rising\ edge}$	3 ns	-	-
t_{d2}	Delay CSB$_{falling\ edge}$ to RDY active	-	-	13 ns
t_{d3}	Delay WRB$_{falling\ edge}$ to RDY$_{falling\ edge}$	-	-	14 ns
t_{d5}	Delay CSB$_{rising\ edge}$ to RDY high-Z			9 ns
t_{pw1}	WRB low time	486 ns[1]	-	-
t_{pw2}	RDY low time	310 ns	-	472 ns
t_{h1}	Hold A valid after WRB$_{rising\ edge}$	170 ns[2]	-	-
t_{h2}	Hold CSB low after WRB$_{rising\ edge}$	0 ns	-	-
t_{h3}	Hold WRB low after RDY$_{rising\ edge}$	0 ns	-	-
t_{h4}	Hold AD valid after WRB$_{rising\ edge}$	4 ns		
t_{p}	Time between consecutive accesses (WRB$_{rising\ edge}$ to WRB$_{falling\ edge}$, or WRB$_{rising\ edge}$ to RDB$_{falling\ edge}$)	320 ns	-	-

Write access timing in INTEL Mode.

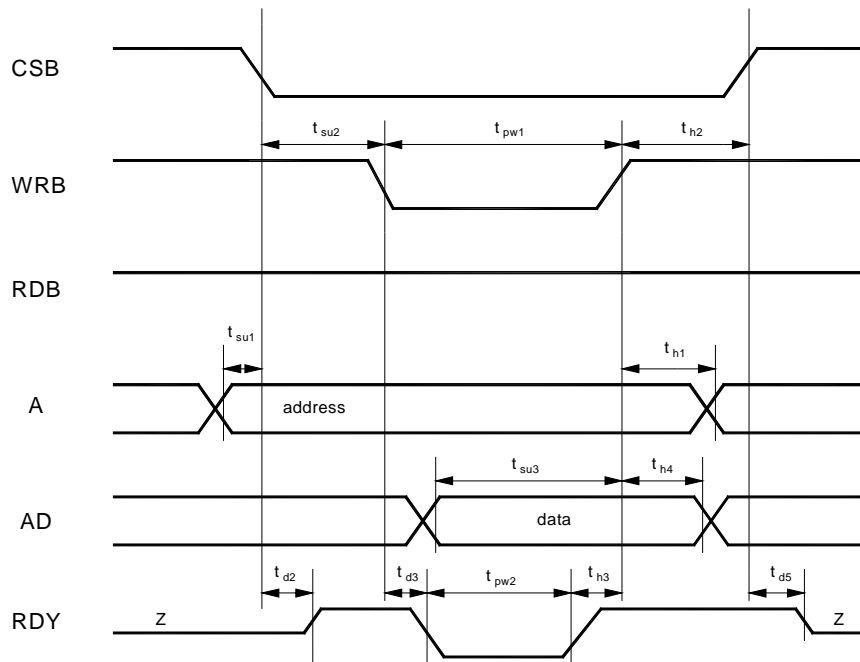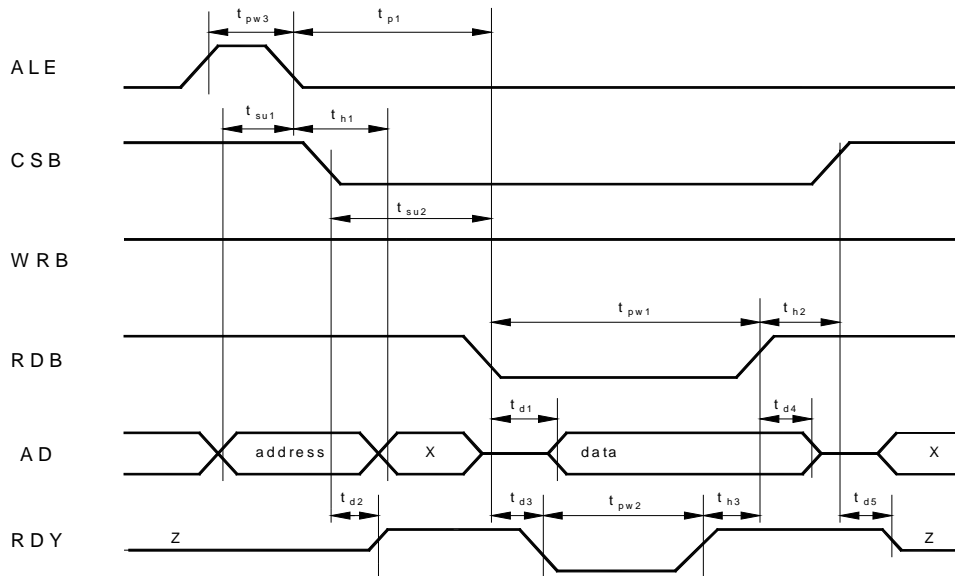Note 1: Timing with RDY. If RDY not used, t_{pw1} becomes 180 ns.
Note 2: Timing if t_{h2} is greater than 170 ns, otherwise 5 ns after CSB rising edge.

MULTIPLEXED Mode

In MULTIPLEXED mode, the device is configured to interface with a microprocessor using a multiplexed address/data bus. The following figures show the timing diagrams of write and read accesses for this mode.

Symbol	Parameter	MIN	TYP	MAX
t_{su1}	Setup AD address valid to ALE$_{falling\ edge}$	2 ns	-	-
t_{su2}	Setup CSB$_{falling\ edge}$ to RDB$_{falling\ edge}$	0 ns	-	-
t_{d1}	Delay RDB$_{falling\ edge}$ to AD data valid	-	-	177 ns
t_{d2}	Delay CSB$_{falling\ edge}$ to RDY active	-	-	13 ns
t_{d3}	Delay RDB$_{falling\ edge}$ to RDY$_{falling\ edge}$	-	-	15 ns
t_{d4}	Delay RDB$_{rising\ edge}$ to AD data high-Z	-	-	9 ns
t_{d5}	Delay CSB$_{rising\ edge}$ to RDY high-Z	-	-	10 ns
t_{pw1}	RDB low time	487 ns[(1)]	-	-
t_{pw2}	RDY low time	310 ns	-	472 ns
t_{pw3}	ALE high time	2 ns		
t_{h1}	Hold AD address valid after ALE$_{falling\ edge}$	3 ns	-	-
t_{h2}	Hold CSB low after RDB$_{rising\ edge}$	0 ns	-	-
t_{h3}	Hold RDB low after RDY$_{rising\ edge}$	0 ns	-	-
t_{p1}	Time between ALE$_{falling\ edge}$ and RDB$_{falling\ edge}$	0 ns	-	-
t_{p2}	Time between consecutive accesses (RDB$_{rising\ edge}$ to ALE$_{rising\ edge}$)	320 ns	-	-

Read access timing in MULTIPLEXED Mode.

Note 1: Timing with RDY. If RDY not used, t_{pw1} becomes 180 ns.
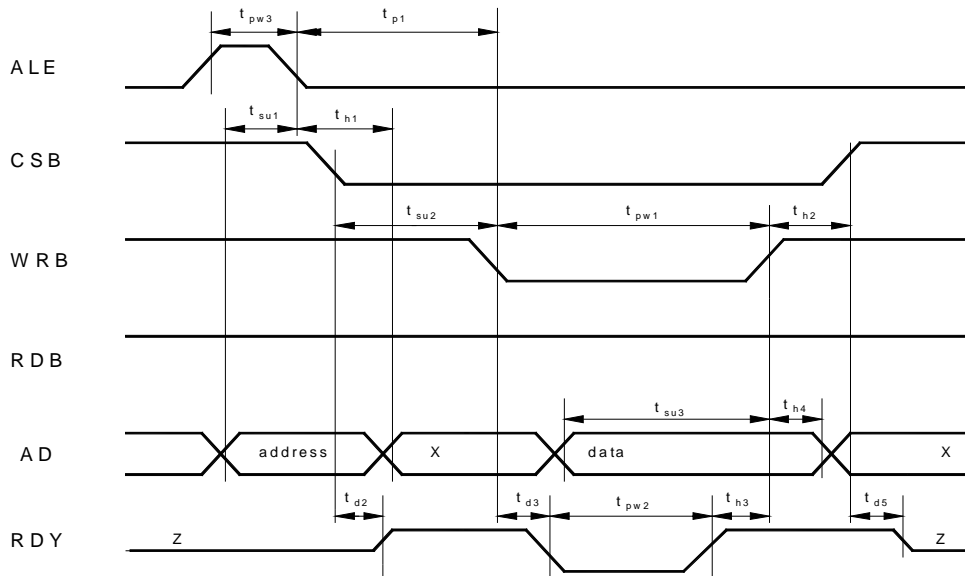
Symbol	Parameter	MIN	TYP	MAX
t_{su1}	Setup AD address valid to $ALE_{falling\ edge}$	2 ns	-	-
t_{su2}	Setup $CSB_{falling\ edge}$ to $WRB_{falling\ edge}$	0 ns	-	-
t_{su3}	Setup AD data valid to $WRB_{rising\ edge}$	3 ns	-	-
t_{d2}	Delay $CSB_{falling\ edge}$ to RDY active	-	-	13 ns
t_{d3}	Delay $WRB_{falling\ edge}$ to $RDY_{falling\ edge}$	-	-	15 ns
t_{d5}	Delay $CSB_{rising\ edge}$ to RDY high-Z			9 ns
t_{pw1}	WRB low time	487 ns[1]	-	-
t_{pw2}	RDY low time	310 ns	-	472 ns
t_{pw3}	ALE high time	2 ns	-	-
t_{h1}	Hold AD address valid after $ALE_{falling\ edge}$	3 ns	-	-
t_{h2}	Hold CSB low after $WRB_{rising\ edge}$	0 ns	-	-
t_{h3}	Hold WRB low after $RDY_{rising\ edge}$	0 ns	-	-
t_{h4}	AD data hold valid after $WRB_{rising\ edge}$	4 ns		
t_{p1}	Time between $ALE_{falling\ edge}$ and $WRB_{falling\ edge}$	0 ns	-	-
t_{p2}	Time between consecutive accesses ($WRB_{rising\ edge}$ to $ALE_{rising\ edge}$)	320 ns	-	-

Write access timing in MULTIPLEXED Mode.

Note 1: Timing with RDY. If RDY not used, t_{pw1} becomes 180 ns.

SERIAL Mode

In SERIAL mode, the device is configured to interface with a serial microprocessor bus. The following figures show the timing diagrams of write and read accesses for this mode.

During read access the output data SDO (AD(0)) is clocked out on the rising edge of SCLK (ALE) when the active edge selection control bit CLKE (A(1)) is 0 and on the falling edge when CLKE = 1.

Address, read/write control bit and write data are always clocked into the interface on the rising edge of SCLK.

Both input data SDI and clock SCLK are oversampled, filtered and synchronized to the 6MHz internal clock.

The serial interface clock (SCLK) is not required to run between accesses (i.e., when CSB = 1).
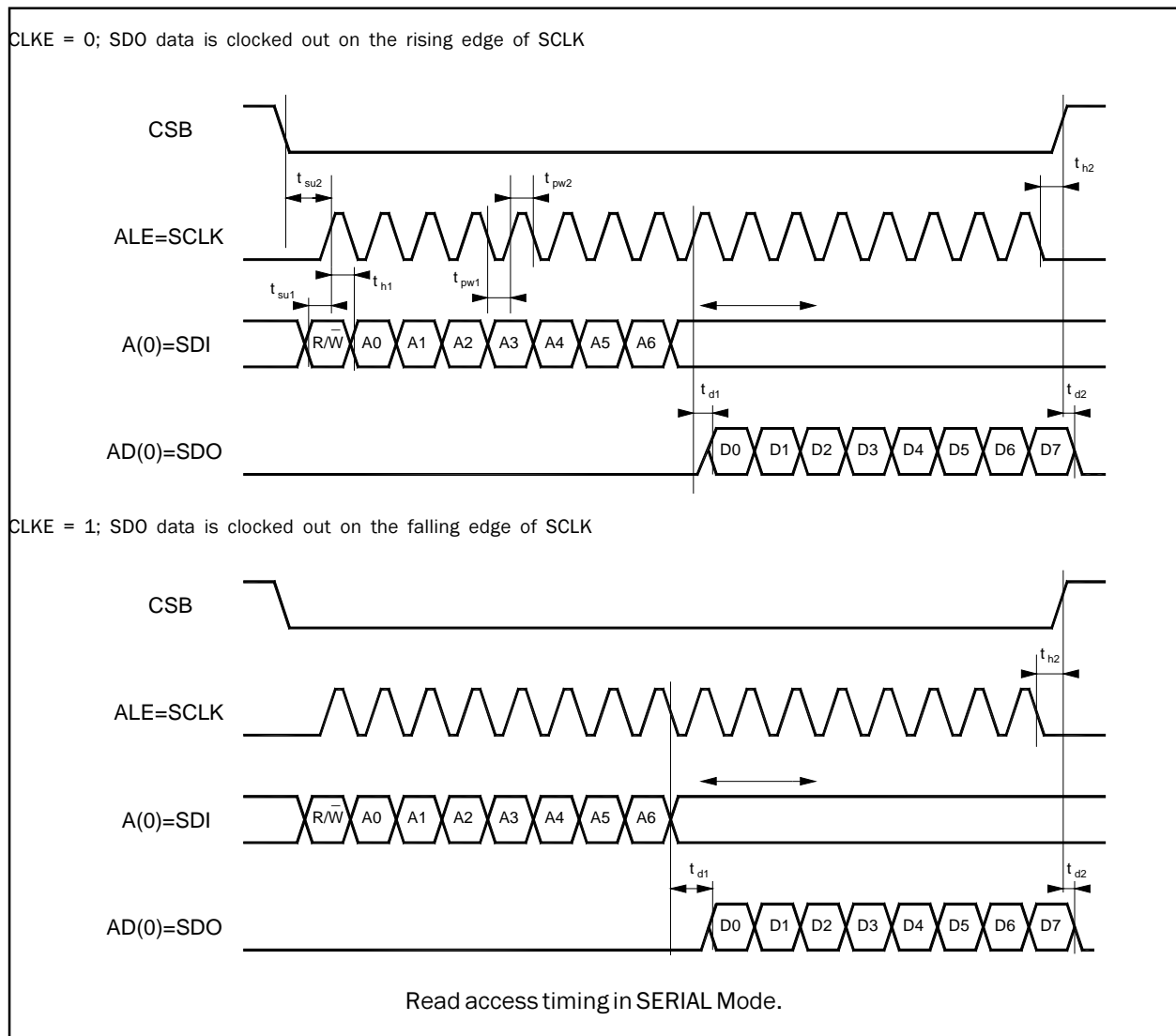
CLKE = 0; SDO data is clocked out on the rising edge of SCLK

CLKE = 1; SDO data is clocked out on the falling edge of SCLK

Read access timing in SERIAL Mode.

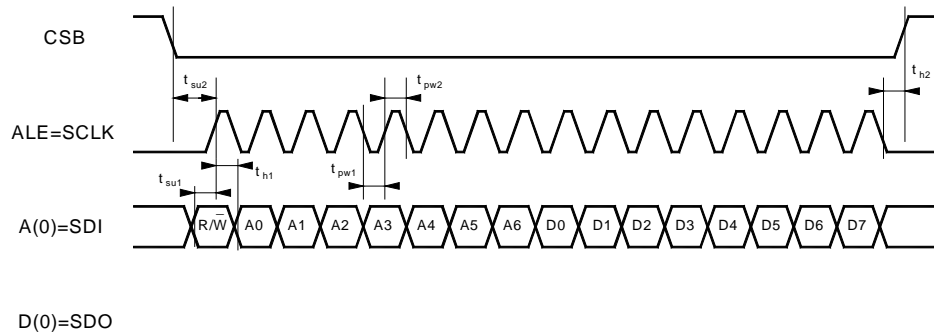| Symbol	Parameter	MIN	TYP	MAX
t_{su1}	Setup SDI valid to SCLK$_{rising\ edge}$	0 ns	-	-
t_{su2}	Setup CSB$_{falling\ edge}$ to SCLK$_{rising\ edge}$	160 ns	-	-
t_{d1}	Delay SCLK$_{rising\ edge}$ (SCLK$_{falling\ edge}$ for CLKE = 1)to SDO valid	-	-	17 ns
t_{d2}	Delay CSB$_{rising\ edge}$ to SDO high-Z	-	-	10 ns
t_{pw1}	SCLK low time	180 ns	-	-
t_{pw2}	SCLK high time	180 ns	-	-
t_{h1}	Hold SDI valid after SCLK$_{rising\ edge}$	170 ns	-	-
t_{h2}	Hold CSB low after SCLK$_{rising\ edge}$, for CLKE = 0 Hold CSB low after SCLK$_{falling\ edge}$, for CLKE = 1	5 ns	-	-
t_p	Time between consecutive accesses (CSB$_{rising\ edge}$ to CSB$_{falling\ edge}$)	160 ns	-	-

Read access timing in SERIAL Mode.

Symbol	Parameter	MIN	TYP	MAX
t_{su1}	Setup SDI valid to SCLK$_{rising\ edge}$	0 ns	-	-
t_{su2}	Setup CSB$_{falling\ edge}$ to SCLK$_{rising\ edge}$	160 ns	-	-
t_{pw1}	SCLK low time	180 ns	-	-
t_{pw2}	SCLK high time	180 ns	-	-
t_{h1}	Hold SDI valid after SCLK$_{rising\ edge}$	170 ns	-	-
t_{h2}	Hold CSB low after SCLK$_{rising\ edge}$	5 ns	-	-
t_p	Time between consecutive accesses (CSB$_{rising\ edge}$ to CSB$_{falling\ edge}$)	160 ns	-	-

Write access timing in SERIAL Mode.

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EPROM Mode

In EPROM mode, the ACS8510 takes control of the bus as Master, and reads the device set-up from an AMD AM27C64 type EPROM at lowest speed (250ns), after device start-up (system reset). The EPROM access state machine in the up interface sequences the accesses.

Further details can be found in the AMD AM27C64 data sheet.

Symbol	Parameter	MIN	TYP	MAX
t_{acc}	Delay CSB$_{falling\ edge}$ or A change to AD valid	-	-	920 ns

Read access timing in EPROM Mode.

Package information

Notes

1. The top package body may be smaller than the bottom package body by as much as 0.15 mm.

2. To be determined at seating plane.

3. Dimensions D1 and E1 do not include mold protrusion. Allowable protrusion is 0.25 mm per side.
   D1 and E1 are maximum plastic body size dimensions including mold mismatch.

4. Details of pin 1 identifier are optional but will be located within the zone indicated.

5. Exact shape of corners can vary.

6. A1 is defined as the distance from the seating plane to the lowest point of the package body.

7. These dimensions apply to the flat section of the lead between 0.10 mm and 0.25 mm from the lead tip.

8. Shows plating.

100 LQFP Package Dimensions in mm	D/E	D1/E1	A	A1	A2	e	AN1	AN2	AN3	AN4	R1	R2	L	L1	S	b	b1	c	c1
Min			1.40	0.05	1.35		11°	11°	0°	0°	0.08	0.08	0.45		0.20	0.17	0.17	0.09	0.09
Nom	16.00	14.00	1.50	0.10	1.40	0.50	12°	12°	-	3.5°	-	-	0.60	1.00 (ref)	-	0.22	0.20	-	-
Max			1.60	0.15	1.45		13°	13°	-	7°	-	0.20	0.75		-	0.27	0.23	0.20	0.16

Thermal conditions

The device is rated for full temperature range when this package is used with a 4 layer or more PCB. Copper coverage must exceed 50%. All pins must be soldered to the PCB. Maximum operating temperature must be reduced when the device is used with a PCB with less than these requirements.

Notes

Application information

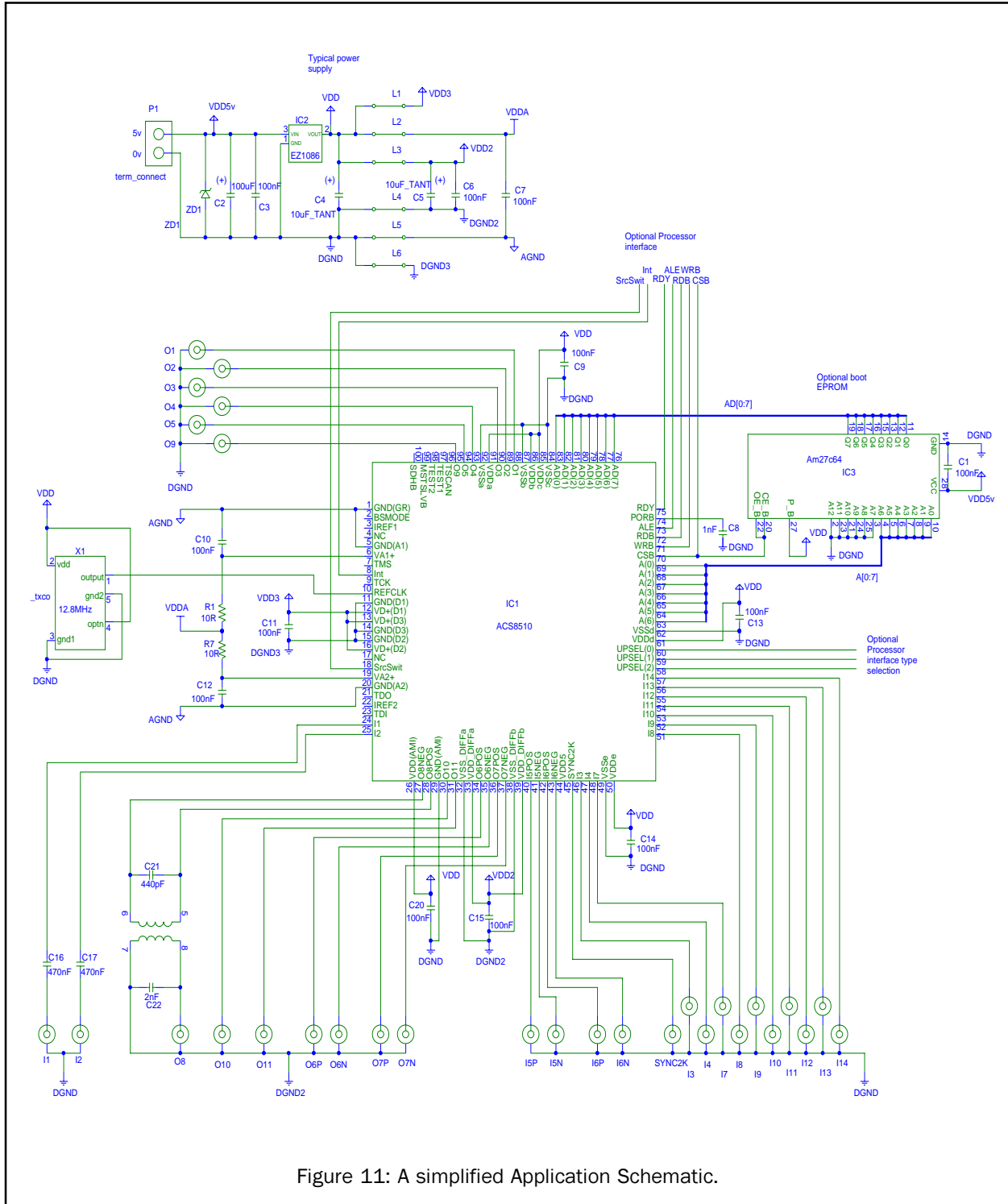A simplified Application Schematic for the ACS8510 is illustrated in Figure 11.

Figure 11: A simplified Application Schematic.

Revision History

Changes from revision 2.06 to 2.07. January 2001.

Item	Section	Page	Description
1	Table of contents	2	Inclusion of Revision History
2	Pin descriptions	5	Pins 34/35 and 36/37 corrected for LVDS/PECL defaults
3	Table 5	15	Ports T_{06} and T_{07} corrected for LVDS/PECL defaults
4	Register description	25	sts_interrupts register re-formatted and address error removed
5	Register description	26	sts_curr_inc_offset register corrected for errors
6	Register description	28	cnfg_sts_remote_sources_valid register re-formatted
7	Register description	28	cnfg_operating_mode register error corrected
8	Register description	31	cnfg_freq_limit register re-formatted and re-written
9	Leaky bucket timing box	36	Omission corrected in default setting equation
10	Holdover mode	39	Spelling error corrected
11	Revision History	68	Section added

Ordering information

PART NUMBER	DESCRIPTION
ACS8510	SONET/SDH Synchronisation, 100 pin LQFP

Disclaimers

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