# HFTA-04.0: Optical/Electrical Conversion in SDH/SONET Fiber Optic Systems

*This article explains the basic functions and design challenges of the optical to electrical and electrical to optical signal conversion in SDH/SONET fiber optic receivers and transmitters. A complete chip set solution to develop the electronic part of OC 12/STM 4 receivers and transmitters is presented.*

*The advent of cheaper and more powerful personal computers has not only expanded the user base; it is also creating a demand for greater transmission capacity among the telecom networks by adding an increasing volume of internet and videophone connections to the traditional phone and fax services. The following discussion of an OC 12/STM 4 receiver/transmitter chipset supports these developments and includes a description of the electronic components required for optic/electric (O/E) conversion in SDH/SONET fiber optic transmission systems.*

Competition among network providers enables the multimedia market to grow, and the introduction of new and improved products and services in the near future should strengthen the demand for increased transmission capacity. This need for more data throughput can be satisfied economically with fiber optic (FO) cables because the transmission capacity is potentially very high (versus that of copper wires). The physical nature of the fiber cable lets providers expand capacity by increasing the transmission bit rate or by introducing alternative transmission techniques, without the need for further upgrades or additional cable installations. These advantages have led many countries to build extensive fiber networks, and further expansion of these networks can be expected.

To transmit optical data via fiber cables, signals must be converted from electrical to optical at the transmit end, and then converted back to electrical at the receive end. These necessary conversions are handled by receiver/transmitter units that contain electronic devices along with the optical components.

## FO transceivers

The widely used Time Division Multiplex (TDM) transmission technique now enables bit rates up to 10Gbps and is well established in modern transport systems. Today's high-speed fiber optic transmission systems offer the following standard bit rates:

| SONET STANDARD | SDH STANDARD | BIT RATE |
|---|---|---|
| OC 1 | — | 51.84Mbps |
| OC 3 | STM 1 | 155.52Mbps |
| OC 12 | STM 4 | 622.08Mbps |
| OC 48 | STM 16 | 2.4883Gbps |
| OC 192 | STM 64 | 9.9533Gbps |

New techniques such as Wavelength Division Multiplexing (WDM) further increase the transmission capacity by sending numerous time-multiplexed data streams over one fiber, using a different wavelength for each data stream. Electronic components in a WDM receiver and transmitter (compared with those in a TDM system) differ according to the behavior of the optical sources and line amplifiers in the WDM transport system. The following section describes the performance required for receivers and transmitters in an optical TDM transmission system.

## Optical receivers

Optical receivers detect optical signals from the fiber and convert them to electrical signals, which must then be amplified before their data waveforms and clock can be recovered. A serial-to-parallel conversion of the data stream may be necessary, depending on the bit rate and the system-specific setup of the following CMOS functions. **Figure 1** shows how the receiver's output interface provides regenerated data in a serial or parallel bit stream, along with the recovered clock.

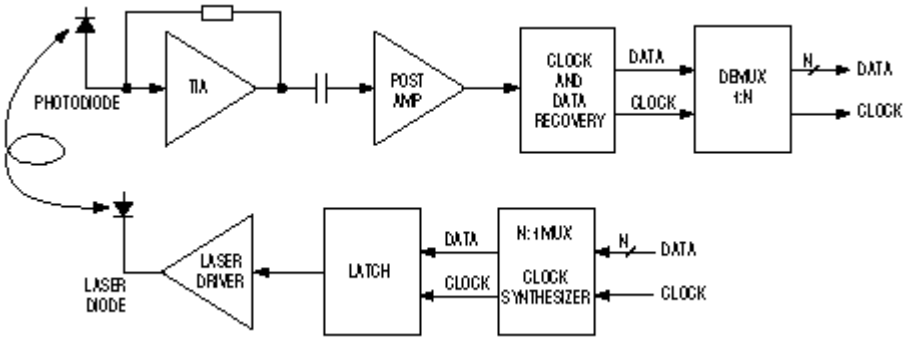


*Figure 1. A typical receiver/transmitter unit for SONET/SDH fiber-transmission systems.*

A PIN or APD (avalanche photodiode) photodetector converts the received light to a signal current. The PIN diode is relatively cheap and operates with the same supply voltage as the electronic components, but for a given optical power it generates fewer electrons than the APD. As a result, the APD provides a more sensitive receiver that can be placed farther away from the transmitter. This advantage is offset by the need for an APD bias circuit, which (depending on the APD type) must provide a reverse operating voltage in the 30V to 100V range. Additionally, the APD adds more noise, costs more, and requires cooling.

The photodetector delivers the extracted current to a transimpedance amplifier (TIA), which first converts the current to a voltage. This single-ended voltage is then amplified by the TIA and (usually) converted to a differential signal as required by state-of-the-art receivers. The TIA should provide both high overload tolerance and high input sensitivity (i.e., a large dynamic range).

To provide the high input sensitivity necessary to receive optical signals weakened by transmitter aging or long transmission distance (or both), the TIA noise must be reduced to a minimum. On the other hand, a high overload tolerance is required to avoid bit errors due to distortion in the presence of strong optical signals. Further, the TIA's maximum achievable gain depends on the operating frequency. To ensure stable operation and the required bandwidth, gain can be optimized only within a narrow range. This limitation may cause the output voltage resulting from low-power optical signals to be insufficient for further processing. To amplify small TIA voltages in the 1mV to 2mV range, the TIA function must be followed by a postamplifier, which in most cases is a limiting amplifier (LA).

As the name implies, a limiting amplifier delivers a certain output-voltage swing whose maximum is independent of the input signal strength. Also included is a loss-of-power indicator (LOP) that warns when the incoming signal falls below a user-defined threshold. As a system-dependent parameter, this threshold must be adjusted externally. A comparator with hysteresis ensures chatter-free operation for the LOP flag when the signal is close to the threshold level.

A key component that follows the limiting amplifier in a receiver unit is the clock and data recovery (CDR) circuit. The CDR performs timing and amplitude-level decisions on the incoming signal, which leads to a time- and amplitude-regenerated data stream. First to be recovered from the received signal is the clock. Several possibilities can support this clock-recovery function (external SAW filter, external reference clock, etc.), but only the fully integrated approach can save both cost and effort.

The challenge for an integrated clock-recovery circuit is to meet the jitter specification recommended by the International Telecommunication Union-Telecom Standards Sector (ITU-T). Jitter refers to the effect in which individual bit transitions ("0" to "1" and vice-versa) are not exactly in phase. The effect becomes visual in an "eye diagram," in which several pseudo-random bit-pattern sequences are superimposed. An eye diagram illustrates the quality of a data stream in terms of the eye opening, measured using the "eye mask" (**Figure 2**).

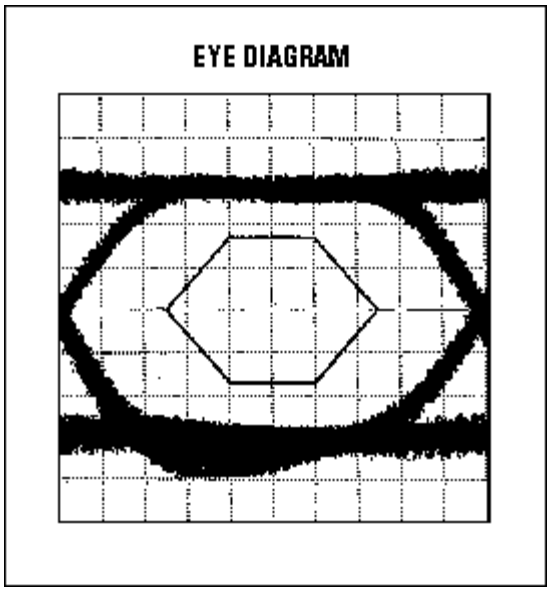


*Figure 2. An "eye diagram" illustrates the signal quality of a data stream.*

ITU-T recommendations specify limits on the tolerance, transfer, and generation of jitter. Signal quality at the LA output (as represented by the eye opening) is usually low, mostly as a consequence of nonideal components in the optical transmission system. Because the CDR must accept a certain amount of input data jitter to achieve normal error-free operation, all receiver units in line-termination and regenerator applications must comply with the ITU-T recommendations for jitter tolerance.

Jitter transfer refers to the portion of jitter allowed to transfer from input to output of the CDR, and jitter generation is that produced by the CDR itself. The ITU-T specs for these two parameters must be met for regenerators in a long-haul system, because at each stage the recovered clock enables transmission to the next regenerator, allowing jitter contributions to accumulate from regenerator to regenerator. Conversely, for line-termination receivers (which are in the majority of applications) the jitter transfer and jitter generation need not meet ITU-T recommendations. In those applications, the regenerated data is synchronized to the system clock.

Aside from jitter effects, noise and pulse distortion both reduce the phase margin in which received bits can be clocked for the purpose of sensing their logic level. The use of a phase-locked loop (PLL) is essential in synchronizing the clock with the data stream, to ensure alignment of the clock with the middle of a data word. To further optimize the bit error rate (BER) in the presence of asymmetrical rise and fall transitions of the received data signal, the system should include an option to adjust the phase relation between clock and data.

The CDR often includes a loss-of-lock (LOL) alarm, which monitors whether the PLL is locked to the received data stream. The CDR's serial stream of regenerated data and the recovered clock signal are usually fed to a deserializer, whose conversion ratio depends on the data's bit rate and the interface capability (speed) of the CMOS system components. The

deserializer must also provide a CMOS-compatible interface. To support bit alignment of the serial data stream to the different deserializer outputs, the deserializer should include bit-synchronization capability.

## Optical transmitter

The optical transmitter in a fiber optic system converts the electrical bit sequence delivered from the CMOS system components to an optical data stream. As shown in Figure 1, it contains a serializer with clock synthesizer (which depends on the system setup and transmission bit rate), a driver, and an optical source.

Two important wavelength ranges (windows 2 and 3) are in use for transmitting information over a fiber cable in telecommunication networks. Within an optical window, the signals benefit from a lower impact on quality (less dispersion) and less attenuation per unit of fiber length. The range between 1000nm and 1300nm, called the second optical window, is known for low dispersion-as low as 0dB. The range from 1500nm to 1800nm, known as the third optical window, offers the lowest attenuation per unit of fiber length (**Figure 3**).

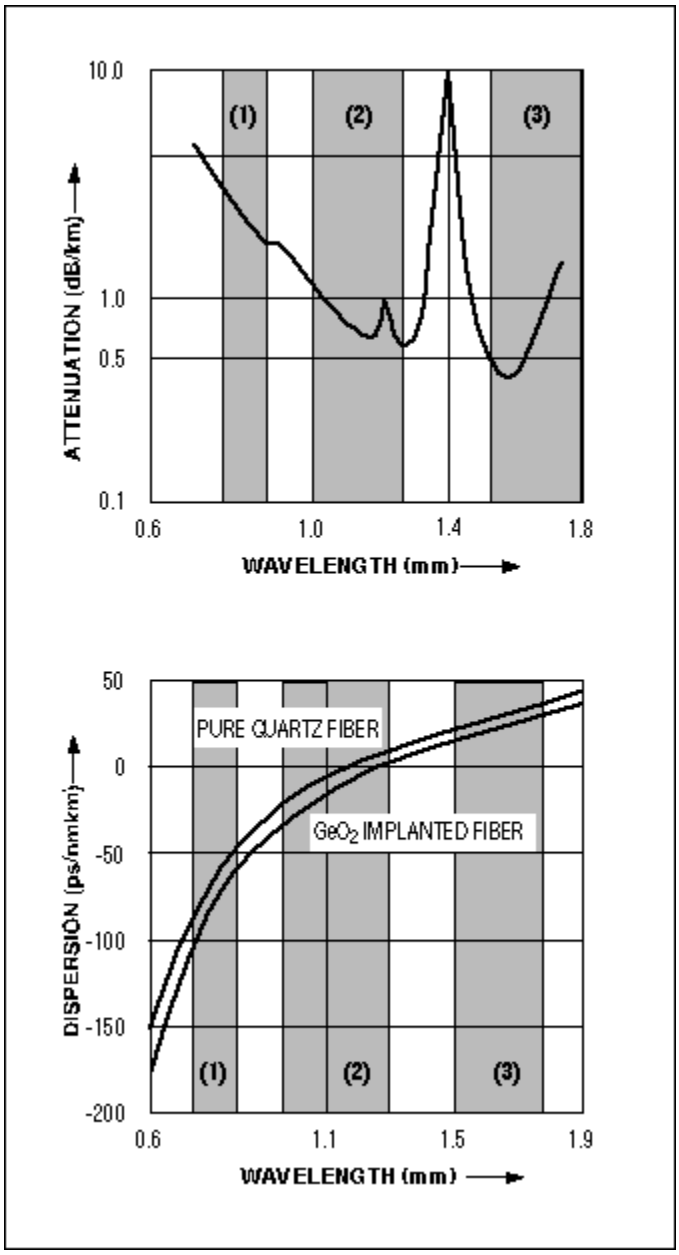


*Figure 3. Variations of attenuation and dispersion vs. wavelength for the first, second, and third optical windows.*

Several optical sources are available for today's optical transmission systems. Light-emitting diodes (LEDs), for example, are often used for low-cost, short-distance local area network (LAN) connections. Disadvantages, however, preclude use of the LED as a transmitter for telecommunications systems: its broad spectral bandwidth allows the coexistence of many optical modes, and it cannot operate at wavelengths of the second and third optical windows.

Unlike the LED, the optical-modulated laser transmitter (the electro-absorption and Mach-Zehnder types, for instance) is an optical source with high spectral purity that can operate in the

third optical window. It is preferred, therefore, for ultra-long-distance or WDM transmission systems in which high performance is mandatory and cost is not a major consideration. For optical links in the majority of telecommunication trunk lines, various types of direct-modulated semiconductor laser diode offer an optimum cost/performance ratio for short, intermediate, and long-haul transmissions. Devices are available for operation in both the second and third optical windows.

All semiconductor laser diodes used for direct modulation have in common the need for a DC-bias current to set the operating point and a modulation current for signal transmission. The values for DC-bias and modulation current depend on characteristics of the laser diode, which can differ from type to type and version to version. The drift of these characteristics with time and temperature should be evaluated carefully when designing a transmitter unit, especially with regard to the more cost-effective, uncooled types of semiconductor laser. The laser driver must therefore offer bias and modulation currents with sufficient range to support the development of optical transmitters with a wide choice of laser diodes.

To compensate for the drift of laser characteristics over time and temperature, the laser driver must maintain the initially adjusted DC operating point. The best way to realize this compensation is to introduce automatic power control (APC). To detect the actual laser power, a photodiode converts the laser light to a proportional current and feeds it to the laser driver, where the actual value is compared with a previous fixed value. Any difference causes the DC-bias current to increase or decrease as required to reach the initially defined laser power.

Often, the APC includes an alarm function that warns if the laser diode's optical power can no longer be sustained due to aging. Like the operating point, optical signal strength is affected by the drift of laser-diode characteristics over time and temperature. To maintain the optical "amplitude," it is necessary to compensate for a decreasing slope in these characteristics caused by time and temperature. The problem is solved either with additional external circuitry or with an integrated Automatic Modulation Control (AMC), which may employ the photodiode already present in the APC loop.

In addition to these fundamental functions, the system must be capable of stopping laser transmissions by disabling the driver without interrupting data reception at the input. By adding a flip-flop or latch (as part of the laser driver or the serializer), jitter performance can be improved by retiming this data stream before it reaches the laser driver's output stage.

Residing between the laser-diode driver and the lower-speed CMOS system components, the serializer converts parallel data to a serial stream for the laser driver. Like the receiver unit's deserializer, the serializer's conversion ratio depends on the transmission bit rate and the speed of the CMOS system interface. The retiming and serialization function requires a transmission clock, which must to be synthesized. This clock synthesizer can be integrated with the serializer, and usually incorporates a PLL. The challenge for the synthesizer is to ensure data transmission with the lowest possible jitter. As a result, the synthesizer plays a key role in the transmitter of an optical transmission system.

## Complete chipset for STM 4 Rx/Tx units

All components of an optical transmission system for telecommunications must comply with the relevant ITU-T recommendations. Provided this basic requirement is met, the next most

important criteria in designing an O/E unit are power dissipation, supply voltage, integration level, and margin of performance. The following section describes a complete chipset that allows designers to optimize the above criteria while developing competitive STM 4 receiver/transmitter units (**Figures 4** and **5**).

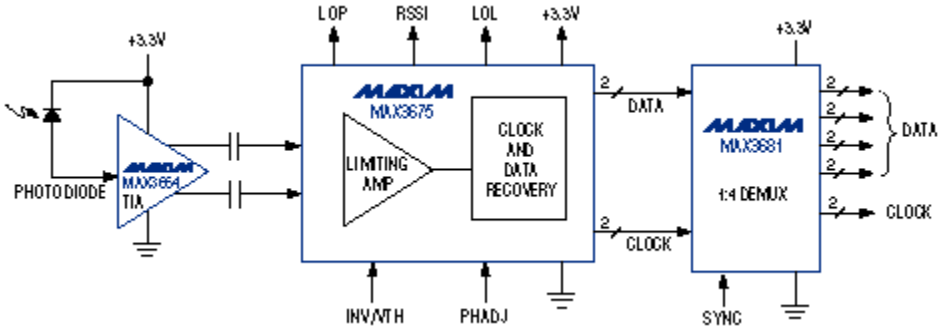


*Figure 4. Three packages from Maxim form an STM 4 receiver.*

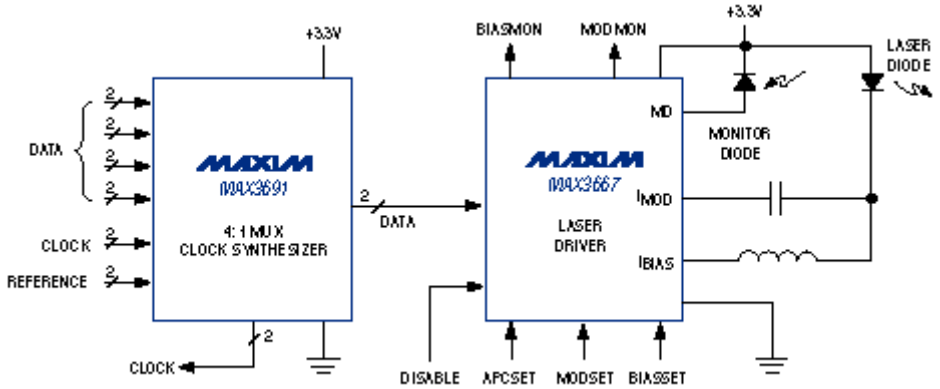


*Figure 5. Two packages from Maxim form an STM 4 transmitter.*

The chipset is based on Maxim's state-of-the-art, high-performance bipolar technologies: CB-2 and GST-2. CB-2 is a fast, complementary-bipolar process whose transit frequencies are 6.4GHz for pnp transistors and 8.7GHz for npn transistors. GST-2 is a very-high-speed, submicron bipolar process with a transit frequency of 27GHz for npn transistors.

The combination of modern high-performance manufacturing and extensive IC design experience has produced a highly integrated, flexible, and powerful STM 4 chipset consisting of five ICs including the serializer and deserializer. In serial-I/O modules the chipset consists of only three ICs, and they can be delivered in die form to accommodate "chip-on-board" mounting technology.

Power dissipation is an important consideration because system cooling requirements usually allow only a limited power budget in the O/E units. Maxim's STM 4 chipset makes extensive use of 27GHz, high-speed technology in reducing power dissipation. It can further reduce power dissipation by operating on +3.3V instead of today's more common +5V. Rather than require an additional source of +5V, the O/E unit can use the +3.3V available for CMOS system components. Or, to be flexible, it can share an existing +5V supply with the front-end ICs. In addition to these features, which pertain to the chipset as a whole, features specific to the individual components are described in the following sections.

### Preamplifier (i.e., transimpedance amplifier)

The transimpedance amplifier (MAX3664) converts a single-ended current from the detector diode to a single-ended voltage, which is amplified and converted to a differential signal. Typical amplification is 6kW. This gain level can be increased by 6dB if the data outputs (back-terminated internally with 60W) are not externally terminated as well. For input currents beyond 100µAp-p, the high gain leads to a limited differential output-voltage swing of 900mVp-p. A DC-cancellation circuit helps to deliver differential output voltages with low pulse-width distortion over a wide range of input-current levels.

Low input-related noise is achieved by careful circuit design and by limiting the bandwidth to 590MHz at an input capacitance of 1.1pF. Assuming a simple PIN detector diode is used, the low noise enables a typical input sensitivity of -32dBm optical power. Power dissipation is less than 85mW at +3.3V. Small size and an optimal bondpad configuration make this component suitable for use in PIN-TIA modules, which combine a PIN diode and transimpedance amplifier in one package (a TO package, for instance).

### Clock and Data Recovery (CDR)

The main functions of the clock and data recovery IC (MAX3675) are to recover the clock signal from the received data stream and to regenerate the data's timing and amplitude characteristics. Because the chip integrates an offset-compensated limiting amplifier as well, two standard products (MAX3664 and MAX3675) contain all the electronics necessary for an O/E receiver unit.

The MAX3675 offers a high-sensitivity differential analog input (3mVp-p) and a differential PECL digital input, providing flexibility that supports a wide range of receiver applications. The MAX3675's power dissipation depends on the input in use: 215mW with analog inputs, or 155mW with digital inputs. Total power consumption for a complete receiver based on the MAX3664 and MAX3675 is less than 300mW at +3.3V.

An LOP alarm function and input-power detector are integrated with the limiting amplifier. The LOP alarm warns if the input signal falls below a user-defined threshold. The reference for this threshold is an internal bandgap circuit that is independent of the supply voltage. To ensure chatter-free operation for input signals near the threshold, the LOP's TTL-monitor output includes hysteresis. The power detector provides a receive signal-strength indicator (RSSI pin) whose output voltage is proportional to input power and is linear in decibels.

The PLL necessary for clock recovery is fully integrated and does not require an external reference clock. It consists of a phase/frequency detector, a loop-filter amplifier with external RC network, and a 622MHz voltage-controlled oscillator. The PLL provides an LOL signal

(LOL pin) and a TTL-monitor output that flags when the PLL loses lock. To improve the system's bit error rate as described in the *Optical Receivers*section, users can adjust clock phase relative to the data signal by accessing the pins PHADJ+ and PHADJ-. Finally, a decision circuit supported by the recovered clock signal (from the PLL) regenerates timing and amplitude characteristics for the incoming data stream.

### Deserializers (DEMUX)

To support the various CMOS system-interface circuits available today, Maxim offers the MAX3680 and MAX3681 deserializers. The MAX3680 converts a 622Mbps serial data stream to a 78Mbps stream of 8-bit words. Data and clock outputs are TTL compatible, and the power consumption is 165mW at +3.3V. The MAX3681 converts a 622Mbps serial data stream to a 155Mbps stream of 4-bit words. Its differential data and clock outputs support an LVDS interface for CMOS system components, and its power consumption is 265mW at +3.3V. Both parts offer serial differential-PECL inputs for data and clock, and a synchronization function (SYNC pin) that enables a bit realignment of the deserializer's data outputs.

### Serializer (MUX)

The MAX3691 serializer converts four LVDS data streams at 155Mbps to a serial stream at 622Mbps. The necessary transmission clock is synthesized using a fully integrated PLL comprising a voltage-controlled oscillator, a loop-filter amplifier, and a phase/frequency detector that requires only an external reference clock. All the data- and clock-input buffers are LVDS-compatible, and the serial data output delivers differential-PECL signals. Power dissipation is 215mW at +3.3V.

### Laser Driver (LD)

The main task of the laser driver (MAX3667) is to deliver the bias (IBIAS) and modulation current (IMOD) for a direct-modulated laser diode. For flexibility, the differential inputs accept PECL data streams and also differential voltage swings as small as 320mVp-p, with DC levels in the range 1V to (VCC - 0.75V). Connecting an external resistor between BIASSET and ground lets you adjust the bias current between 5mA and 90mA, and a resistor between MODSET and ground lets you adjust the modulation current between 5mA and 60mA.

An integrated, temperature-stabilized reference voltage ensures stable bias and modulation currents. To avoid laser damage, a protection circuit disables the MAX3667 when any of the pins BIASSET, MODSET, or APCSET are short-circuited to ground. To avoid excessive current that could alter the laser's performance, an internal circuit also limits the sum of output currents IMOD and IBIAS to approximately 150mA. As described in the *Optical Transmitter* section, an integrated APC circuit, supported by an external detector diode, maintains the initial user-defined average laser power constant over time and temperature.

The detector diode's average current value is established by applying an external resistor between the APCSET and GND pins. Two monitor outputs (BIASMON and MODMON) deliver output currents directly proportional to the bias and modulation currents. The bias, modulation, and APCSET currents can be disabled via the DISABLE pin, but all other functions including the reference voltage remain active to allow a fast and predictable wake-up. In addition, an integrated slow-start function provides a 50ns minimum turn-on time that reduces laser stress. In contrast to other laser drivers available in today's market, the MAX3667 can operate from a single +3.3V supply.

As an alternative to the 622Mbps MAX3667, the MAX3766 laser driver can be used for STM 4 transmitter units supporting data rates from 155Mbps to 1.25Gbps. Designed to operate on a single +5V supply, the MAX3766 incorporates all attributes mentioned for the MAX3667 plus the larger bandwidth (to 1.25Gbps). Other features include extensive laser-safety provisions and the option to add a single external resistor that maintains "optical amplitude" by compensating for the effect of temperature on the slope of the characteristic laser curve. The resistor's value depends on the laser diode's temperature characteristic.

**MORE INFORMATION**

MAX3664: QuickView -- Full (PDF) Data Sheet (248k)

MAX3667: QuickView -- Full (PDF) Data Sheet (648k) -- Free Sample

MAX3675: QuickView -- Full (PDF) Data Sheet (568k) -- Free Sample

MAX3681: QuickView -- Full (PDF) Data Sheet (64k) -- Free Sample

MAX3691: QuickView -- Full (PDF) Data Sheet (90k) -- Free Sample