# SONY CXB1107Q/Q-Y

T-46-07-08

## Decision Circuit with Differential I/O

### Description

The CXB1107Q is an ECL ultra high speed monolithic Decision Circuit, which contains a D Flip-Flop with High Gain Slicer at the input stage.

Differential data input is amplified by the High Gain Slicer and stored in the D Flip-Flop at the positive transition of the Clock. The stored data is held at Q and $\overline{Q}$ pins untill the next positive transition of the Clock occurs. The Clock input has differential input pins C and $\overline{C}$. Built-in reference voltage is provided at $V_{BB}$ pins to facilitate the use of single input operation.

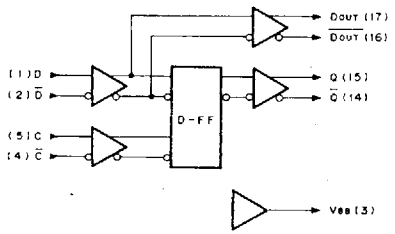
### Features

- Typical AC characteristics: Clock rate up to 3.2GHz
  Clock rate up to 2.3GHz at an input level of 50mV
- Differential Data and Clock inputs
- Internal pull down resistors on input pins to maintain logic LOW level with the pins left open
- ECL 100K compatible I/O levels

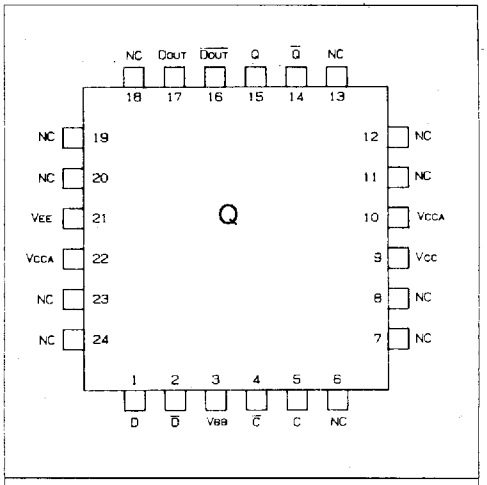
### Pin Names

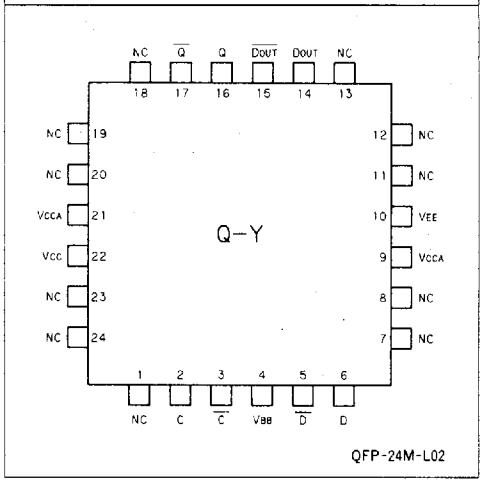
| | |
|---|---|
| D, $\overline{D}$ | Data input |
| C, $\overline{C}$ | Clock inputs (positive edge trigger) |
| Q, $\overline{Q}$ | Data output |
| $D_{OUT}$, $\overline{D_{OUT}}$ | Buffered input data outputs |
| $V_{BB}$ | Reference voltage output |
| $V_{CC}$ | Circuit ground |
| $V_{CCA}$ | Circuit ground for outputs |
| $V_{EE}$ | Negative power supply |

### Logic Symbol




### Pin Assignment




QFP-24M-L02

T-46-07-08

## DC Characteristics

$V_{EE}=-4.5\pm0.3V$, $V_{CC}=V_{CCA}=GND$, $V_{TT}=-2.0V$, $T_C=0°C$ to $+85°C$

| Item | Symbol | Test Condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| Power supply current | $I_{EE}$ | | −116 | −85 | −59 | mA |
| Input voltage range | $V_{IN}$ | | −2.0 | −1.3 | −0.5 | V |
| Min. Decision voltage | $V_D$ | $f_{CLOCK}=1.8GHz$ | | | 50 | mVpp |

Note: Other DC characteristics; See pages 3-3 and 3-4.

## AC Characteristics

$V_{EE}=-4.5\pm0.3V$, $V_{CC}=V_{CCA}=GND$, $V_{TT}=-2.0V$, $T_C=0°C$ to $+85°C$, $R_T=50\Omega$ to $V_{TT}$

| Item | Symbol | Input | Output | Test Condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|---|---|
| Propagation delay time | $T_{PLH}$ | C | Q | | 460 | 610 | 770 | ps |
| | $T_{PHL}$ | | | | 440 | 590 | 750 | |
| | $T_{PLH}$ | D | $D_{OUT}$ | | 420 | 570 | 730 | |
| | $T_{PHL}$ | | | | 400 | 550 | 710 | |
| Set up time | $T_S$ | D, C | Q | | 220 | | | |
| Hold time | $T_h$ | C, D | | | 120 | | | |
| Max. Clock frequency | $f_{MAX}$ | D | | Vin=50mVpp | 1.8 | 2.3 | | GHz |
| | | | | Vin=800mVpp | 2.6 | 3.2 | | |
| Rise time | $T_{TLH}$ | C | | 20% to 80% | | 220 | 280 | ps |
| Fall time | $T_{THL}$ | | | | | 170 | 220 | |

Note: AC test circuit; See pages 4-3, 4-4 and 4-5.

## Truth Table

| Input | | Output | |
|---|---|---|---|
| D | C | Q | $D_{OUT}$ |
| L | L | Hold | L |
| H | L | Hold | H |
| L | ∫ | L | L |
| H | ∫ | H | H |
| L | H | Hold | L |
| H | H | Hold | H |

Note: H; HIGH voltage level
L; LOW voltage level
∫; Positive transition edge
Hold; Means no-change in the output

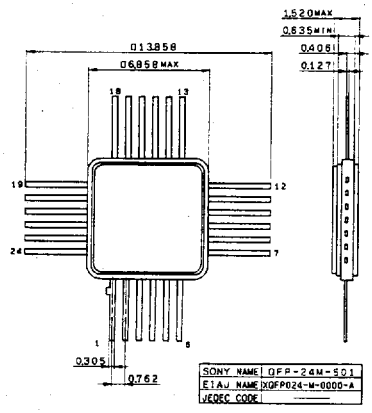
# Package Data

T-90-20

**Package Outline** Uuit: mm

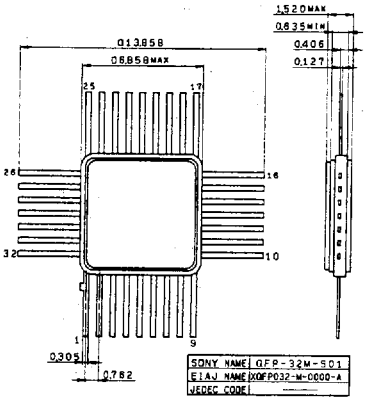
24pin QFP (QFP-24M-S01)

24pin QFP (Metal) 0.3g



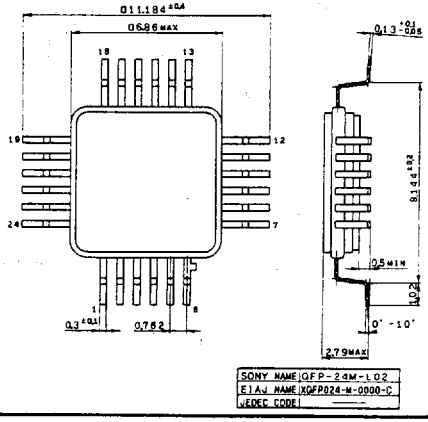

32pin QFP (QFP-32M-S01)

32pin QFP (Metal) 0.2g




24pin QFP (QFP-24M-L02)

24pin QFP (Metal) 0.3g



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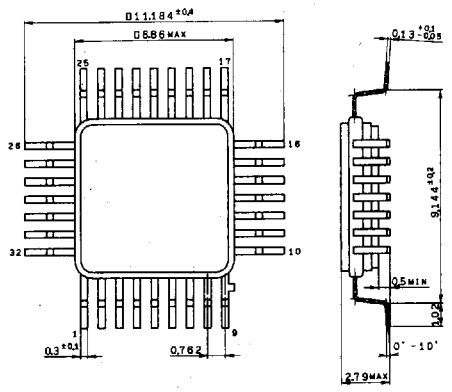
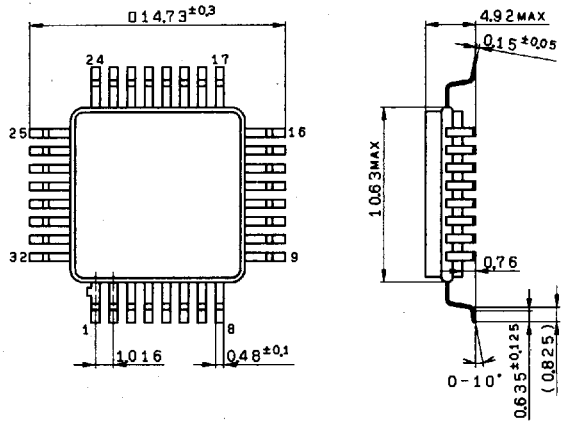



| | |
|---|---|
| SONY NAME | QFP-32M-L02 |
| EIAJ NAME | XQFP032-M-0000-C |
| JEDEC CODE | |

32pin QFP (QFP-32C-L01)

32pin QFP (Ceramic)




| | |
|---|---|
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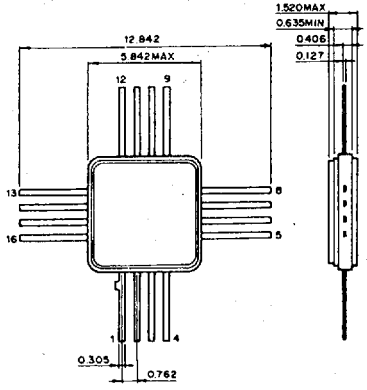
| EIAJ NAME | XQFP032-G-0000-A |
| JEDEC CODE | |

16pin QFP



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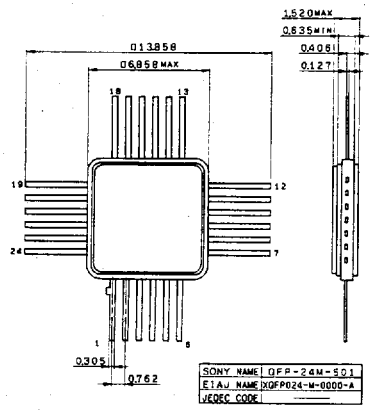


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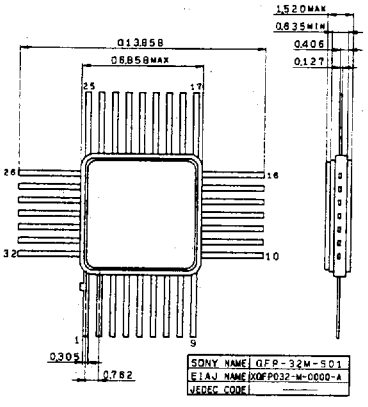
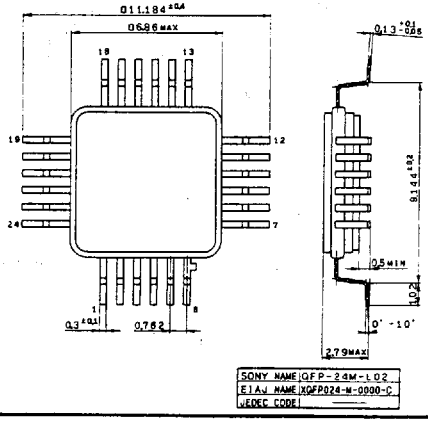


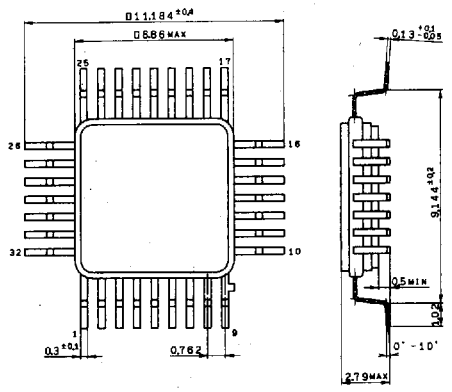

24pin QFP (QFP-24M-L02)

24pin QFP (Metal) 0.3g



32pin QFP (QFP-32M-L02)

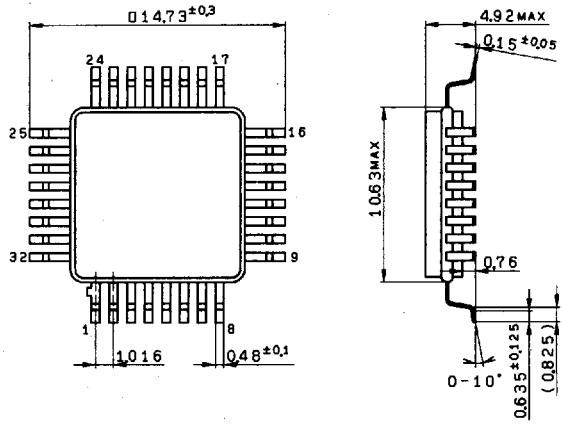
32pin QFP (Metal) 0.2g




| | |
|---|---|
| SONY NAME | QFP-32M-L02 |
| EIAJ NAME | XQFP032-M-0000-C |
| JEDEC CODE | |

32pin QFP (QFP-32C-L01)

32pin QFP (Ceramic)




| | |
|---|---|
| SONY NAME | QFP-32C-L01 |
| EIAJ NAME | XQFP032-G-0000-A |
| JEDEC CODE | |

16pin QFP